89633300

CONTROL DATA CORPORATION

CONTROL DATA®
CENTRAL PROCESSING UNIT

AB107 AB108

BA201 BT148

BU120 GD611

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
02	ECO CK0456 released manual to class B.
(January 1974)	
03	ECO CK0522 and ECO CK0748 completely revised manual.
(October 1974)	
04	ECO CK1117 revised manual.
(March 1975)	
A	ECO CK1312 released manual to class A.
(August 1975)	
B	ECO CK1347 affected pages: xv, 2-5, 2-6, 3-13, 3-19, 5-7, 9-1, 9-147.
(October 1975)	
C	ECO CK1421 incorporated Field Change Orders CK1415, CK1422, CK1431.
(January 1976)	Pages revised: ii to xv, 3-13, 4-45, 4-46, 4-56, 5-39, 5-87, 5-145, 5-151, 5-155, 5-159, 5-259
	5-379, 5-380 to 5-383, 5-385, 5-389, 5-393, 5,397, 5-403, 5-408, 5-409, 5-414 to 5-421, 5-430,
	6-4, 8-1, 8-2, 9-2, 9-7, 9-26, 9-36, 9-37, 9-40, 9-45, 9-49, 9-55, 9-57, 9-63, 9-80, 9-85, 9-88,
	9-89, 9-90, 9-93, 9-98, 9-147
	Pages added: 3-13A, 3-13B, 5-160 to 5-166, 5-410 to 5-413, 5-422, 9-2A.
D	ECO CK1559 incorporated ECO CK1526 and CAR's LJL043, 158, 173, 174.
(July 1976)	
E	ECO CK1830.
(July 1977)	CAR's incorporated: LJL046/268, LJL072/383, Internal CAR 406, LJL186/505, LJL199/515, LJL203-381/517, LJL206/519, LJL207/520, LJL211/524
	ECO's incorporated: CK1054, CK1436, CK1588, CK1788, and ECO/FCO CK0676.
	Pages added: 3-29, 3-30, 8-3. Pages deleted: 9-2A.
	Pages revised: iii to vi, viii, xii to xvii, 4-5, 4-9, 5-23, 5-32, 5-36, 5-82, 5-89, 5-145, 5-296,
	5-371 to 5-420, 5-435, 6-4, 6-27, 8-1, 8-2, 9-1 to 9-8, 9-43, 9-61.
	Updated: Manual-to-Equipment Correlation sheets and Parts Data.
F	ECO CK1996 Incorporated Models C and D. Reference CAR LJL209/522, CAR LJL216/531.
(November 1977)	
G	ECO CK2784 corrected the following:
(July 1979)	Wrong Console PWA part number 89602068 changed to 89602069: pages 5-143, 5-145, 5-157.
	Switchcap part number 89769400 added to Parts Data; 29 must be ordered with Console PWA 89602069
	in series A13 up: pages 8-1, 8-2. Page 8-3 deleted by new layout.
	Three wires changed in wiring list due to ECO/FCO CK2372: pages 9-34, 9-67, 9-68.
	Drawing error corrected by adding connection. U5-11 (sheet 6) to U52-4 (sheet 2): page 5-395.
H	ECO CK 3018 Incorporated changes of Series Codes, part numbers and pin numbers in the wiring list.
(July 1980)	Ref. CAR 252 and TAR 065965. Pages to be replaced: ii, iii/iv, 5-143, 5-421, 5-425, 5-429/5-430,
	5-431/5-432, 8-1, 8-2, 8-3/8-4, 9-46, 9-65, 9-66, 9-71 and Comment Sheet.

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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

MANUAL REVISION	EQUIPMENT TYPE	WITH ECO/FCO			COMMENTS
02	AB107-A04	CK0573			
	AB108-A04	CK0263			
	AB107/8-A05	CK0677			
	AB107/8-A06	CK0705			
	AB107/8-A07	CK0736			
	BT148-A04	CK0668			
	BA201-A03	CK0652			
	BA201-B03	CK0457			
02/03/04	BA201-A/B04	CK0673			
	BU120-A03	CK0705			
02 up	GD611-A02	CK0245			
03	AB107/8-A08	CK0840			
	BT148-A05	CK0677			
	BU120-A04	CK0939			
04	AB107/8-A09	CK1063			
	AB107/8-A10	CK1011			
	AB107/8-A11	CK0992			
	AB107/8-A12	CK1241			
	BT148-A06	CK1063			
	BU120-A05	CK0992			
A/B	AB107/8-A13	CK1109			
	BT148-A07	CK0906			
	BA201-A/B05	CK0978			
	BU120-A06	CK1241			
C	AB107-A14	CK1272			
	AB108-A14	CK1273			
	AB107/8-A15	CK1416			
	AB107/8-A16	CK1415			
	AB107/8-A17	CK1431			
	BT148-A08	CK1415			
	BU120-A07	CK1272			
D/E	AB107/8-A18	CK1448			
	AB107/8-A19	CK1526			
	BU120-A08	CK1588			
F	AB107/8-C01	CK1491,1931			
	AB107/8-C02	CK1502,1931			
	AB107/8-C03	CK1562,1931			
	BT148-C01	CK1491			
	BT148-C03	CK1842			
	AB107/8-D01	CK1909,1931			
	BT148-D01	CK1909			
G/H	AB107/8-D02	CK2372			

PREFACE

This manual provides customer engineering information for the CONTROL DATA® AB107 and AB108 with memory and supporting equipment. The AB107 and AB108 computers are physically compact and are designed for high computation and input output speeds. They feature a semiconductor memory with a basic size of 4096 (4K) 18-bit words which is field expandable in 4K word increments to 65K words.

NOTE: Equipments identified without type identifier A,C,D refer to all three.

The following Control Data publications may be useful when installing and maintaining this equipment.

Control Data Publication	Pub. No.
1784 Computer System Reference Manual	89633400
1784 Key to Logic Symbols	89723700
System Maintenance Monitor Manual (SMM17)	60182000
AB107/AB108 Execution Charts	89723800
1784 Computer Input-Output Specification Manual	89673100
CDC Mini-Computer System Site Preparation Manual, section 2	60437000

1784 Computer System Peripheral Equipment Hardware Maintenance Manuals: (HR/M means combined Hardware Reference/Maintenance Manual)

AF108 Paper Tape Reader/Punch Controller	HR/M	89865200
AT310 TTL A/Q DSA Bus Expander		89758600
DJ815 Asynchronous Communications Controller	HR/M	89600054
FA442 ICL Magnetic Tape Transport Controller		89637700
FA446 LCTT Magnetic Tape Transport Controller		89637700
FA716 Cartridge Disk Drive Controller		89638100
FC106 Key Entry Station Controller		89672200
GN109 Key Entry Distribution Unit		89672200
FE119 Card Reader Controller	HR/M	89637500
FE203 Card Punch Controller		89910800
FF524 Line Printer Controller		89637300
FJ505 Binary Synchronous Communication Controller		89934100
FJ606 Synchronous Communications Controller		89638500

(Continued on next page)

Control Data Publication	Pub. No.
FV497 ICL Phase Encoding Formatter	89796100
FV618 LCTT Phase Encoding Formatter	89796100

The following list includes the documents associated with the conversational display terminal:

Title	Publication No.
713-10 Operator's Guide	62037900
713-10 Reference Manual	62033400
713-10 On-Site Maintenance Manual	62048500
713-10 Installation Instruction	62048700

Following is a list of documents relating to the non-impact printer station:

Title	Pulication No.
713-11 Operator's Guide	62149600
713-11 Reference Manual	62149700
713-11 Installation Instructions	62149800
713-11 On-Site Maintenance Manual	62149900

Other Publications

For 33 ASR/KSR teletypewriters:

- Teletype Bulletin 310B, Volume 1
- Teletype Bulletin 310B, Volume 2
- Teletype Bulletin 1184B, Parts Schematic package WDP0316 includes document Nos. 11805D, 9334WD, 9335WD, 9336WD, 4970WD, 7887WD, 181821, 183079, 183087.

For 35 ASK/KSR teletypewriters:

- Teletype Bulletin 281B, volume 1
- Teletype Bulletin 281B, Volume 2
- Teletype Bulletin 1201B, Parts Schematic Package.

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SECTION 1

GENERAL DESCRIPTION

GENERAL DESCRIPTION

INTRODUCTION

The CONTROL DATA® AB107 and AB108 computers are small, stored program parallel mode digital computers with semiconductor memory of a basic 4096 (4K) 18-bit words, field expandable to 65K words in 4K word increments. The main computer enclosrues houses the first 32K words (32,768) memory bank, the second bank (memory expansion) being accommodated in the BT148 Expansion Enclosure. The main computer and the expansion enclosures also house the peripheral controllers. The following table lists the equipment which make up the AB107 and AB108 computers. Equipment described in this manual (see preface for CE Manuals of associated equipments).

TABLE 1-1. EQUIPMENT DESCRIPTION

Equipment Number	Description
AB107-A	The central processing unit performs the following functions: a. Arithmetic and logical operations required by the stored program. b. Control operations to execute and synchronize operations within the central processor, in the memory and for input/output. c. Interrupt processing for one internal and fifteen external priority interrupts. d. Program protection to protect one set of programs in the memory from the effect of other programs. The equipment combines with up to eight BA201-B Memory Modules housed in the computer enclosure to provide a bank of 32,768 (32K) words of semiconductor memory storage with a cycle time of 900 nanoseconds.

AB107-A (cont'd)	The memory may be expanded by up to eight BA201-B Memory Modules to provide a second bank of 32K words housed in the BT148-A Expansion Enclosure with the BU120-A Memory Expansion Controller to give a total of 65,536 (65K) words memory. The memory is inherently volatile. It may be made non-volatile within an enclosure by installing the optional GD611-A Memory Hold Battery in the enclosure. The equipment includes the following, in addition to the central processing unit: a. Front panel Programmer's Console carrying all the system controls. b. Non-buffered input/output channel based on the A and the Q register (A/Q channel). c. Direct Storage Access (DSA) channel for the buffered data transfers from peripheral control equipment housed in the main computer enclosure or external to it. d. Controller for the standard input/output Teletypewriter. The Teletypewriter to be used is the Teletype Corp. Models ASR/KSR 33/35. e. Wiring, power supplies and enclosure for the AB107-A equipment circuits and in addition, for the following circuits: * FA716-A Cartridge Disk Drive (CDD) Controller * FA442-A/FV497-A Magnetic Tape Transport (MTT) Controller * peripheral controllers, up to four on the A/Q channel and up to three on the DSA channel * FA446-A/FV618-A Magnetic Tape Transport (MTT) Controller * GD611-A Memory Hold Battery (optional) The equipment works from 110 vac 50/60 Hz line voltage, and can be field converted to 220 vac, 50/60 Hz.

AB108-A	Equipment identical to the AB107-A except in that it combines with BA201-A Memory Modules to provide a memory cycle time of 600 nanoseconds. The input/output operations (A/Q and DSA channels) are correspondingly faster in this computer but the input/output equipment used is the same as in the AB107-A. The equipment works from 110 vac 50/60 Hz line voltage, and can be field converted to 220 vac, 50/60 Hz.
BA201-A BA201-B	Semiconductor storage module containing 4096 (4K) 18-bit words. The unit is designed to operate with the AB107 and AB108 computers and uses control logic provided by them to execute read and write operations. The storage read/write cycle durations are: BA201-A controlled by AB108-A: 600 nanoseconds BA201-B controlled by AB107-A: 900 nanoseconds
BT148-A	Expansion enclosure houses (but does not include) a) a bank of up to eight BA201-A or BA201-B Memory Modules to provide a memory expansion of up to 32,768 18-bit words for the AB107/AB108 computers. b) the BU120-A Memory Expansion Controller (similar to the Memory Controller of the AB107/AB108). c) peripheral controllers for I/O expansion. (Note that this requires TTL A/Q-DSA Bus Expander, equipment AT310-A in the main computer enclosure). The equipment includes the cabinet wiring and power supplies. It works from 110 vac 50/60 Hz line voltage and can be field-converted to 220 vac, 50/60 Hz.

GD611-A	The AB107/AB108 can utilize an optional Memory Hold Battery, equipment GD611-A,which can be housed in the computer enclosure. On failure of the main power the equipment switches automatically to the battery. This will supply power for retaining the memory content in the full memory of 32 kilowords for at least eight hours, but will not provide the equipment with normal operating capability. The battery is recharged automatically during power-on periods, and is fully charged in not more than 32 hours. The GD611-A equipment can also be installed in the BT148-A Expansion Enclosure so as to preserve the contents of the memory expansion of up to, another, 32 kilowords.

PHYSICAL CHARACTERISTICS

Dimensions (approximate) each enclosure :

Width	19	inch,	483 mm
Height	$15^{3}/4$	inch,	400 mm
Depth	20	inch,	508 mm

Weight: The basic complete enclosure weighs about 80 lbs, 36.4 kg.

ENVIRONMENT

Operating Temperature	40°F to 120°F (5°C to 50°C)
Operating Humidity	10% to 90% non-condensing
Storage and Shipping Temperature	-40°F to 160°F (-40°C to 70°C)
Storage and Shipping Humidity	0 to 100% RH non-condensing

NOTE

Extremes of temperature and humidity must not occur together.

SYSTEM POWER

Power input

104 - 127 vac, 49 - 60.6 Hz, single phase, 600 VA

or

198 - 264 vac, 49 - 60.6 Hz, single phase, 600 VA

Note: the equipment can be field-converted from one voltage range to the other (see Section 3).

Equipment ground

The equipment chassis is connected to the third (ground) lead in the line cord. It must be connected to a good ground (refer to Site Preparation Manual, publication No. 60437000).
The logic ground of the equipment is isolated from the chassis. It should be connected to the general logic ground of the installation.

SECTION 2

OPERATION AND PROGRAMMING

OPERATION AND PROGRAMMING

PROGRAMMING

For programming information refer to the 1784 Computer System Reference Manual, Publication number 89633400.

OPERATION

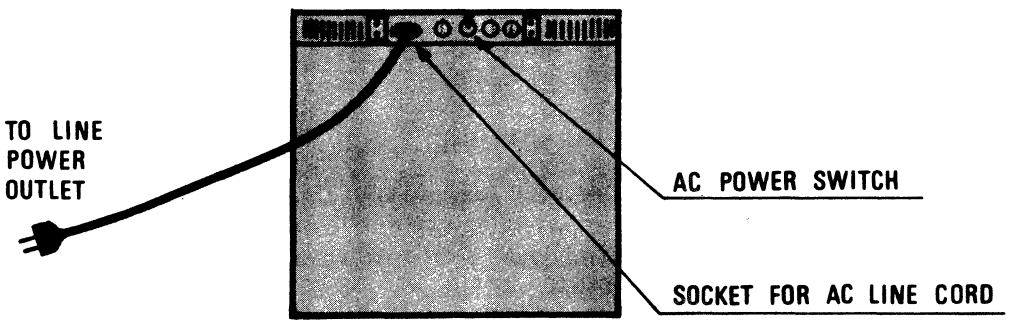
This part describes the switching on and operation of the computer using the controls and indicators on the Programmer's Console (front panel). The console is illustrated in Figure 2-2, the controls and indicators are described in section 6 of the 1784 Computer System Reference Manual, Publication number 89633400.

SWITCHING ON PROCEDURE

After the computer has been installed, checked and the initial operation procedure carried out (Section 3), the computer may be switched on by performing the following steps:

1. Connect the main computer enclosure (equipment AB107/AB108) to the power outlet by means of the power cord and apply the power by switching on the AC POWER switch at the top of the enclosure rear panel (Figure 2-1).

ENCLOSURE REAR PANEL

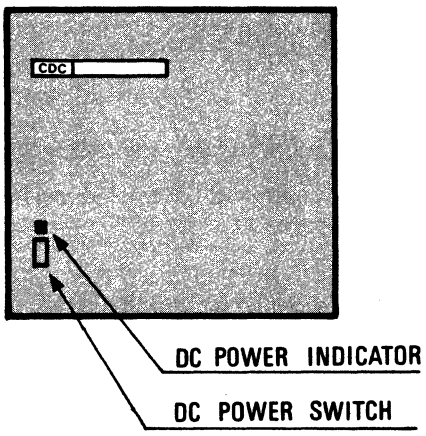


2. Switch ON the dc POWER switch on the Programmer's Console front panel (see Figure 2-2). The indicator above the switch should light.

WARNING

If the indicator does not light or if any other fault is suspected, the computer must be switched off immediately by turning off the AC POWER switch at the top of the rear panel. Refer to Section 6 for further procedures.

EXPANSION ENCLOSURE FRONT PANEL



3. If an expansion enclosure (equipment BT148) is connected, carry out steps (1) and (2) above for the expansion enclosure. The controls on the expansion enclosure are in the same relative positions as those on the main computer enclosure.

WARNING

Should it become necessary to switch off the computer always switch off the expansion enclosure first at the rear panel AC POWER switch.

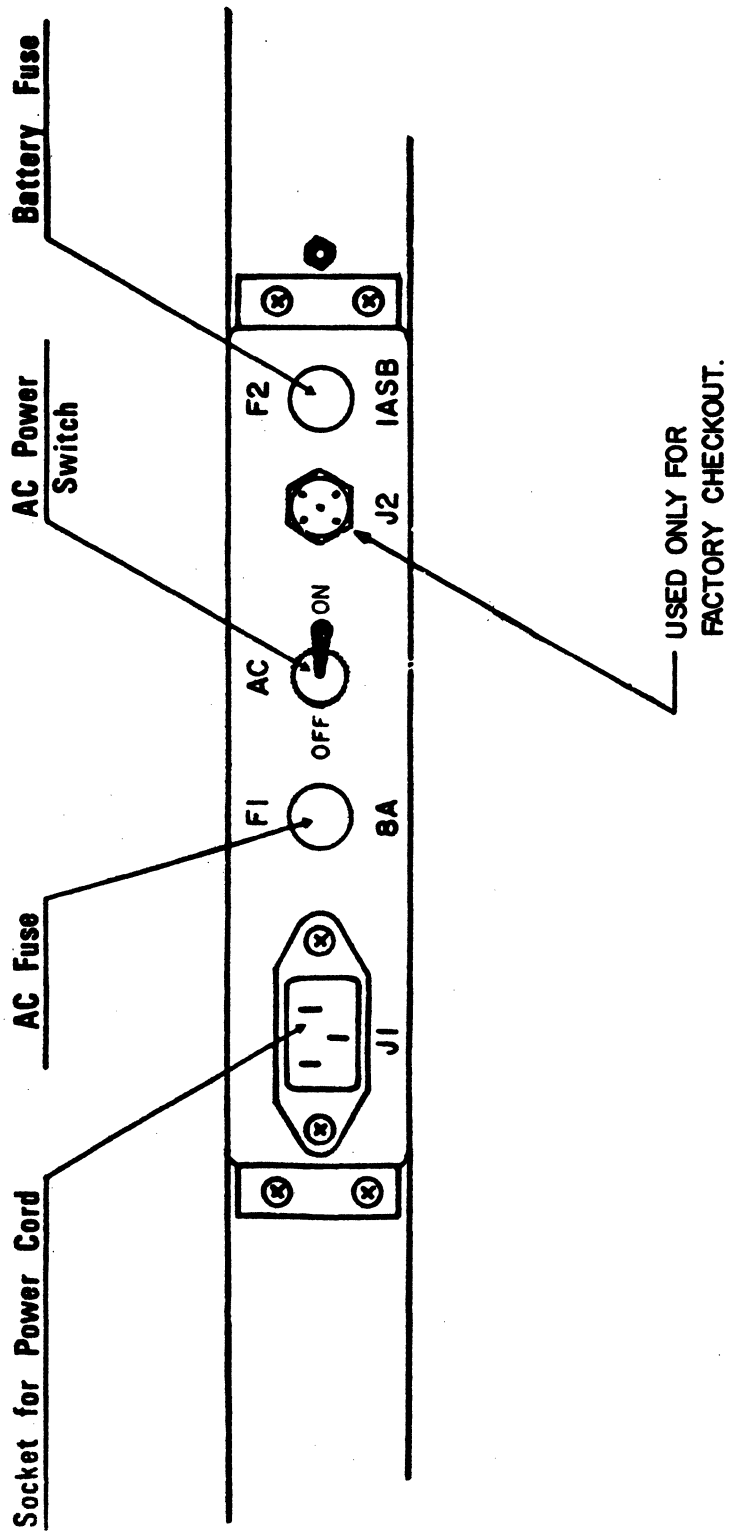


Figure 2-1. AC Power Switch and Connection

INITIAL CONDITIONS AND OPERATION

NOTE

The manual controllers and indicators on the Programmer's Console (front panel) are shown in Figure 2-2 and are described in Section 6 of the 1784 Computer System Reference Manual, Publication number 89633400.

Set up initial conditions by the following procedure (use the controls on the Programmer's Console).

1. The installation has up to 32K word memory:

   1.1 Press MASTER CLEAR pushbutton.

   1.2 Set Mode switch (65K/32K) to 32K.

   1.3 Set ENTER/SWEEP switch to ENTER.

   1.4 Set INSTRUCTION/CYCLE switch to its central (COMPUTE) position.

   1.5 Set PARITY FAULT STOP switch to the central (off) position.

   1.6 Set SELECTIVE STOP and SELECTIVE SKIP switches to the down (off) position.

   1.7 Press the GO pushbutton.

   1.8 Press MASTER CLEAR pushbutton.

2. The installation includes memory expansion (equipments BU120-A and BA201-A or BA201-B) in the expansion enclosure (equipment BT148) and therefore has more than 32K (but less than 65K) words memory:

   2.1 Press MASTER CLEAR pushbutton on the main computer.

   2.2 Set Mode switch (65K/32K) to 65K on the main computer.

   2.3 Set ENTER/SWEEP switch to ENTER.

   2.4 Set INSTRUCTION/CYCLE switch to its central (COMPUTE) position.

2.5 Set PARITY FAULT STOP switch to the central (off) position.

2.6 Set SELECTIVE STOP and SELECTIVE SKIP switches to the down (off) position.

2.7 If the full complement of eight memory modules is installed in the expansion enclosure: set P register to $FFFF_{16}$.

2.8 Press the GO pushbutton on the main computer.

2.9 Press the MASTER CLEAR pushbutton on the main computer.

The computer may now be operated.

NOTE

Do not switch SELECTIVE SKIP or PROGRAM PROTECT switch when computer is in RUN operation.

BATTERY OPERATION

Introduction

On failure of the external ac power the computer automatically switches to the Low Power Data Retention (LPDR) mode of operation, and so connects the optional Memory Hold Battery, equipment GD611-A. In this mode, the battery (if installed) supplies the power to retain the memory content in the full memory of 32 kilowords, but the equipment does not have normal operating capability. The battery, when installed, provides power for LPDR operation for at least eight hours when fully charged. It is recharged automatically during normal operation and reaches full charge in not more than 32 hours.

Memory Expansion

The Memory Expansion Controller, equipment BU120-A, and the BT148 Expansion Enclosure provide the same facilities for power failure to the memory expansion. Thus with a Memory Hold Battery, equipment GD611-A, installed in the expansion enclosure, the full memory content can be retained for eight hours after failure of the external ac power.

Operation

Failure of the external ac power is shown by the POWER indicator light and all other indicators going dark during operation. If this happens, check the external ac supply. If this failed because of no voltage or voltage reduced under allowed tolerances (see section 1, System Power) this is indicated by "brown out" of illumination. The battery will conserve the contents of the memory for eight hours. Operation of the computer may be resumed as soon as ac power returns. If the ac power appears to be in order but the front panel indicators are still dark, switch off the AC POWER switch at the top of the computer rear panel (figure 2-1) and refer to section 6.

WARNING

Do not switch off the front panel DC POWER switch.

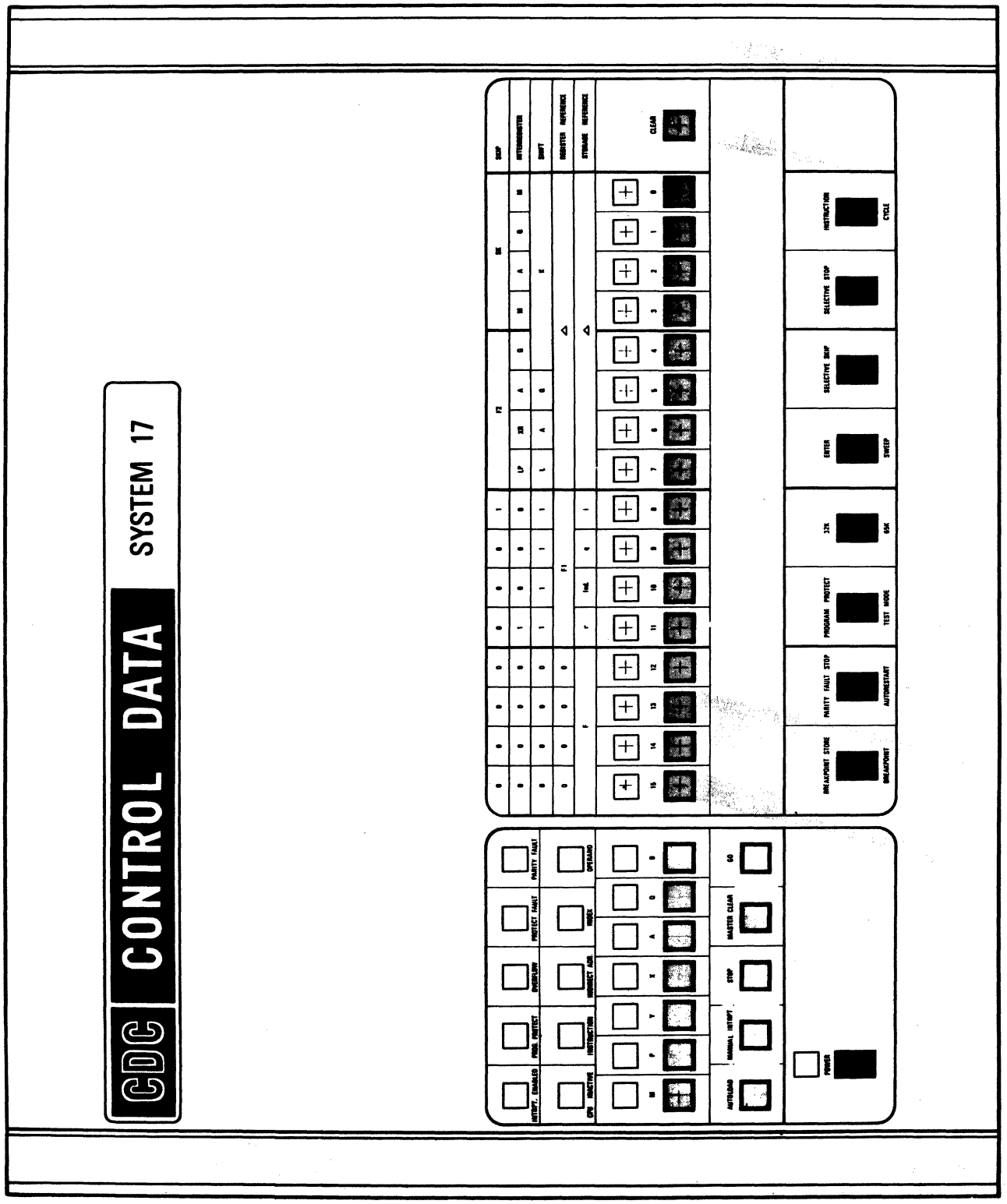


Figure 2-2. Computer Front View.
(Programmer's Console, Controls and Indicators).

SECTION 3

INSTALLATION AND CHECKOUT

INSTALLATION AND CHECKOUT

INTRODUCTION

This section provides installation procedures for the AB107/AB108 computers. To install peripheral equipments refer to the appropriate Customer Engineering or Installation manuals. Refer also to Control Data Mini Computer Systems, Site Preparation Manual, publication No. 60437000.

UNCRATING

INSPECTION

The equipment is packed in cartons with adequate packing material in the carton to isolate it from shocks in transit. A preliminary inspection of the carton must be made before uncrating. Evidence of damage must be noted and reported immediately (refer to Field Procedures Guide).

UNPACKING

To unpack the equipment lay each carton in turn on a clean smooth flat surface. Cut the sealing tape of the carton, open out the flaps, remove the packing material on top and sides of the equipment and lift out the equipment onto the clean surface beside the carton. Check the contents of each carton against packing (consignment) list and inspect each item for transit damage (dents, scratches, signs of breakage). Note and report damaged or missing parts (refer to Field Procedures Guide).

CRATING INFORMATION

Consult Control Data procedure 8.504.00 in the Customer Engineering Field Procedures Guide.

INSPECTION AND PREPARATION

Inspect the main computer enclosure and the expansion enclosure BT148 (if ordered) as follows:

a. Mechanical inspection

* Inspect the enclosure for superficial damage, loose cables and screws

* Open the enclosure

* Check the Identification Plates on the right hand side of the enclosure (inside the door). Make sure that the equipment supplied corresponds to the Customer's order

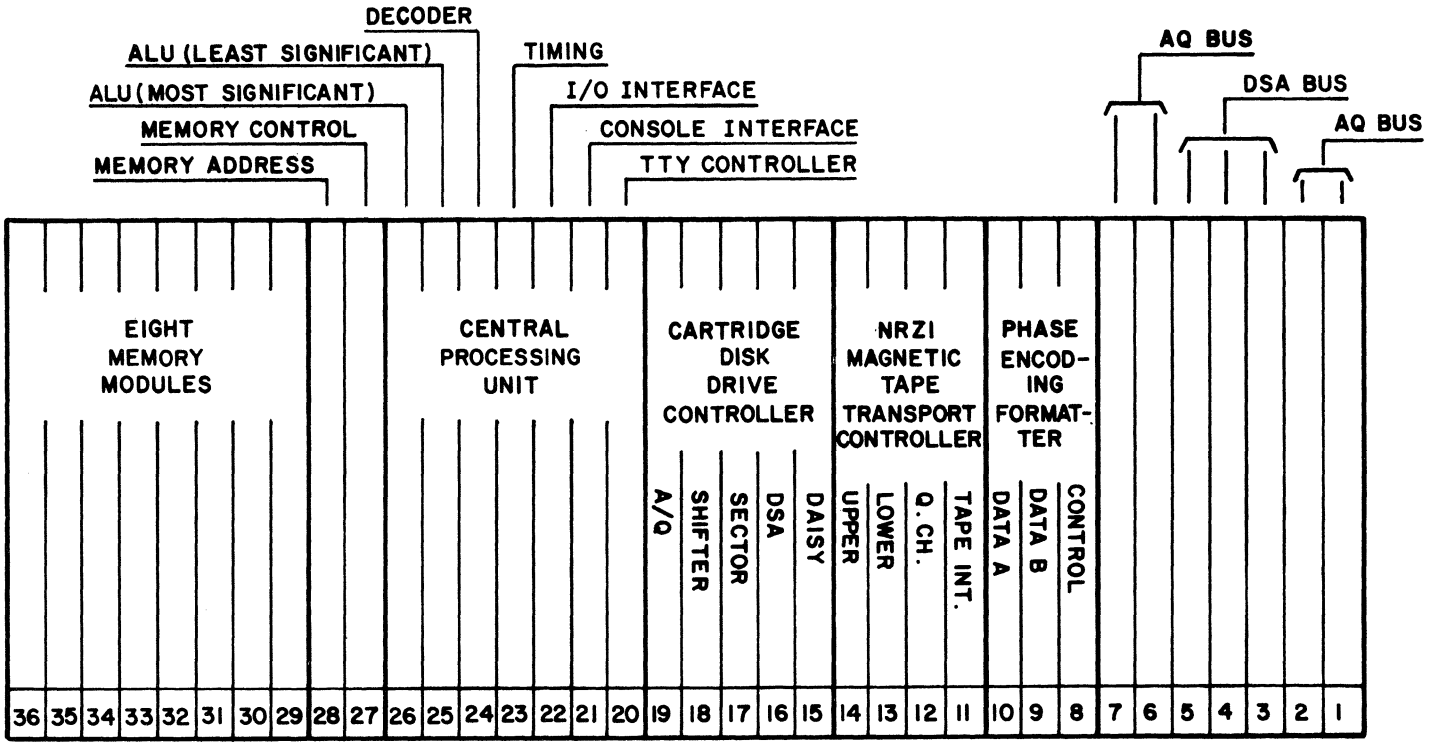
* Check that all the printed wiring assemblies corresponding to the equipments shown on the Identification Plates are inserted in their proper slots (see Figures 3-1, 3-2) If necessary insert them and stick the corresponding Identification Plate on the right side of the enclosure interior.

* Check that the computer enclosure corresponds to the Memory Modules supplied:

Enclosure		Computer Cycle Time	Memory Module
main	expansion		
AB107	BT148	900 nsec	BA201-B
AB108	BT148	600 nsec	BA201-A

* Check that each printed wiring assembly is properly seated

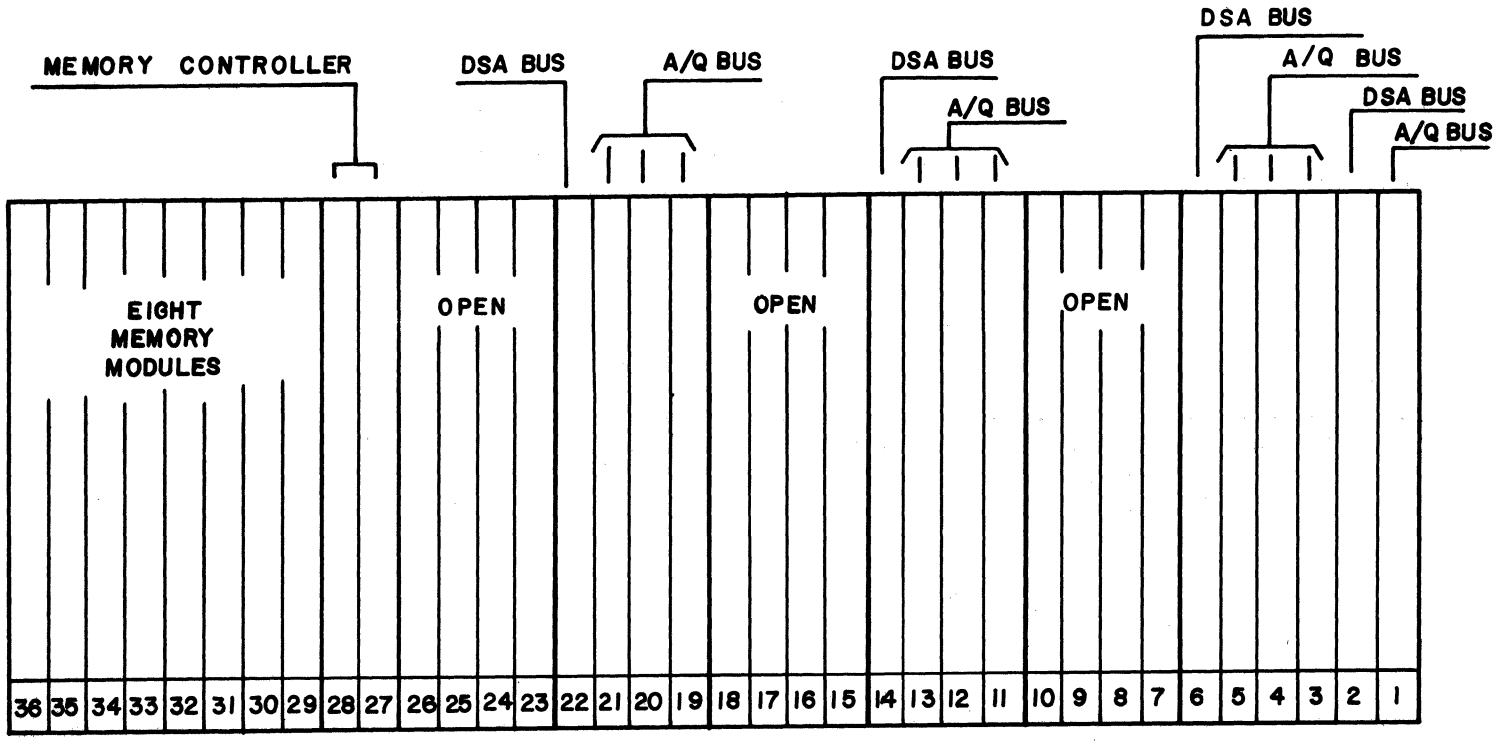
* Note serial number and part number of equipments supplied for future reference. This information is written on the Identification Plates.



NOTES

1. The Memory Control board and the Memory Address board together form the Memory Controller. This is similar to equipment BU120-A in the Expansion Enclosure.
2. Memory modules must be installed sequentially from slot 29. For instance, if equipment contains 16K, four modules are installed in slots 29 through 32.
3. See section 1 for definition of equipments.

Figure 3-1. Card Placement Slot Assignment: Main Computer Enclosure



NOTES

1. The Memory Control board and the Memory Address board together form the Memory Expansion Controller, equipment number BU120-A.

2. Memory modules must be installed sequentially from slot 29. For instance, if equipment contains 16K, four modules are installed in slots 29 through 32.

3. See section 1 for definition of equipments.

Figure 3-2. Card Placement Slot Assignment: Expansion Enclosure

b. Electrical inspection and preparation

* Check the ac line voltage available

* The equipment can accommodate one of the following nominal line voltages:

either 110 vac, 50-60 Hz, single phase
or 220 vac, 50-60 Hz, single phase

Note: the exact specifications are given in Section 1.

* Check the enclosure Identification Plate for the line voltage of the enclosure. If this coincides with the one available, skip the next paragraph and proceed to the one after; if the enclosure line voltage is not the same as that available, proceed with the modification as described in the next paragraph.

* To modify the enclosure (main or expansion) to allow it to accommodate a line voltage (110 vac or 220 vac nominal) other than it is connected for, proceed as follows:

- make sure that the enclosure is not connected to line voltage
- remove the power supply heat shield by removing its retaining screws on the inside of the enclosure front cover (refer to Figure 3-3).

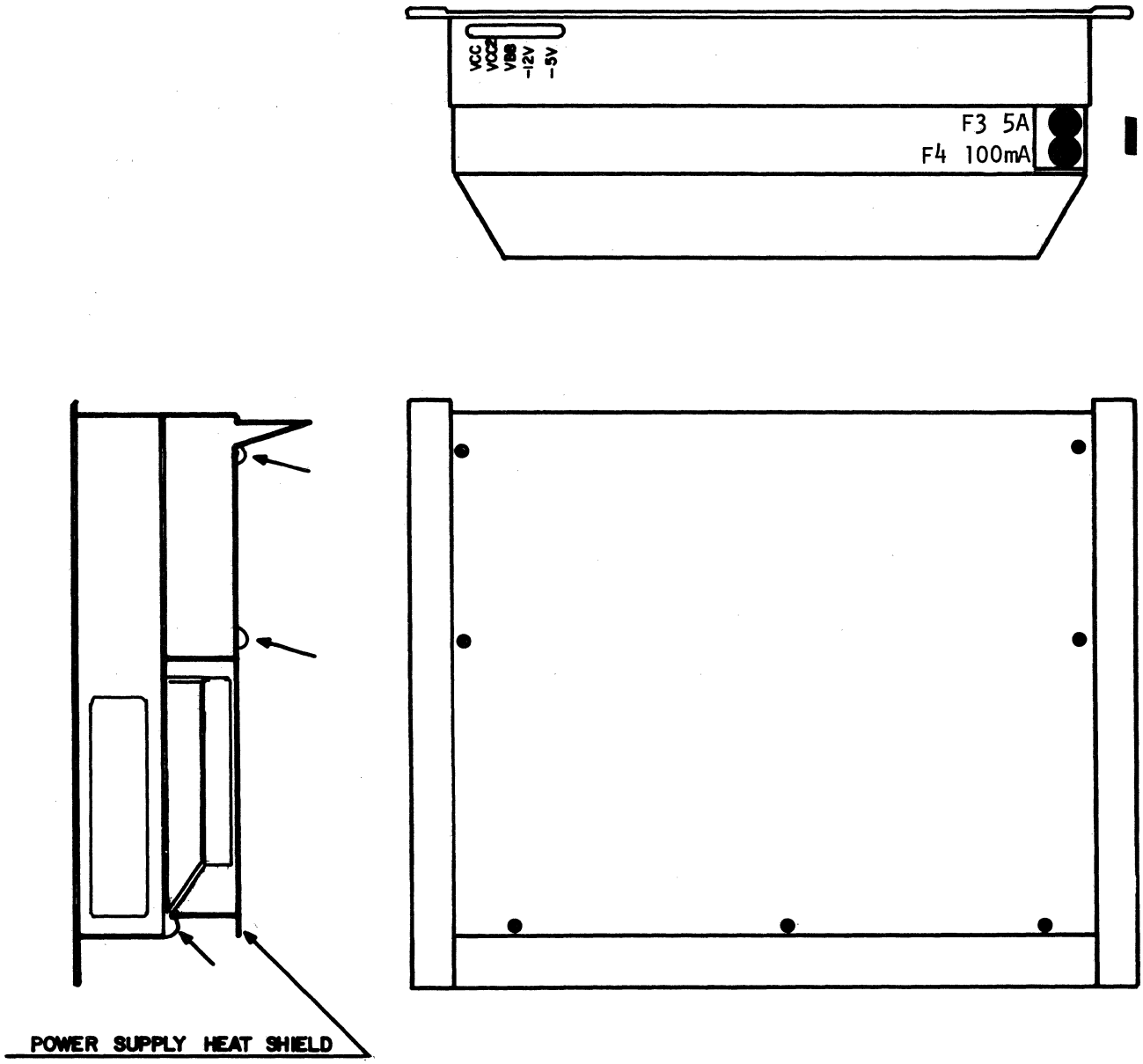


Figure 3-3. Power Supply Heat Shield and Retaining Screws

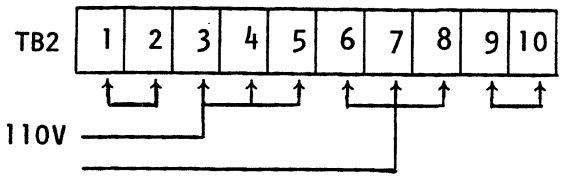
- connect the shorting links on TB2 of the power supply connection panel according to the supply voltage available. See figures 3-4 and 3-5.

NOTE: The view in figure 3-4 is exact for series A12 and down. Three areas, marked PC, PS, MH in figure 3-4, were physically altered in series A13 and up, including type identifiers C and D.

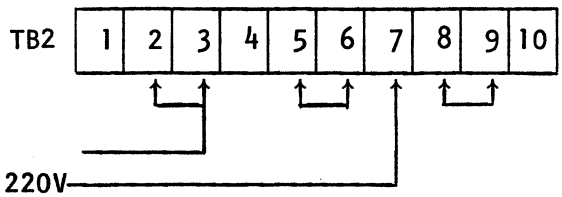
PC: The soldered connections of the programmer's console cable to the programmer's console card were replaced by two horizontal connectors, which are mounted in the same area and are marked J20 and J21 on the nearby enclosure wall.
This change affects the procedure for removing the console card.

PS: The three soldered connections to the power supply were replaced by a single vertical connector.
This change affects the procedure for removing the console card.

MH: The route of the main harness to the backplane under the cardfile was shifted away from the enclosure wall towards the center.
This change does not affect the procedure for removing the card.



SHORTING LINKS FOR 110VAC INPUT



SHORTING LINKS FOR 220VAC INPUT

NOMINAL INPUT VOLTAGE	SHORTING LINKS ON TB2 TERMINALS	INPUT TO TERMINALS
110 vac	1-2, 3-4-5, 6-7-8, 9-10	3, 7
220 vac	2-3, 5-6, 8-9	3, 7

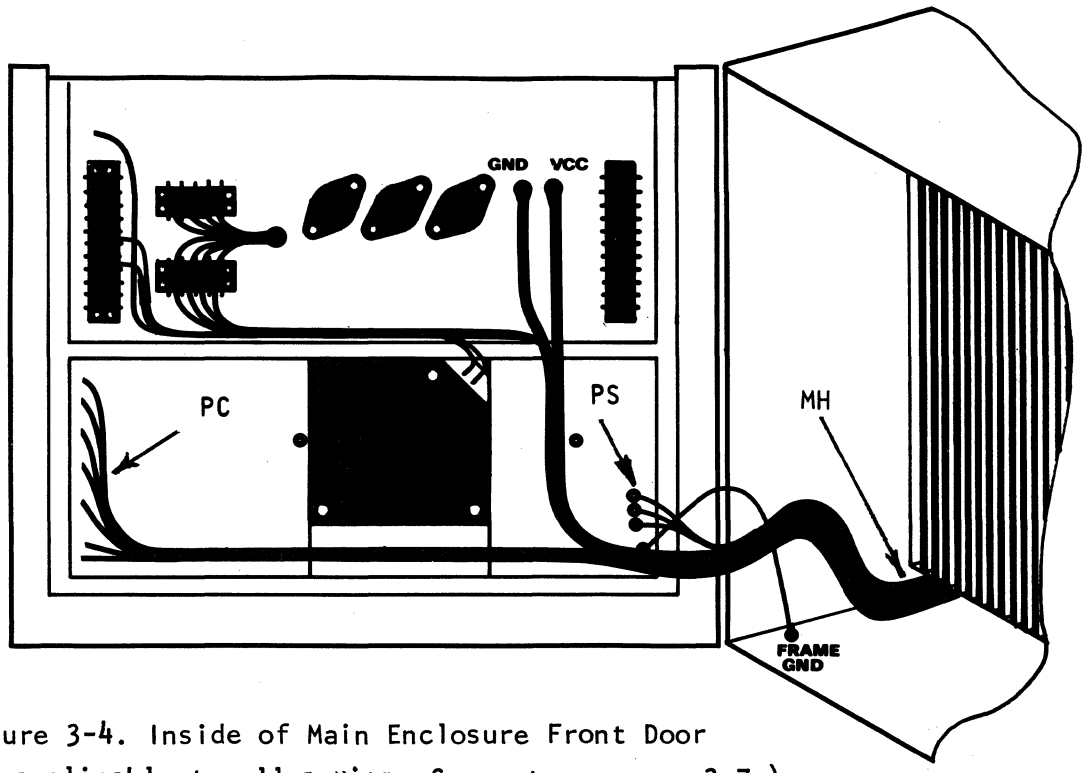


Figure 3-4. Inside of Main Enclosure Front Door
(Not applicable to all series. See note on page 3-7.)

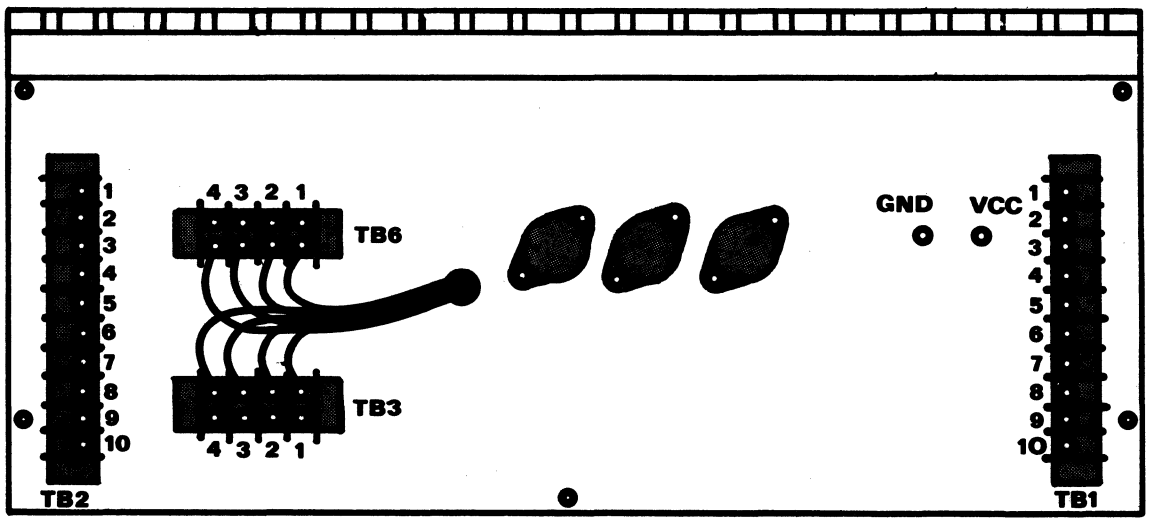


Figure 3-5. Power Supply Connector Panel

* As a further check inspect the power supply connections as follows:

  - make sure that the enclosure is not connected to line voltage
  - remove the power supply heat shield by removing its retaining screws on the inside of the enclosure front cover (unless already removed). Refer to figure 3-3 and to figure 3-4.
  - inspect the shorting links on TB2 of the power supply connection panel and make sure that they are in their correct position. Refer to figures 3-4 and 3-5.

* Check fuses:

Fuse designation	Function	Current	Speed (blow)	Location	Location refer to
F1	ac power	8 A for 110 vac	-	Input unit	Figure 3-6
		4 A for 220 vac	-		
F2	battery	1 A	slow		
F3	dc power	5 A	fast	Power Supply	Figure 3-3
F4	dc aux	100 mA	slow		

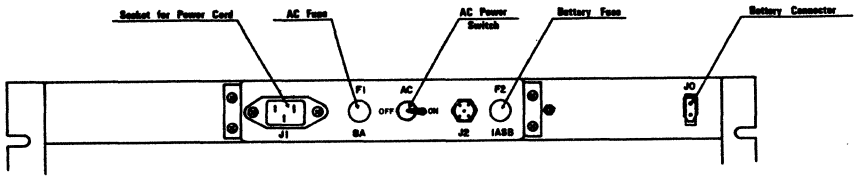


Figure 3-6. AC Power Switch and Connection

* If the system includes the memory back up power source, battery equipment GD611-A, check:

  - proper installation of the equipment in each enclosure (refer to installation procedure)

  - voltage at the battery terminals (nominal 28 vdc; for exact specification refer to Section 1)

  If the battery has to be changed refer to battery installation information at the end of this section.

* Check for electrical short circuit between conductors on the equipment power supply cable connector, also between each conductor and logic ground (do not forget the third conductor). Use highest resistance scale on the multimeter and make sure that the AC POWER switch at the top of the equipment rear panel is OFF (Figures 3-6 and 3-7).

* Check all connections for tightness.

* Reinstall the power supply heatshield by replacing its retaining screws (refer to Figures 3-3 and 3-4).

* If the system includes a BT148 Expansion Enclosure, check that the equipments match by checking the identification plates on the enclosure, on the two assemblies of the Memory Expansion Controller and on each of the memory modules (refer to the table on page 3-13).

  Make sure that the main computer and the expansion unit match.

12. If the system includes memory expansion (equipments BU120 and BA201-A or BA201-B) in the BT148 Expansion Enclosure and therefore has more than 32K words memory, carry out the following:

Switch off the dc POWER on both enclosures. Install the expansion enclosure cables (refer to Figure 3-7). Switch on the dc POWER on both enclosures.

12.1 Press STOP switch on main computer.

12.2 Make sure that the main computer and expansion equipment have the same memory cycle time (see page 3-13).

12.3 Perform steps 1 and 2 above for the enclosure.

NOTE

All control switches (except the dc POWER ON switch of the Expansion Enclosure) are located on the main computer front panel.

12.4 Press MASTER CLEAR switch.

12.5 Set Mode switch (32K/65K) to 65K.

12.6 Set ENTER/SWEEP switch to ENTER.

12.7 Set INSTRUCTION/CYCLE switch to its central (COMPUTE) position.

12.8 Set PARITY FAULT STOP switch to its central (off) position.

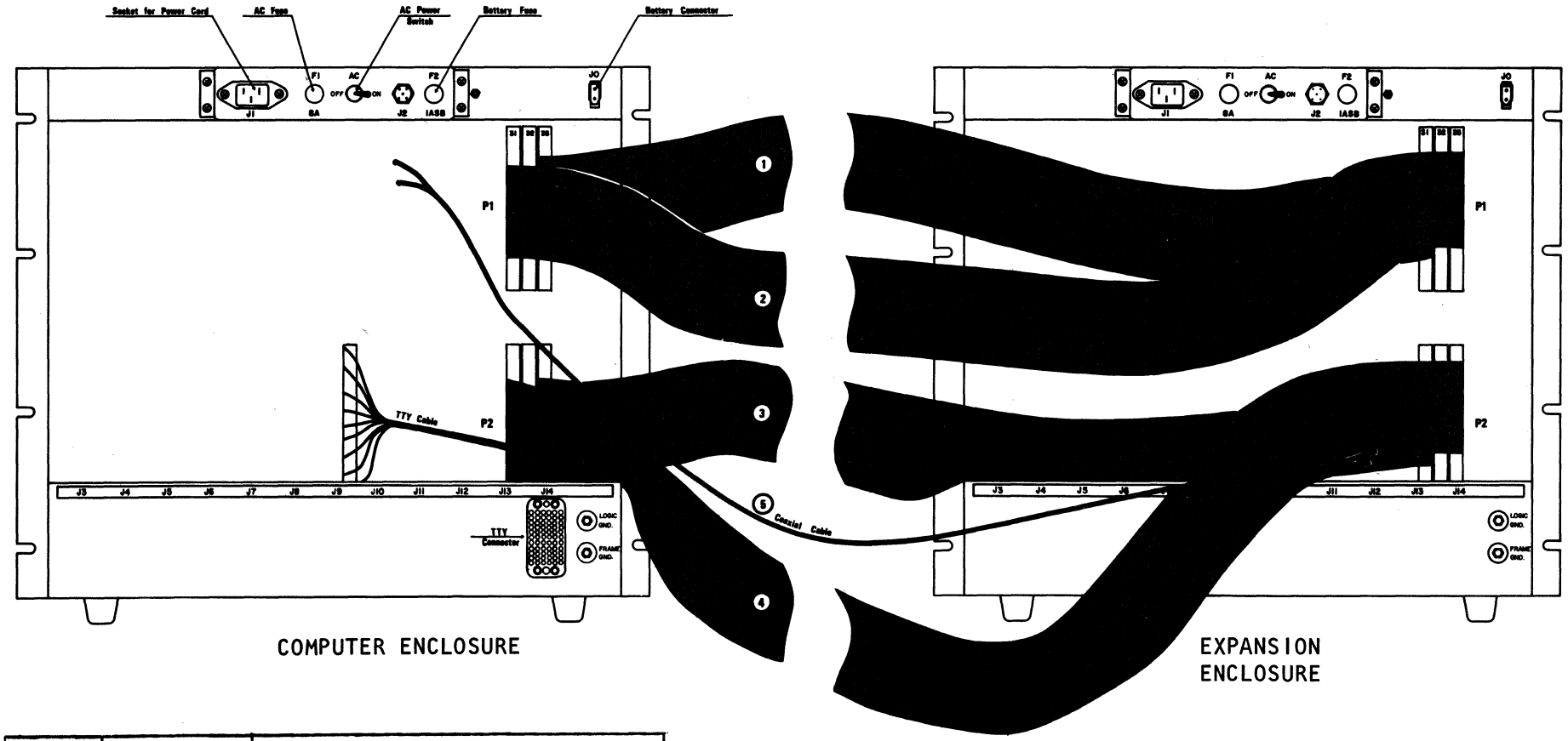
12.9 Set SELECTIVE STOP and SELECTIVE SKIP switches to their down (off) positions.

12.10 If the full complement of eight memory modules is installed in the expansion enclosure: set P register to $FFFF_{16}$.

12.11 Press the GO pushbutton.

12.12 Press MASTER CLEAR pushbutton.

12.13 Perform steps 12.4, 12.5, 12.6 above.



Cable	Part Number	Connections	
		Computer	Expansion
1	89658100	33P1	31P1
2	89658100	31P1	33P1
3	89658500	33P2	31P2
4	89658500	31P2	33P2
5	89802800	23P1A07 23P1B11(GND)	27P2A23 27P2B21(GND)

Figure 3-7. Rear of Enclosures

Memory Cycle nsec	Equipment Number		
	Memory Expansion Enclosure	Controller	Memory Module
900	BT148	BU120-A	BA201-B
600	BT148	BU120-A	BA201-A

Note power supply requirements: Initial Operation paragraph 4

Insert the Memory Expansion Controller assemblies (2) and the memory module assemblies in the slots of the expansion assigned to them and make sure that they are well seated. (Figure 3-2)

Connect the five cables of the Memory Expansion Controller (refer to Figure 3-7 and Section 9). Note that the Memory Expansion Controller (slots 27,28) are wired to slots 31 and 33 through the back plane.
The flat cables plug into slots 31,33.

* Connect on each enclosure a length of insulated wire of adequate crossection to the enclosure ground and one to the logic ground lug (refer to Figure 3-7); make sure the wire is long enough to connect the computer (or expansion enclosure) to the nearest logic ground outlet in the installation.

Adequate crossection for this ground-wire is considered to be

110 vac line voltage: AWG 12
220 vac line voltage: AWG 16

INSTALLATION

Ensure that there is no obstruction to free air circulation around either enclosure and that there is enough room to insert connectors and open the rear cover. See figures 3-8, 3-9 for the necessary clearance dimensions around the enclosure.

Ensure that the equipment is properly grounded by performing the following for each enclosure:

* check that the third pin (ground) of the power cord (chassis ground) connects to a good ground
* connect the logic ground of each enclosure to the system logic ground (refer to Figure 3-7 and the paragraphs on preparation of the equipment)
* connect the chassis ground to the system ground.

Refer to the Mini Computer Site Preparation Manual, CDC publication number 60437000.

Hook up the power by plugging the equipment line cord to the enclosure rear panel (J1: Figures 3-6 and 3-7) and then to the utility outlet.

INITIAL OPERATION

The equipment has been fully tested in the factory before despatch. The following procedure checks the equipment on first installation on site and prepares it for operation. It is assumed that it has been checked as detailed in the previous paragraphs and any discrepancies corrected.

The computer main enclosure is set up first; only when that is prepared is the expansion enclosure prepared, if it is part of the installation.

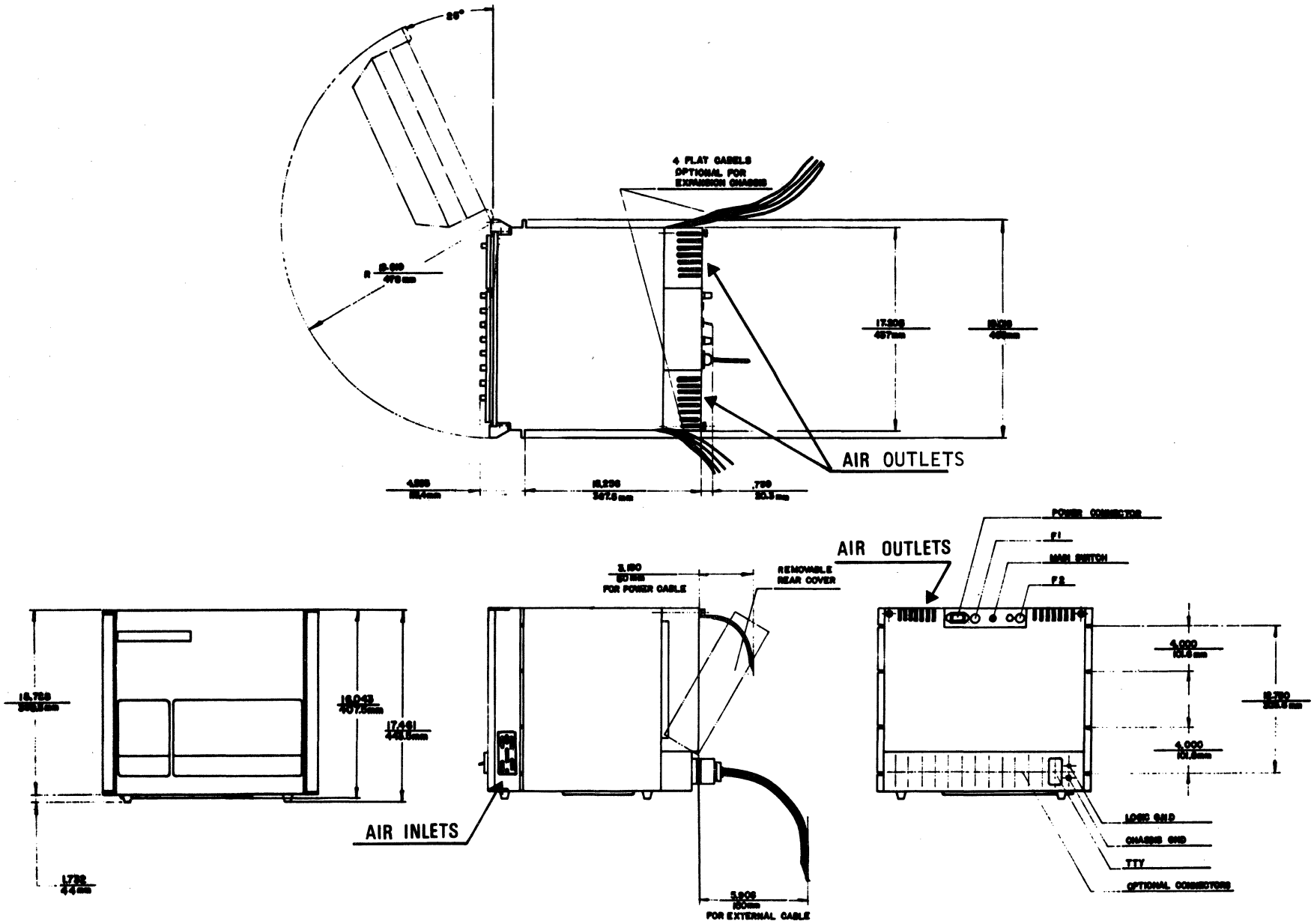
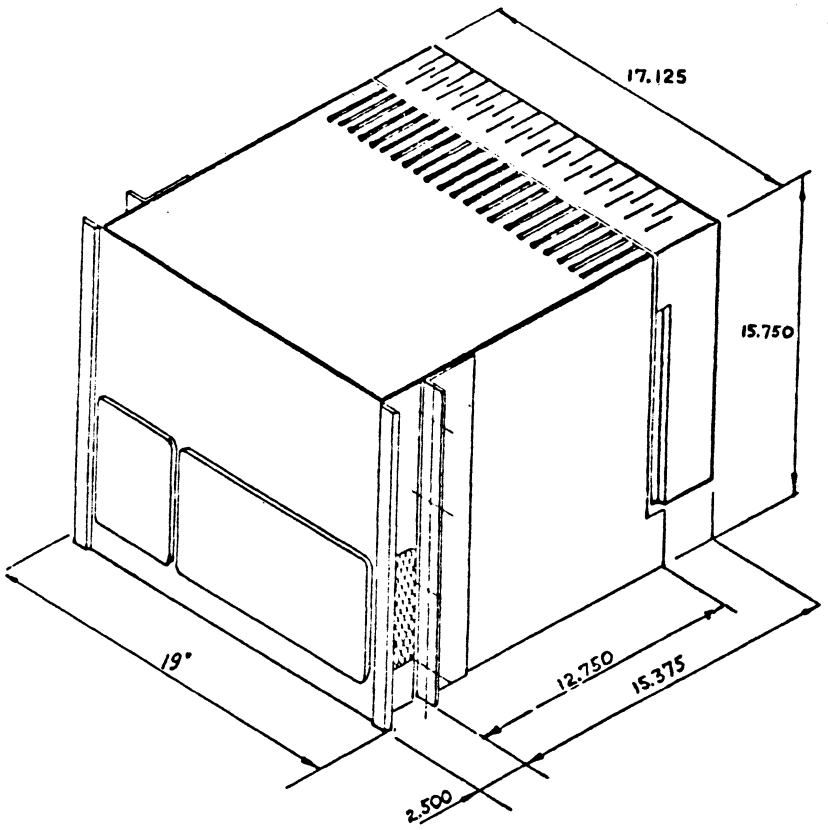


Figure 3-8. General View and Dimensions of Main Enclosure: Type Identifier A

Type
Identifier
A

AB107-A
AB108-A
BT148-A



Type Identifier C

Type Identifier D

AB107-C
AB108-C
BT148-C

AB107-D
AB108-D
BT148-D

* Type identifiers C and D have two fans installed in the base of the enclosure.

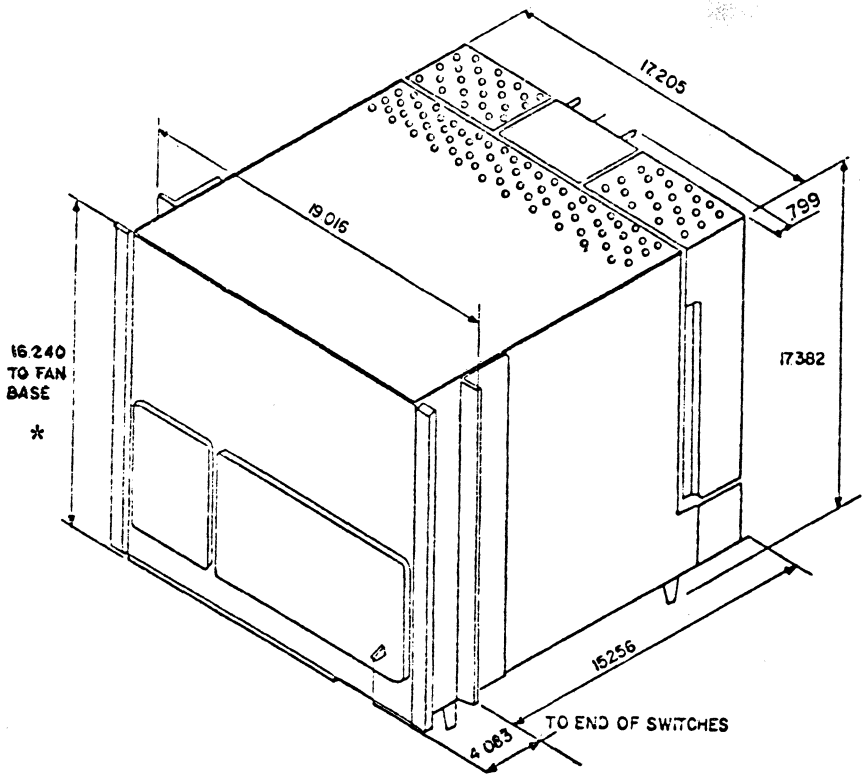


Figure 3-9. External Dimensions of Main Enclosure: Type Identifiers A,C,D

The Programmer's Console (front panel) controls used in the following are described in Section 6 of the 1784 Computer System Reference Manual, publication number 89633400. The console is shown in figure 2-2 of this manual.

1. Open the front cover of the enclosure and pull out all the printed wiring assemblies from their connectors but leave them in their slots.

2. Turn on the AC POWER switch at the top of the rear panel (see figures 3-6 and 3-7). Examine the enclosure to see that all blowers work.

   NOTE: The number of blowers is four or six, depending on the type identifier. Refer to Maintenance Section 6.

   If there is no airflow, or some other fault is detected, switch off the equipment immediately using the emergency shut-down procedure on page 6-3. Location of the air inlets and outlets is shown in figures 3-8 and 3-9.

3. Turn on the DC POWER switch on the operator's console (enclosure front panel - refer to figure 2-2). The indicator above the switch should light.

   WARNING

   If the indicator does not light, or if any other fault is suspected, the equipment must be switched off immediately by turning off the AC POWER switch at the top of the rear panel. See page 6-3 for the emergency shut-down procedure.

4. Check the power supply voltages (see section 6). Check that the value of V_{SS} is correct for the memory modules installed: BA201-A or BA201-B. See table 6-1 for power supply voltages.

5. Switch off the DC POWER switch on the Operator's Console and re-insert the printed wiring assemblies. Make sure that they are well-seated.

6. Repeat step 3 in this procedure.

7. If the Expansion Enclosure, equipment BT148, is part of the installation, repeat steps 1 through 6 for it.

Set up initial conditions by the following procedure:

8. The installation has up to 32K word memory:

   8.1 Press MASTER CLEAR pushbutton.

   8.2 Set Mode switch (65K/32K) to 32K.

   8.3 Set ENTER/SWEEP switch to ENTER.

   8.4 Set INSTRUCTION/CYCLE switch to its central (COMPUTE) position.

   8.5 Set PARITY FAULT STOP switch to its central (off) position.

   8.6 Set SELECTIVE STOP and SELECTIVE SKIP switches to their down (off) positions.

   8.7 Press the GO pushbutton.

   8.8 Press MASTER CLEAR pushbutton.

9. Check all registers by entering data in each one. Note that this check also serves as a lamp test for the indicators associated with the registers and the data input keys.

10. Enter a pattern into memory and correct any problems.

11. Sweep the memory to check for parity error.

NOTE

In steps 8 and 9 refer also to 1784 Computer System Reference Manual, publication 89633400.

INSTALLATION/REMOVAL OF THE BATTERY (Figure 3-10)

The optional power back-up source, rechargeable battery equipment GD611-A is normally packed separately. In operation,the battery is housed in the rear cover of the enclosure. To install the battery follow the outline procedure given below.

Installation of the battery

1. If the battery is new, install the battery, starting from step 4.

   If the battery is not new, or if there is some doubt about its state of charge, go on to the next step.

2. Check the open circuit voltage of the battery.

2.1 Connect a voltmeter/multimeter of 20,000 ohms per volt or more across the terminals of the battery.

2.2 Measure the open-circuit voltage to be 24.2 vdc or more.

2.3 If not, replace the battery by a fully-tested one.
If yes, go on to the next step.

3. Check the full load voltage of the battery.

3.1 Connect two 60 ohm, 5%,10 Watt resistors in parallel across the terminals.

3.2 Connect the voltmeter.

3.3 Measure the full load voltage to be 24.2 vdc or more.

3.4 If not, replace the battery by a fully-tested one.
If yes, disconnect the multimeter and resistors and install the battery, starting from step 4.

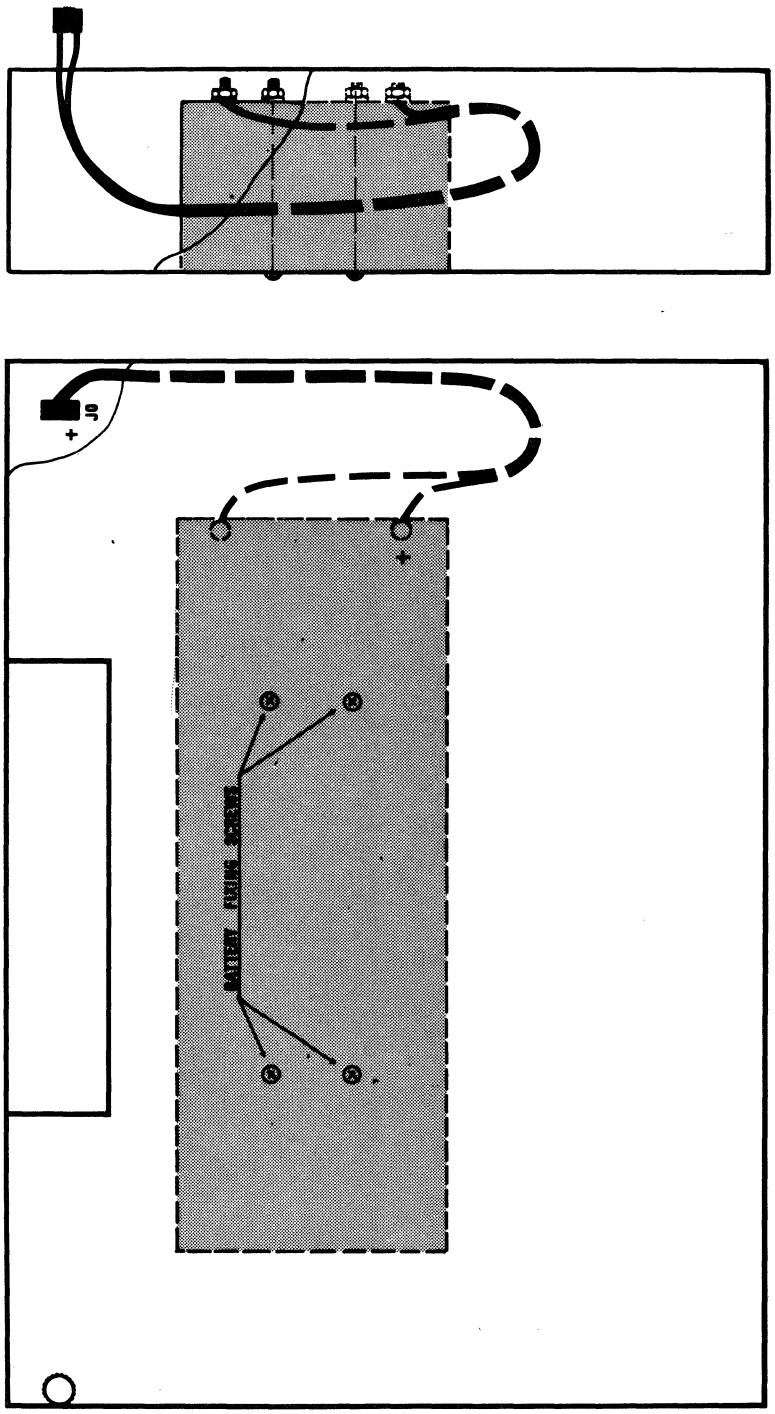


Figure 3-10. Rear Cover With Battery

4. Remove rear cover of the enclosure by undoing the two thumb-screws at the top of the rear cover, tilting the cover back and sliding it out of its slots.

5. Fix the battery to the rear cover (Figure 3-10)using the four screws and corresponding nuts and washers provided.

6. Install the battery cable provided as follows:

6.1 connect the cable shoes under the nuts on the battery terminals, the red lead to the positive (+) terminal

6.2 slide the rear cover (with the battery fixed to it) into its slots and support it by hand

6.3 connect the other end of the cable to connector J0 on the enclosure, inserting the red lead to the lower pin of the connector

6.4 close the rear cover onto the enclosure and tighten the two thumbscrews

7. Check the battery fuse (refer to Figure 3-6).

If the equipment is newly installed or has not been used with a battery before perform also the following steps:

8. Load the memory with a pattern and check the pattern under normal operating conditions. Record the pattern.

9. Turn off the equipment power supply (Power Off Procedure, section 6)

10. After a few minutes turn on the power again (Power On Procedure, Section 6) and check that the pattern in the memory has been retained.

If the pattern has been retained, proceed with normal operation. If the pattern has not been retained recheck the battery (see step 1 above). If battery is in order proceed to memory diagnostics.

Removal of the battery : Do steps 6, 5, 4, in that order.

PROCEDURE TO INSTALL EXTERNAL SHIELDED CABLE ASSEMBLIES (Figure 3-11)

The ground screw to which the external shielded cable is to be attached may or may not have a cable already attached to it.

Ground Screw Without Cable Attached

1. On the interior surface of the rear connector panel, scrape off a 0.5 inch (12.7 mm) diameter circle of paint around each of the three lower holes.
2. Open Installation Kit Part No. 89986600 that contains all the attachment parts needed.
3. Slide the external tooth lock washer onto the screw.
4. Insert the screw and external tooth lock washer into the hole of the rear connector panel.
5. Mount the spring lock washer.
6. Mount the plain washer.
7. Mount one of the two hexagonal nuts.
8. Slide the flat-locking terminal of the cable onto the screw.
9. Mount the other hexagonal nut. Secure the cable into place.

Ground Screw With Cable Attached

1. Remove the securing nut and save it.
2. Slide the flat-locking terminal of the cable onto the screw.

CAUTION

Do not mount more than four external shielded cables onto the same screw.

3. Mount again the nut that was removed in step 1.
   Secure the cable into place, making sure there is proper electrical contact with the cables already attached.

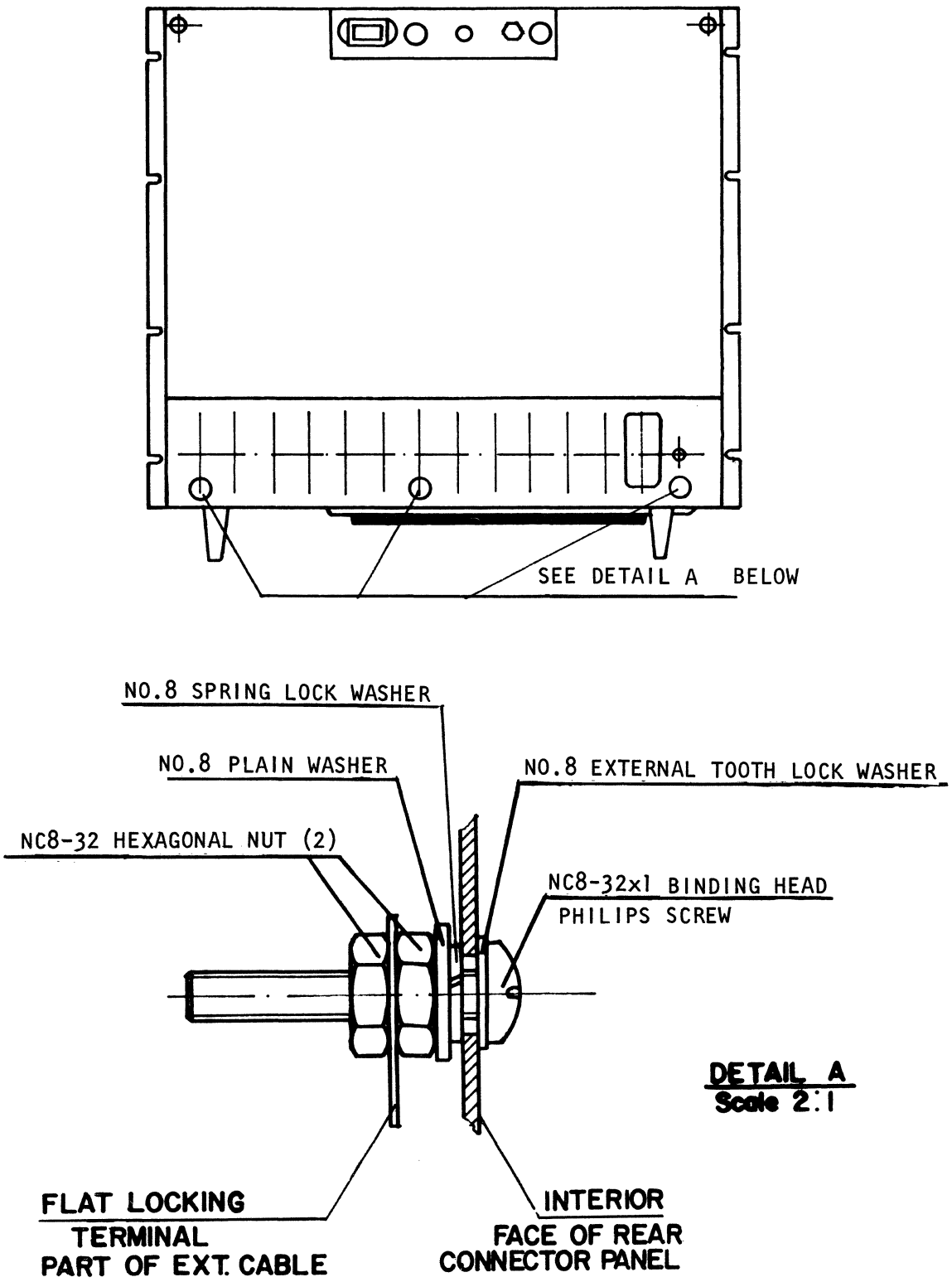


Figure 3-11. Installation Kit Part No. 89986600 For External Shielded Cables

13. Teletypewriter (TTY)

NOTE: In the following refer to the Teletype Corportation instruction manual for the Teletypewriter in the system. Carry out all procedures and checks listed there. In addition, carry out the procedure outlined below.

* Inspect the teletypewriter for superficial damage, loose cables and screws.

* Check the teletypewriter wiring:
  - loop-current must be 20 milliamperes
  - connect for full-duplex operation
  - wiring changes as detailed below.

Models 33 ASR/KSR

Modifications to run full duplex with a 20 ma current loop. The changes are noted on the diagram for the customer interface (TTY 9336WD-B2) on terminal strip BL (x). Also, see Note 9 on 9336WD-A1.

Instructions for conversion:

1. Move the purple wire on BL(X)-8 to BL(X)-9.

2. Move the White-Blue Wire on BL(X)-4 to BL(X)-5.

3. Move the Brown-Yellow wire on BL(X)-3 to BL(X)-5.

4. Ref. diagram 9336WD-B1
   Move wire on AC(R-1) tab 3 to R-1 tab 4. Blue wire.

Facing the rear of the unit, the terminal strip BL is located on the lower left side near the cable entry.

13. Teletypewriter (TTY) Continued

R-1 is located on the left side midway to the front, a large brown resistor with 4 tabs.

Models 35 ASR/KSR

This type of TTY does not have the same jack/connector configuration as the 33 KSR/ASR teletypewriter, so it does not utilize the connector on the TTY external cable assembly. The connector must be cut off and terminal lugs should be installed on the wires.

Remove the terminal strip cover of the terminal strip located in the place normally occupied by the I/O connectors. Remove the shorting brackets from TB 5, 6, 7, and 8, if they exist.

Connect the TTY external cable wires to TB5, 6, 7 and 8. Then replace the terminal strip cover and close the TTY to cover.

35 KSR/ASR Teletypewriter I/O Cable Connections

66-PIN CONTINENTAL CONNECTOR PIN AT CPU END	TB PIN
Pin 47	5
Pin 43	6
Pin 49	7
Pin 45	8

* The teletypewriter normally operates from a power line with a nominal voltage of 110 volts. Check the teletypewriter and the available line voltage. If they match, hook up the power to the teletypewriter by plugging the line cord into the utility outlet.

13. Teletypewriter (TTY) Continued

If the power line voltage is 220 volts a transformer will have to be used. To determine the power rating of the transformer, consult the teletypewriter instruction manual.

* The 33 KSR/ASR TTY's come equipped as either 60 Hz or 50 Hz devices. Both units require single phase 120 vac.

* The 35 MSR/ASR teletypewriters are shipped with a 50 Hz mechanical conversion kit (see Section 10.2). When installed, these TTY's will accept 50 Hz, 120 vac. Install this kit if applicable. The kit contains the necessary instructions to accomplish the change.

* It may be necessary to replace the male connector of the TTY primary power cord to make it compatible with the customer power source.

* Check the teletypewriter operation by performing the following:

  - set power switch to LOCAL ON
  - press a number of characters on the keyboard and check that the printer prints them correctly.
  - press LINE FEED and CARRIAGE RETURN (LF CR) buttons on the keyboard.

* Check the teletypewriter in conjunction with the computer by performing the following:

  - switch off the AC POWER switch on the expansion enclosure and on the computer rear panel.
  - connect the external data cable from the teletypewriter to the main computer enclosure (refer to figure 3-7); check that the internal cable (P14 to slot 20) is correctly seated.

13. Teletypewriter (TTY) Cont'd

- make sure the baud select on the TTY controller is properly installed, (Baud rate 110 is selected with Jumper on TTY Controller).
- Switch on the AC POWER switch on the computer rear panel and the DC POWER switch on the Programmer's Console.
- Set teletypewriter power switch on ON LINE
- press a character a number of times in succession: the teletypewriter should print the character twice (and twice only) showing presence of the TTY Controller board in the com-computer enclosure.
- press the MASTER CLEAR switch on the computer Programmer's Console.
- press again a character on the keyboard a number of times in succession: the teletypewriter should again print the character twice.
- run the applicable diagnostics as detailed in the System Maintenance Monitor (SMM) for the TTY.

14. Conversational Display Terminal (CDT)

* Inspect the Conversational Display Terminal for superficial damage, loose cables and screws.

* The CDT normally operates from a power line with a nominal voltage of 110 volts. Check the CDT and the available line voltage. If they match, hook up the power to the teletypewriter by plugging the line cord into the utility outlet. If the power line voltage is 220 volts a transformer will have to be used. To determine the power rating of the transformer, consult the CDT instruction manual.

14. Conversational Display Terminal (CDT) Cont'd

* The CDT can be utilized as a 50 Hz/60 Hz 120 vac device without any internal changes. It may be necessary to change the connector on the primary power cord before connecting it to the customer power source.

* Check the CDT operation by performing the following:

  - set power switch to ON
  - ensure local switch is in the OFF position.
  - press a number of characters on the keyboard and check that the printer prints them correctly.
  - press clear to see if screen is cleared of all characters.

* Check the CDT in conjunction with the computer by performing the following:

  - switch off the AC power switch on the expansion enclosure and on the computer rear panel.
  - connect the external data cable from the CDT to J14 in the main computer enclosure. Check that the CDT/TTY internal cable (P14 to slot 20), is correctly seated.
  - If the Non-Impact Printer (NIP) is part of the system, install cable assembly P/N 62078801 between the CDT and the NIP. The printer daisy chain output on the NIP must be terminated with terminator assembly P/N 62078900.
  - make sure the baud select on the TTY controller board is properly installed. Baud rates are 110, 300, 1200, and 9600 only. Maximum baud rate for NIP Printer is 300. Use of NIP Printer at baud rate greater than 110 will require software restrictions to prevent lost characters after a carriage return.

14. Conversational Display Terminal (CDT) Cont'd

- Odd or even parity operation of the CDT may be required by specific applications. In that event, changes will have to be made on the TTY controller board.
- To select even parity and seven data bits per character, add a wire between P2-B22 and U53-7. To select odd parity and seven data bits per character, add another wire between P2-B28 and U52-7.
- Install wires, if required, on the component side of the TTY controller board.
- Switch on the AC POWER switch on the computer rear panel and the DC POWER switch on the Programmer's Console.
- set CDT switch to ON.
- Run the applicable diagnostics as detailed in the System Maintenance Monitor (SMM) for the TTY.

15. Install all peripheral controllers according to appropriate Customer Engineering manual. Refer to delivery note/equipment order for list of peripheral controllers and to Figures 3-1,3-2. Make sure that the appropriate internal and external cables are connected (refer to the cable list of the peripheral Customer Engineering manual). The preface to this manual lists the Customer Engineering manuals of the peripheral controllers.

WARNING

Before attempting to insert any controller make sure that the enclosure dc POWER switch is off.

16. Install all interconnecting cables between the main computer enclosure and the expansion enclosure (if part of system).

Conversational Display Terminal (CDT) Continued

17. Make all interrupt connections according to system requirements on the computer main enclosure back plane using the interrupt cable assembly number 89724702. For interrupt pin assignments on the CPU refer to Table 4-5.

18. Make all DSA scanner connections according to system requirements. Refer to AB107/AB108 Computer Input/Output Specification Manual, publication number 89673100 as well as the CE manuals for specific controllers. The preface to this manual has a complete list.

19. Run diagnostics (SMM 17).

SECTION 4

THEORY OF OPERATION

THEORY OF OPERATION

INTRODUCTION

This section presents general and detailed functional descriptions of the equipment, using aids such as overall and detailed block diagrams and timing diagrams. Descriptions are keyed to the detailed logic diagrams in the Diagram Section (Section 5) and afford a basis to understand the detailed description of the specific circuit in that section.

NOTE

It is assumed that the reader is familiar with Control Data equipment and with the programming characteristics of the Computer as described in the 1784 Computer System, Reference Manual, Publication No.89633400.

BASIC COMPUTER

The AB107/AB108 with the memory and other supporting equipment is a stored program parallel mode digital computer. The computer word contains 18 bits; the 16 least significant bits (bits 00 through 15) contain data and instructions, bit 16 is the parity bit, bit 17 is the program protect bit.

The simplified block diagram of the computer system is given in Figure 4-1. It shows the principal functional units of the computer with an indication of their equipment numbers. The interconnection between the units is shown both within an equipment and between the main computer enclosure (equipment AB107 or AB108) and the expansion enclosure (BT148). The main computer equipment houses up to eight memory modules (equipment BA201-A/B). It also houses the optional Memory Hold Battery (equipment GD611-A) and provides slots and wiring for peripheral equipment controllers on the A/Q and Direct Storage Access (DSA) input/output channels. The expansion enclosure (equipment BT148) similarly houses the whole of the memory expansion system and the Memory Hold Battery and provides slots and wiring for peripheral equipment controllers on the two input/output channels. The equipment is listed and described in Section 1 of this manual; detailed circuit, logic and interconnection diagrams are given in Section 5. Functional block diagrams are given in this section.

Most of the circuitry of the computer is accommodated on 50-PAK printed wiring boards. The power supply forms a separate component unit within the computer enclosure. Table 4-1 lists the units of the basic computer, their slot allocation within the computer enclosure is shown in Figure 3-1.

TABLE 4-1. BASIC COMPUTER FUNCTIONAL UNITS

Subsystem	Unit designation	Slot	Assembly/Mounting
CPU	Timing	23	single P.W.A.
	Decoder	24	single P.W.A.
	Arithmetic and Logic Unit (ALU)	25,26	two identical P.W.A.'s
	Console Interface	21	single P.W.A.
	I/O Interface	22	single P.W.A.
	Teletypewriter Controller (TTY)	20	single P.W.A.
	Programmer's Console	-	enclosure front panel
Memory System	Memory Module (900 nsec)BA201-B (600 nsec)BA201-A	29÷36	one to eight P.W.A.'s (BA201-A or BA201-B)
	Memory Address Assy } Memory	28	single P.W.A.
	Memory Control Assy } Controller	27	single P.W.A.
Power Supply	Power Supply Unit	-	Unit mounted on front door of enclosure
Battery (optional)	Equipment GD611-A	-	Mounted on rear cover of enclosure

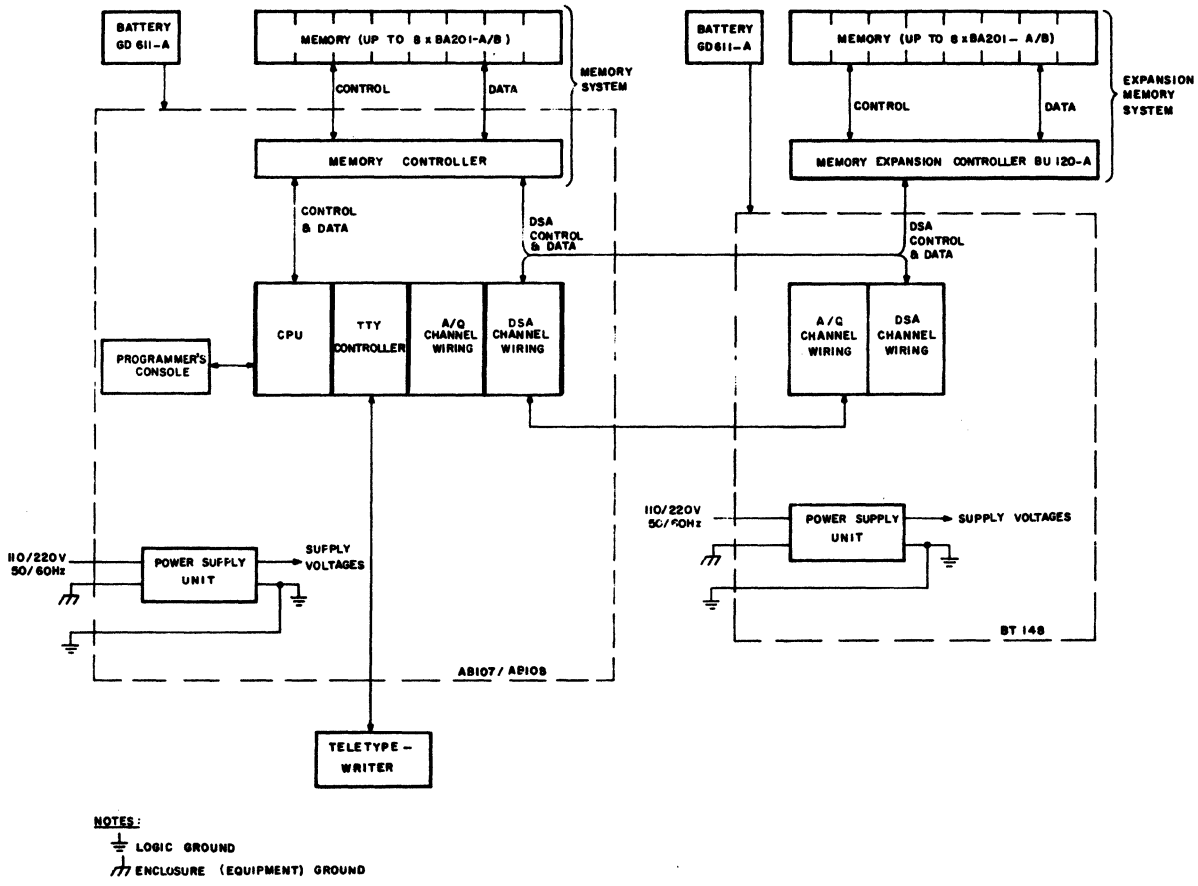


FIGURE 4-1 COMPUTER SYSTEM SIMPLIFIED BLOCK DIAGRAM

Figure 4-1. Computer System Simplified Block Diagram

THE CENTRAL PROCESSING UNIT (CPU)

DATA PATH

The block diagram of Figure 4-2(a) shows the main circuits in the arithmetic and control portion of the 1784 computer. The input/output (I/O) and memory interfaces are indicated.

As shown, the CPU consists of the ALU/Shifter network, control circuits and registers. In general, the registers contain operators and data for some period of time. When the register contents require an arithmetic, logical, or transfer operation, they are transmitted through the ALU/Shifter network. The ALU/Shifter network combines these quantities in a logical or arithmetic operation, operates on them independently as in a shift, or simply serves as a path to transfer the contents of one register to another. Thus the ALU/Shifter serves as the main path for all arithmetic, logical or inter-register transfer operations.

The AB107/AB108 instruction Execution Charts (publication number 89723800) give details of the contents of the computer circuits at the various stages of execution of the program commands.

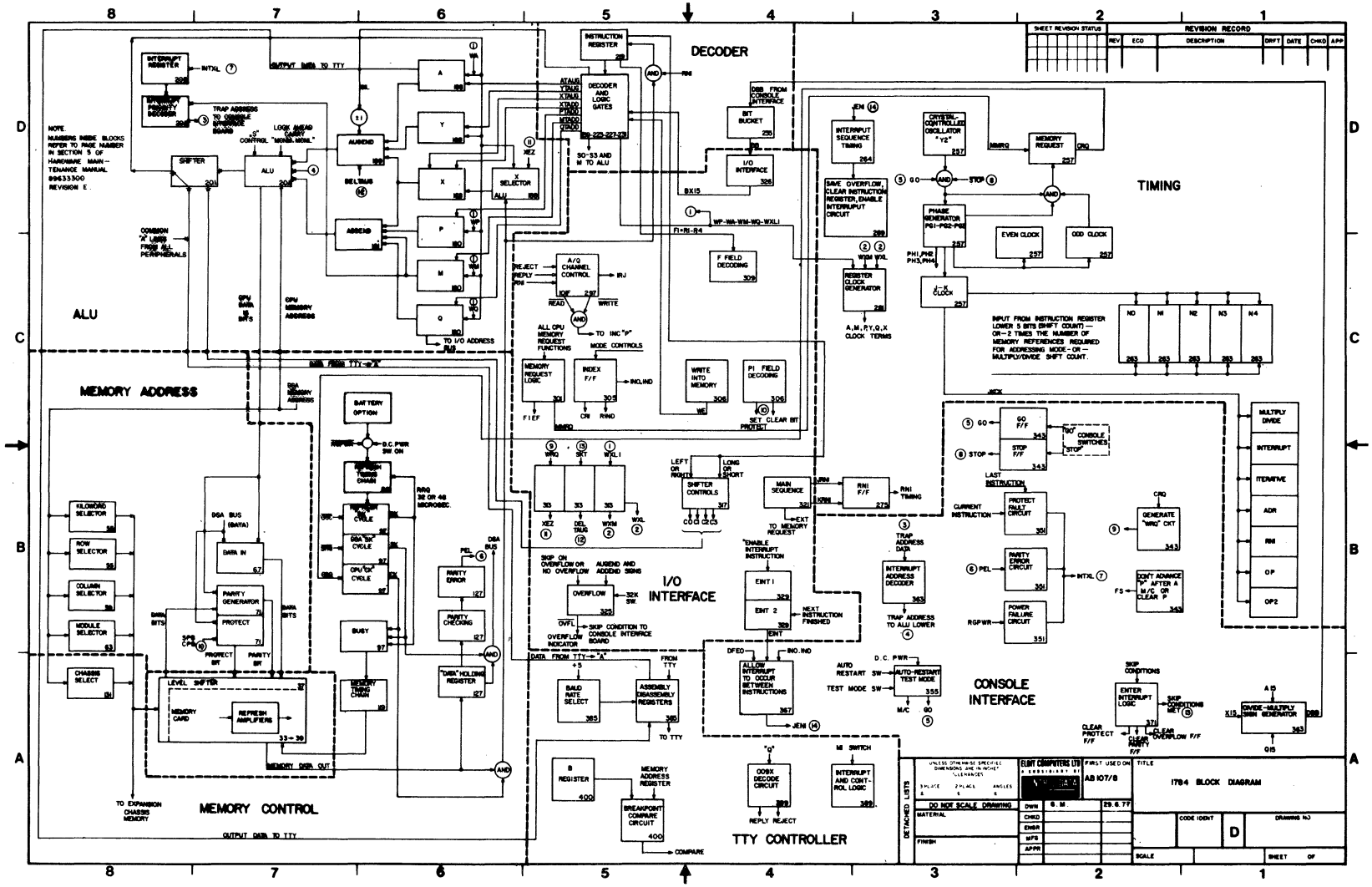
MAIN REGISTERS

X Register

The 16 bit data (X) register temporarily stores all data words read from the memory by the CPU. This register holds one of the parameters in most arithmetic operations.

Y Register

The 16 bit address (Y) register temporarily stores incomplete addresses during address modification (indirect addressing). It stores the final effective address when modification is complete. It is also used to store temporarily a data word whose protect bit is being modified during set/clear protect bit instructions; or one whose data content (16 bits) is increased by +1 during Replace-Add-One instruction.



Errata: 1. Zone D-7: input to ALU block should be "S" CONTROL (not „S" CONTROL)
2. Zone B-4: input should be "ENABLE INTERRUPT" INSTRUCTION (missing quotation marks).
3. Zone D-3: INTERRPUT SEQUENCE TIMING should be INTERRUPT SEQUENCE TIMING (spelling).
4. Zone D-3: in block of SAVE OVERFLOW etc, INTERRUPUT should be INTERRUPT (spelling).

Figure 4-2. CPU Block Diagram

A Register

This 16 bit register is the principal arithmetic register in most arithmetic and logical operations. The sixteenth bit in the register is the sign bit. The register is also used as a temporary store for data received or transmitted on the A/Q channel.

Q Register

The 16 bit Q register serves as the auxiliary register in most arithmetic and logical operations. It is also used to hold address codes of peripheral devices operating on the A/Q channel; it also serves as index register No. 1.

P Register

The program address (P) register contains 15 bits in the 32K mode and 16 bits in the 65K mode (operation with memory expansion). It holds the program address of the instruction currently being executed. In the later stages of execution of most instructions the P register is advanced by adding +1 through adder/shifter network for referencing the next instruction. The P register may be decremented by adding -1 during some interrupt sequences.

M Register

The 16 bit mask (M) register stores the interrupt mask bits. Each bit in the mask register corresponds to a particular interrupt line. For the computer to recognize an interrupt when it occurs, the corresponding bit of the mask register must be active (high).

B Register

The 16 bit breakpoint (B) register holds data for address comparison during breakpoint mode of operation. This register can be accessed only manually through the Programmer's Console front panel controls.

Instruction Register

The 16 bit instruction register stores those words read from the memory which are to be treated as instructions. These bits, when decoded, direct the execution of the instructions.

I Register

Storage location $00FF_{16}$ serves as index register No. 2 for indirect addressing; index register No. 1 is the Q register.

Addend/Augend Gates

These gates serve as the input gate control for the ALU/Shifter. In most arithmetic, logical and register transfer operations one input is selected by the addend gates and one by the augend gates.

The gates can select signals as follows:

Gate	can select
addend	- output of X, P, M, Q registers
augend	- output of X, Y, A registers - lower 4 bits of X register (other bits equal 0) - lower 8 bits of X register (other bits sign-extended) - lower 8 bits of X register (other bits equal 0) - constants ±1 and ±0

The constant +1 is used to increment the P register at the end of most instructions.

The constant -1 is used during enter interrupt sequence to decrement the P register.

The constants +0 and -0 are used to sign-extend the Δ field of the instruction register.

The lower four bits of the X register are used during skip instructions.

ALU/Shifter

The ALU/shifter is used for the following operations:

- arithmetic and logical operations on the contents of registers
- transfer of A/Q channel input data, Programmer's Console input data and the Interrupt Trap Address into the CPU data path
- calculation of memory address

It also serves as the transfer path for all interregister transfer operations.

CONTROL AND TIMING SECTION

This section generates the basic timing and control signals for the computer. Figure 4-2 (b) gives its block diagram.

Programmer's Console

The equipment front panel serves as the programmer's console: it carries the switches and indicator lights which enable the operator to control and monitor the computer manually.

The controls and indicators are described in the 1784 Computer System Reference Manual, publication no. 89633400. Their layout is shown in Figure 2-2 of this manual. The circuitry associated with the programmer's console consist of three groups of circuits:

* register selectors
* data bit entry circuit
* control switches and indicators

These circuits are described in detail in Section 5 of this manual. They interface with the computer control circuits through the console interface.

Clock

The oscillator and phase generator together form the clock. The oscillator generates crystal controlled symmetrical clock pulses. Different crystals are used to produce the frequencies needed for the two versions of the computer:

Equipment	Cycle time	Oscillator frequency	Phase Generator Repetition Rate
AB107	900 nsec	12.222 MHz	81.8 nsec
AB108	600 nsec	18.333 MHz	54.5 nsec

The phase generator converts the oscillator signal to pulse trains on five clock lines (PH1 through PH5). The timing diagram is given in Section 5 for the Timing unit. The repetition rate for the pulses is given in the table above. A CPU cycle consists of a series of five pulses, one each on the phase generator output lines.

Main Sequence Control and Even/Odd Cycles

The sequence control circuit controls the mode of operation for the execution of a given instruction. There are four modes of operation controlled by four state flip-flops:

- Read Next Instruction (RNI)
- Address (ADR)
- Operand (ØP)
- Operand 2 (ØP2)

In addition every CPU cycle is defined as either an even or an odd cycle. The even and odd flip-flops determine the state of the machine. Usually even and odd cycles will alternate so that one flip-flop will be set and the other reset on the first cycle, and both flip-flops will change state on each following cycle. In some cases the odd state remains for two successive cycles. In such a condition a third flip-flop, called ØDD2 will be set during the second odd cycle. The ØDD2 flip-flop is set by the signal EXT from the I/O interface board and resets itself after one cycle.

The RNI state is active at the beginning of each instruction during both the EVEN, and the ØDD CPU cycle. Some interregister instructions and skip instructions are completed during RNI so that the RNI state remains active during the whole instruction.

In memory reference instructions the RNI state is usually followed by the Operand 1 or Operand 2 (ØP, ØP2) states. These are also used in register reference instructions.

The ADR state is active following RNI in memory reference instructions while the effective address is being calculated. The ADR state lasts from 2 to 6 CPU cycles if there is no multi-level indirect addressing (65K mode). Otherwise it remains high until addressing is completed (32K mode). The ADR state is followed by ØP or ØP2 except in jump instructions.

The entire effective address can be calculated during the RNI·ØDD cycle and the ADR state is not needed. This is referred to as SHort ADDRessing (SHADR). Double addressing is explained in the part of Section 5 describing the ALU circuits.

The other control signals and timing diagrams are given in Section 5 facing the Timing circuits (sheets 2, 5).

Counter

The binary 5-bit count-down counter is used in three operations:

* shift: it counts the number of times a word is to be shifted (shifting distance)
* multiply/divide: it counts the number of iterations necessary to complete the operation
* address: it controls the execution of address calculations

MEMORY SYSTEM

INTRODUCTION

The AB107/AB108 equipment contains the Memory Controller of the memory system. The Memory Controller together with the Memory Modules, equipment BA201-A/B, constitutes the main computer memory system. Up to eight memory modules, equipment BA201-A/B may be accommodated in the main computer enclosure. Each memory module carries 4096 (4K) 18-bit words.

The Expansion Enclosure, equipment BT148, can house the memory expansion system consisting of the Memory Expansion Controller, equipment BU120-A and up to eight memory modules, equipment BA201-A/B.

The memory system housed in the main computer enclosure together with the memory expansion system form the computer memory system having up to 16 memory modules and thus up to 65,536 (65K) 18-bit words.

The memory system will be described in the following paragraphs. The description falls in two parts: the control and access circuits (Memory Control System) are described briefly, followed by a description of the Memory Module, equipment BA201-A/B and the memory unit it is based on. As the AB107/AB108 uses a semiconductor memory, the theory of operation of the memory module is explained in greater detail than that of other circuits. A detailed circuit description of the control circuits is given in Section 5. The memory system is accessed from the CPU (A/Q channel) or from peripheral devices through the Direct Storage Access (DSA) channel. Refer to the paragraphs on input/output in this section.

MEMORY CONTROL SYSTEM

The memory control system is made up of two printed circuit wiring assemblies: the Memory Address and the Memory Control.

Figure 4-3 is a block diagram showing the memory address system and data flow.

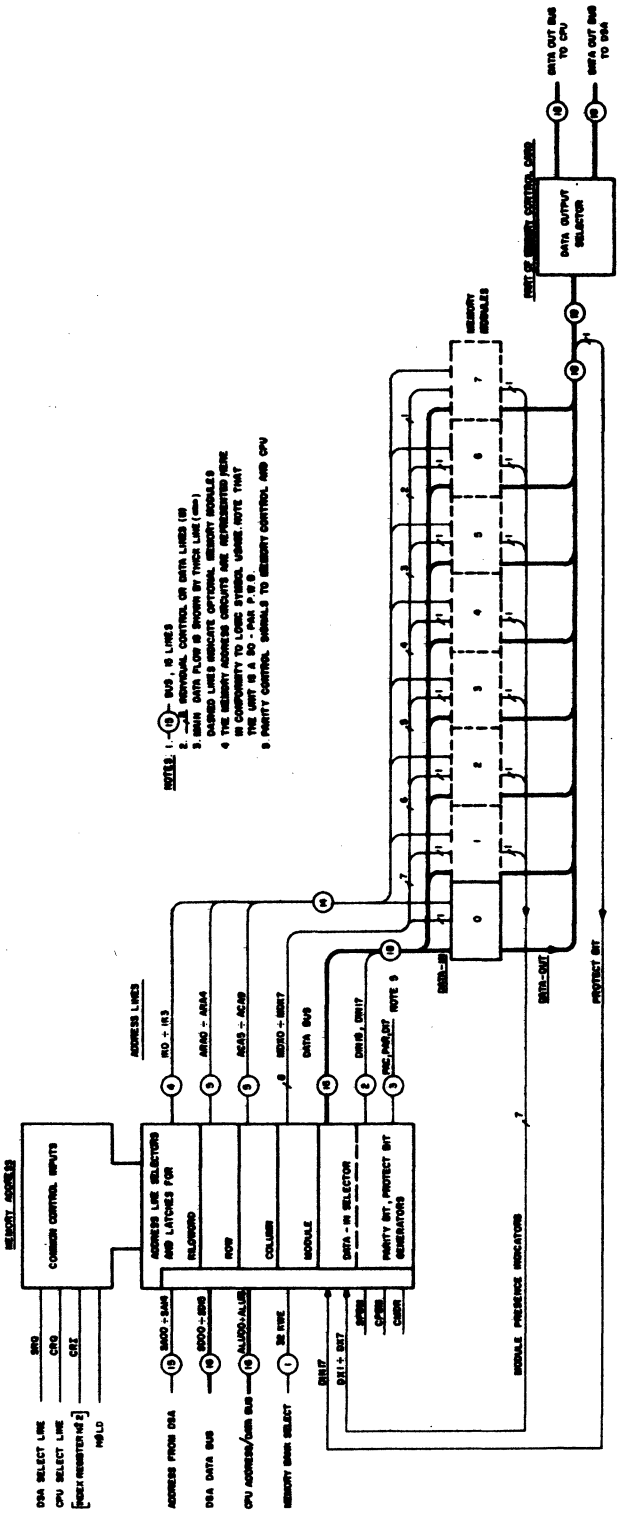


Figure 4-3. Memory Address System and Data Flow

All the memory locations are defined and accessed through the memory address assembly in the following steps:

Step	Selection of-	Defines
1.	Memory bank	- main memory/expansion memory
2.	Memory module	- any one of installed modules (up to eight in main enclosure, up to eight in expansion enclosure)
3.	Kiloword	-- one of four kilowords on selected memory module
4.	Row and column	- word location within the kiloword (bit within the memory unit)

In addition to accessing operations the memory address circuits define the origin of memory access. The following table defines the different memory access cycles:

	Designation	Data flow to/from
1.	Refresh cycle	Internal to memory system
2.	DSA cycle	Direct Storage Access channel (DSA)
3.	CPU cycle	Central Processing Unit

Data input (16 bits) to the memory is through the memory address circuits, which also generate the parity and protect bits, that make up the 18-bit computer word.

Data output is through the memory control circuits to either the CPU or the DSA channel. The control circuits also produce the timing and control signal for the memory system, under command of the CPU and synchronously with the CPU clock.

PRINCIPLES OF THE DYNAMIC SEMICONDUCTOR MEMORY CHIP

Introduction

The memory module (equipment BA201-A/B) of the AB107/AB108 Computer uses dynamic 1024 bit ("one kilobit") random access memory units, built on semiconductor chips using silicon gate MOS technology. They are Large Scale Integrated (LSI) networks, and perform several system functions on the same chip.

Device Operation

The memory unit is a 1024-bit, fully decoded read-write Random Access Memory (RAM). Each bit of information is held in capacitive cells as a stored charge. Because of charge leakage, each bit must be regularly refreshed (recharged). The memory is organized in a matrix of 32 rows by 32 cells. The row and column address select one unique bit from the 1024 storage bits on the chip. Each time a bit is read from or written into a memory cell, all 32 bits of its particular row address are automatically refreshed.

The circuit of each memory cell is shown in Figure 4-4. An array of 1024 of these are mounted in an 18 lead dual in-line package. Figure 4-5(a) shows the block diagram of the circuit package, together with pin connections. A more detailed logic diagram is shown in Figure 4-5(b). The following paragraphs describe the operation of the memory cell and the integrated circuit package in greater detail.

The Memory Cell

The dynamic MOS memory cell circuit is shown in Figure 4-4.

NOTE

"High" and "Low" refer to signal level change with respect to the MOS substrate.

Data is stored as charge on the parasitic capacitance C_S associated with the gate of Q2 and the junction of Q_1 connected to it. Data may be written into this capacitance via the transmission gate formed by transistor Q_1. The data to be written is placed on the WDATA line and WSEL is activated (made high). To read from the cell, the RDATA line with its associated capacitance (or amplifier input) is initially charged high through the external gate by activating the P (Precharge) signal. To complete the reading operation the RSEL line is activated and the RDATA line is recharged only if the capacitor C_S is charged high; the RDATA line remains high only if C_S contains a low. Thus after the reading operation the RDATA line carries the logical complement of the cell data.

Although the read-out operation from the cell is non-destructive, the leakage associated with the junction of Q_1 eventually may result in the loss of the charge stored in C_S. To maintain the data stored in the cell, it is periodically refreshed through feedback of the cell content to the WDATA line during every memory cycle. This is accomplished by reading the contents of the cell onto the read RDATA line, inverting the resulting signal in the refresh amplifier and applying it to the WDATA line, and writing it back into the cell by activating the WSEL line. For the RAM of equipment BA201-A regeneration has to take place every 2 milliseconds, (1 millisecond in equipment BA201-B). During normal operation of the computer refresh cycles are generated automatically, interleaved with CPU and DSA access cycles. Refresh cycles take priority. Special refresh cycles are generated when no access cycles occur.

The dynamic cells are laid out in a two dimensional array on the chip. One entire row of cells is refreshed (or accessed) at one time, one refresh amplifier being provided for each column of cells in the array. To refresh the entire memory, each row of cells must be individually refreshed.

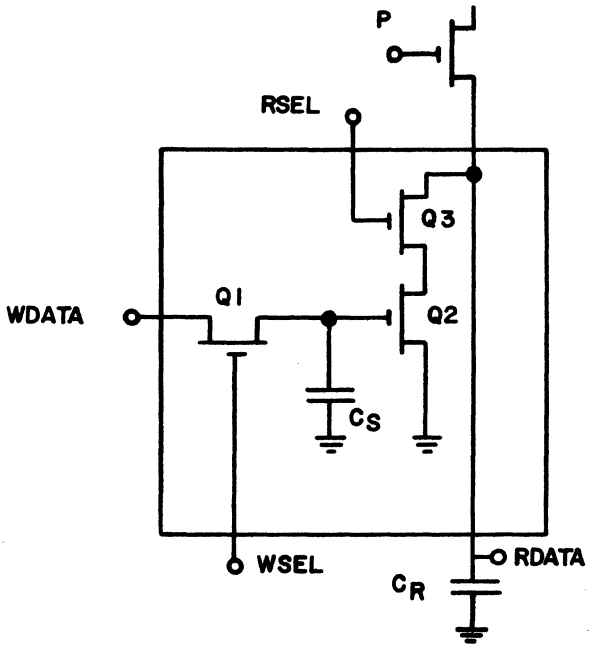


Figure 4-4. The Memory Cell

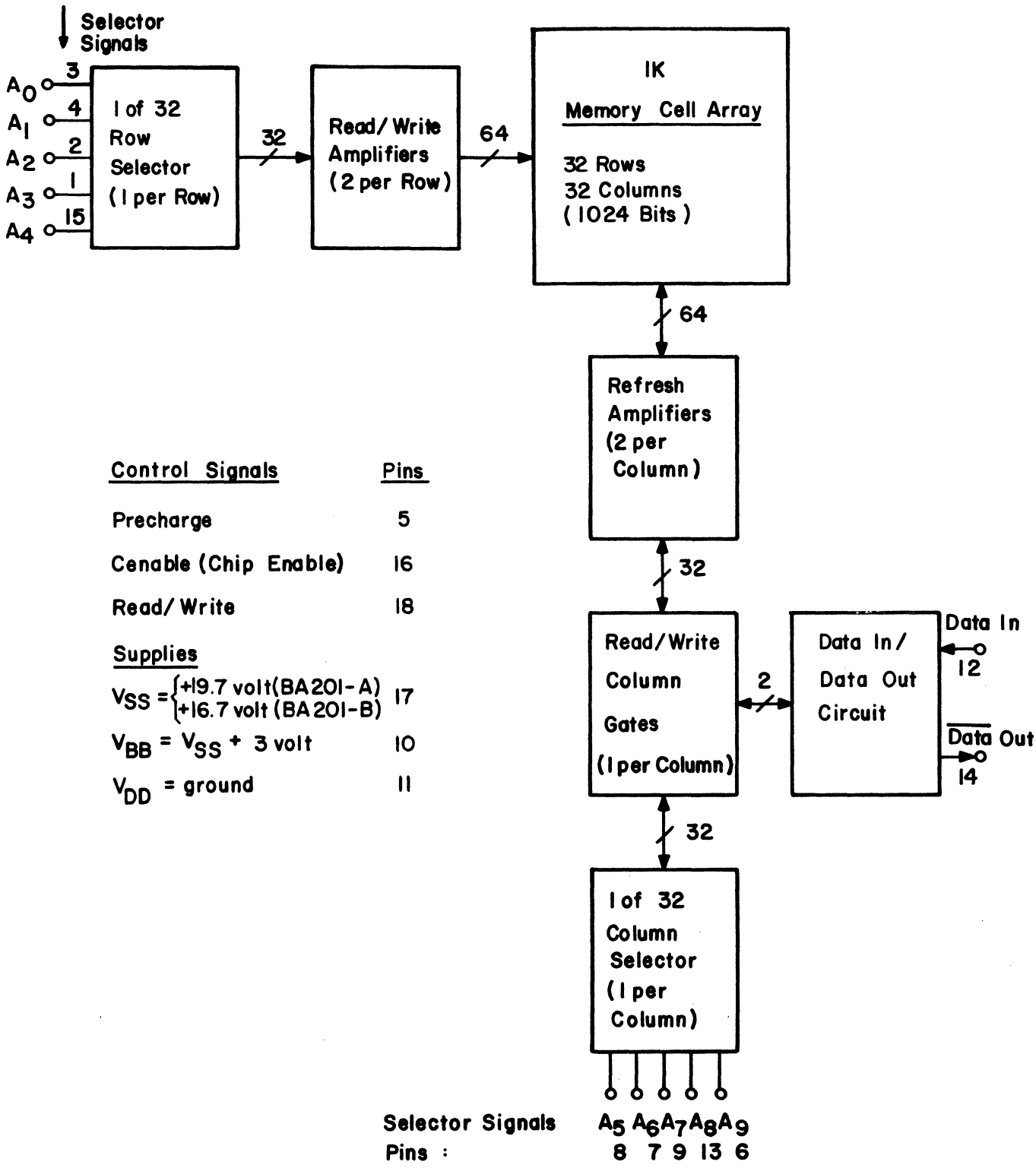
Organization

General block diagrams of the memory unit are shown in Figures 4-5 (a) to (d). The memory is organized in a matrix of 32 rows by 32 cells each. Five row address lines, A0 through A4, are decoded to select one row of cells. When accessed, the contents of the selected row are transferred to a row of 32 refresh amplifiers. In the course of a memory cycle, whether read or write, the data is regenerated and written back into the selected row of cells. Address bits A5 through A9 are decoded to select one refresh amplifier for communication with the data input and output terminals, through the Read/Write Column Gates. Activation of the write-clock (Read/Write signal) effectively disconnects the refresh amplifier and so causes new data to be written into the cell. Data output is sensed as a current through the common data output gate ($\overline{\text{DATA}}$ out gives zero current output for DATA high, about 0.9 milliamperes for DATA low).

Timing

Figure 4-6 shows the basic timing of the chip memory cycle.

The cycle timing is established by the three clock signals: Precharge, Cenable (Chip Enable), and Write. Initially (prior to execution of a memory cycle) all clocks are at their high state, at a voltage approximately equal to the supply voltage, V_{SS}. Access begins t_{AC} before the negative transition of Cenable. During this period Precharge is active, and the address becomes stable in both row and column decoders. After the Cenable transition the contents of the 32 cells along the selected row are written into the 32 on-chip refresh amplifiers. At the positive transition of the Precharge the contents of the refresh amplifiers are written back into their respective columns and the output appears t_{PO} later. A delay of t_{PW} after the positive edge of the Precharge, new data on the data input line may be written into the selected cell using a read/write pulse (minimum duration t_{WP}).



Control Signals	Pins
Precharge	5
Cenable (Chip Enable)	16
Read/Write	18
Supplies	
V_{SS} = {+19.7 volt (BA201-A) / +16.7 volt (BA201-B)	17
$V_{BB} = V_{SS} + 3$ volt	10
V_{DD} = ground	11

Figure 4-5. Memory Unit.
(a) Block Diagram and External Connections.

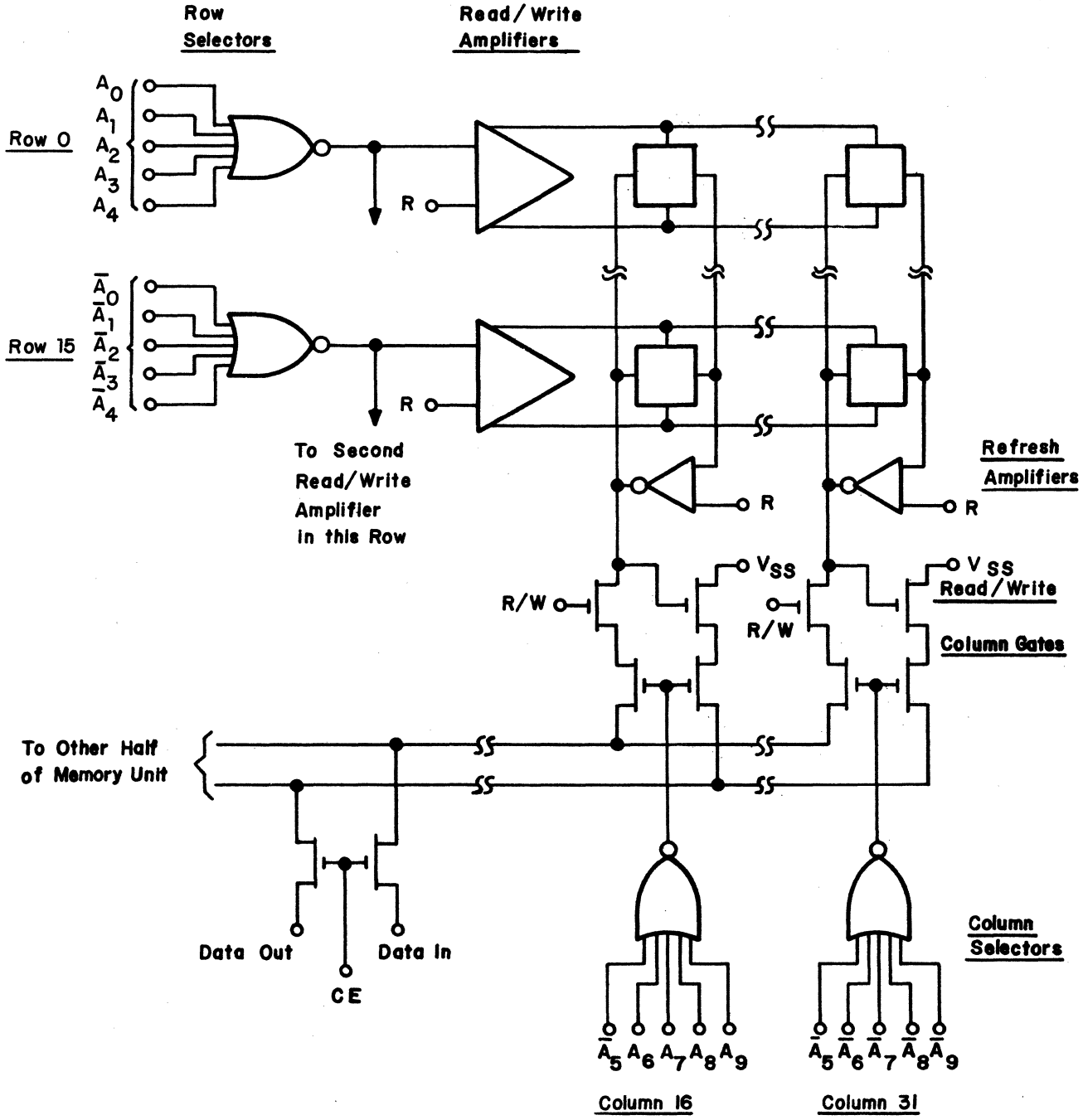
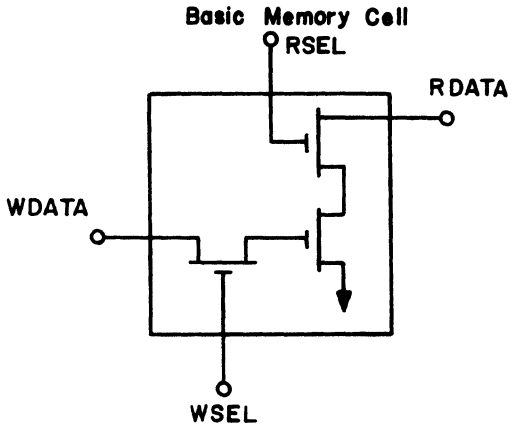
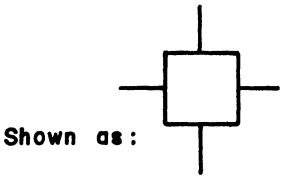
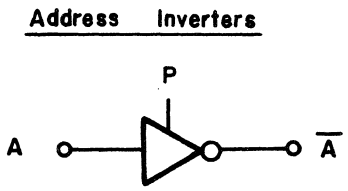


Figure 4-5. Memory Unit.
(b) Detailed Block Diagram.







A: A_0 through A_9

A	P	$\overline{A}$
L	L	H
L	H	H
H	L	L
H	H	value of previous state

H: High
L: Low

Figure 4-5. Memory Unit.
(c) Circuit Details.

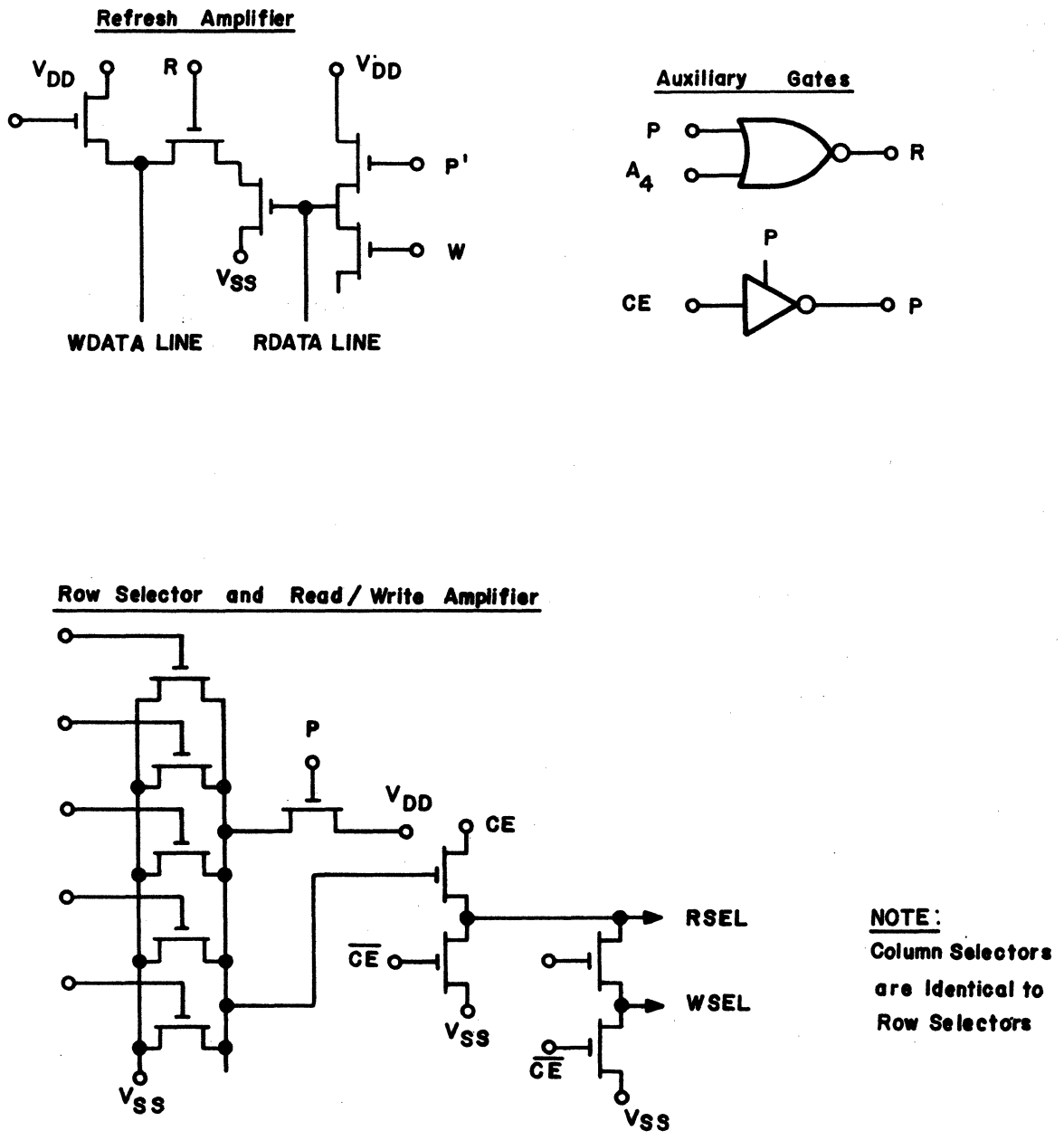


Figure 4-5. Memory Unit.
(d) Circuit Details.

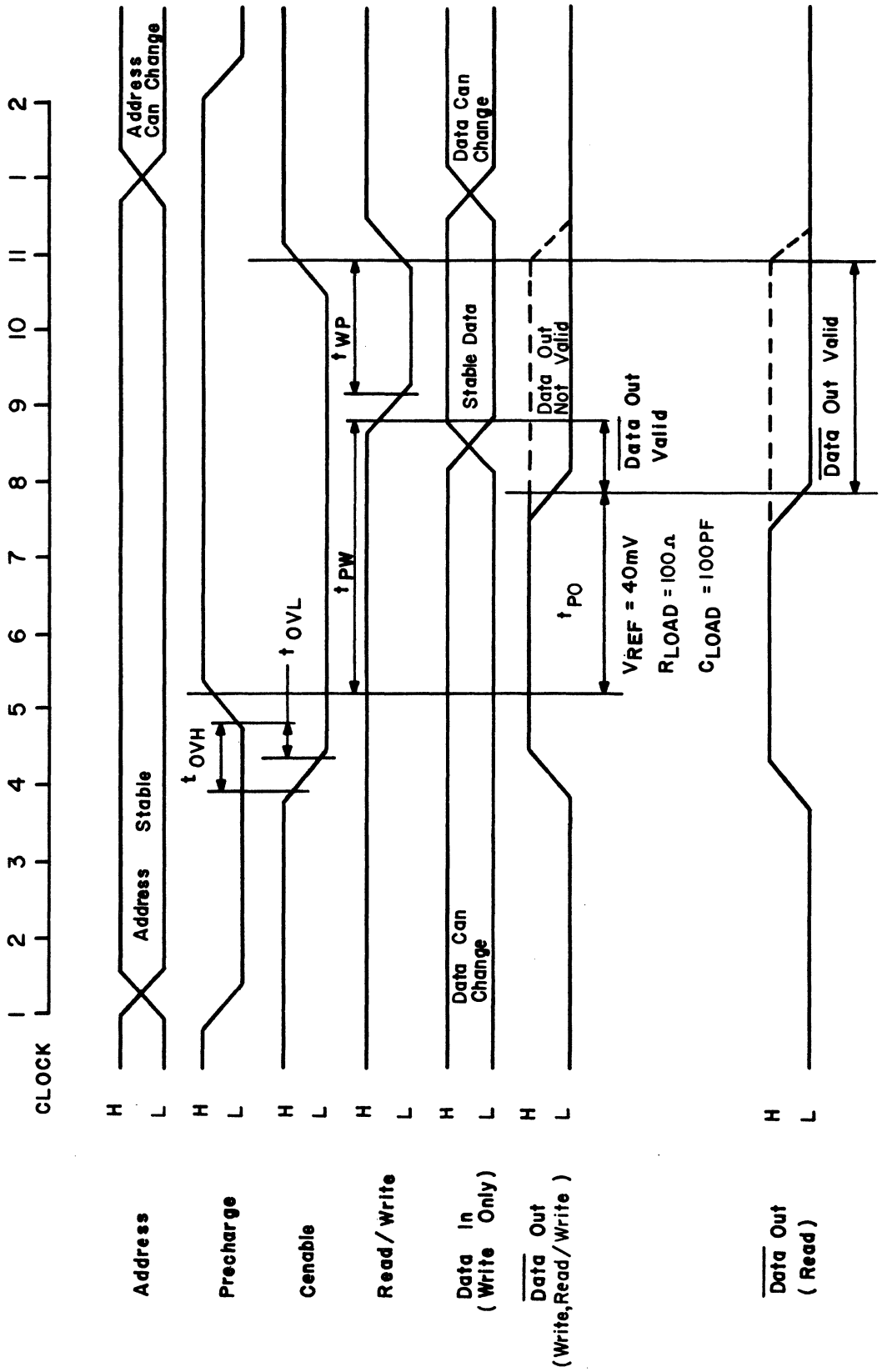


Figure 4-6. Memory Timing
(a) CPU and DSA Cycles.

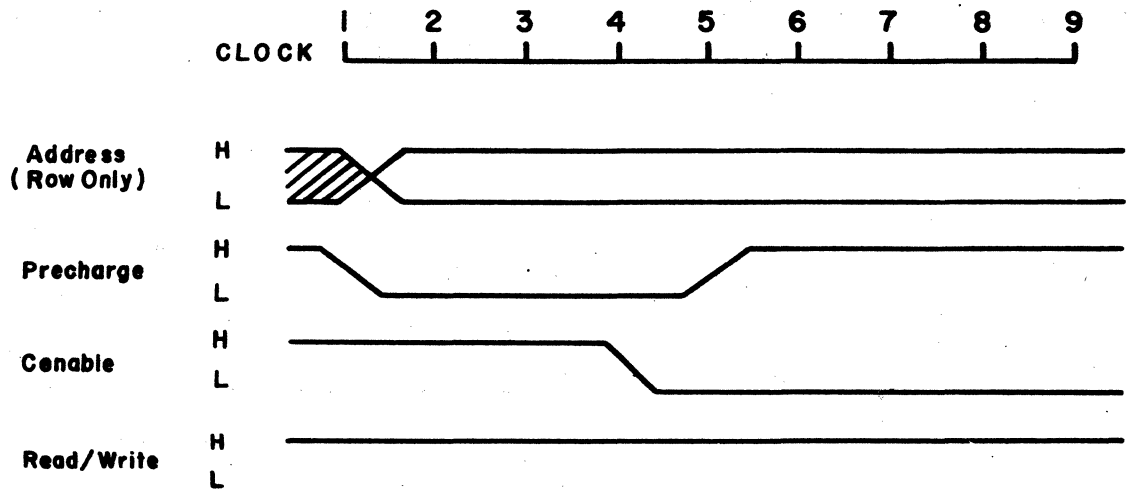


Figure 4-6. Memory Timing.
(b) Refresh Cycles

The memory unit described here has two versions differing in their basic cycle times:

* the BA201-B module allows a computer cycle time of 900 nanoseconds in the AB107 equipment
* the BA201-A module allows a computer cycle time of 600 nanoseconds in the AB108 equipment

One type of memory module (BA201-A or BA201-B) may be accommodated in the enclosures (computer enclosure and expansion enclosure, equipment BT148) at any one time. The memory controller and memory expansion controller are suitable for both types and only the enclosure supply voltage (V_{SS}) has to be changed. This is done at the time of installation of the first memory module in the enclosure.

The basic timing specifications of the memory units are given in Table 4-2.

TABLE 4-2. BASIC TIMING SPECIFICATIONS OF THE MEMORY UNITS

Symbol	Period	Chip used in BA201-B Module		Chip used in BA201-A Module		UNIT
		MIN	MAX	MIN	MAX	
t_{REF}	Time between refresh		2		1	ms
t_{AC}	Address to Cenable setup time	115		30		nsec
t_{OVL}	Precharge & Cenable overlap, low	25		-10		nsec
t_{OVH}	Precharge & Cenable overlap, high		140		85	nsec
t_{PW}	Precharge to Read/Write delay	165	500	115	500	nsec
t_{WP}	Read/Write pulse width	50		40		nsec
t_{PO}	End of Precharge to output delay		120		75	nsec
t_{ACC1}	Address to Output Access	300		135		nsec
t_{ACC2}	Precharge to Output Access	310		165		nsec

DETAILED OPERATION OF THE MEMORY UNIT

To begin a cycle, Precharge is brought low, to approximately V_{DD} potential. This operation activates the row and column decoders, and also charges all read and write data lines negatively, i.e., to the equivalent of a logic "high" state for the P-channel MOS. (In the discussion which follows, clocks, etc. are considered "on" at V_{DD} level, and "off" at V_{SS} level. "High" and "Low" refer to the change with respect to the MOS substrate.)

The decoder circuitry is somewhat faster than the line charging circuitry, so addresses need not be stable until somewhat after Precharge is applied. Address data may be provided before Precharge is turned on.

After Precharge and address data have been present long enough for the data lines to charge and the row and column decoders to stabilize (time t_{AC} after Precharge is low) the Cenable clock is turned on - i.e., dropped to its low state. At this time, the desired read-select line is activated and the read-data line charging circuits are disabled. This initiates the writing of the contents of the 32 cells along the selected row into the 32 on-chip refresh amplifiers, one amplifier for each column in the array. The data lines begin to discharge selectively, with the signals on them approaching values corresponding to the complements of the data stored in the selected row of cells.

As the read-data lines selectively discharge, the Precharge signal is turned off, i.e., raised high to V_{SS}. Following this the contents of the refresh amplifiers are written back into their respective columns; and after the period t_{PO} the output appears. This is accomplished by the removal of the charging signal on the write-data lines, and closing a path to selectively discharge these lines. The cell contents are restored by activating the write-select line corresponding to the selected read-select line. The signal level on the write-data line is a function of the overlap time between Precharge

and Cenable. If this overlap is too short, the read-data lines will not have discharged sufficiently when the discharge path from the refresh amplifiers to the write-data lines is closed. As a result, high (negative) levels written into the cells may be reduced.

If, however, the overlap time is excessive, weak lows within the cells may result in some discharge of the read lines before closure of the write-back path. Thus cells with weak lows have higher levels (even weaker lows) written back into them, eventually resulting in lows changing to highs. This problem is somewhat aggravated by the small but unavoidable capacitive coupling between the data and select lines and the cell storage capacitor. Provision is made for controlling the overlap time in the Memory Control and Memory Address units.

When Cenable is turned on, a current path from V_{SS} to the output is established, for one column decoder is enabled and all write-data lines have been charged high (negative). If the selected cell (the cell at the intersection of the selected column and selected row) contains a low, the write-data line will discharge after Precharge is removed and the output current will be cut off. If, however, the selected cell has been negatively charged (high), the output current will continue to flow.

Cenable must remain present for a sufficient time after Precharge turn-off to allow the contents of the selected row of cells to be refreshed. Even after Cenable is turned off (raised to V_{SS}) the addresses must remain present for about 20 nanoseconds to allow completion of internal operations. Precharge will not be applied again until Cenable has been off for at least 85 nanoseconds (see Memory Control operation).

To write new data into the selected cell, with or without a read operation, all sequences proceed as above. However, the write line is activated before Cenable is removed and t_{PW} after the positive edge of Precharge; this allows the write-data lines to stabilize. As a result, the read

data lines are discharged, effectively disconnecting the refresh amplifiers from the write data lines. A path from the data-input line is also enables into the selected write data line. Thus, a direct path from the data input to the selected cell is established. A signal on this input will then overwrite the contents of the cell.

The timing specifications for operating the unit are shown in Table 4-2. All the time values listed, except t_{PO}, t_{ACC1} are generated by the memory system. The time designated t_{PO} refers to the time delay observed between the turn-off of Precharge and the availability of data at the chip output terminals, and is a characteristic of the unit.

The two access times, t_{ACC1} and t_{ACC2} represent a combination of system operating parameters and characteristics of the chip. Thus the stated "minimum" values represent the shortest access times which can be guaranteed when the unit is operated within the limits specified and with rise and fall times of 20 nanoseconds. System access times will exceed these values because of the additional delays and tolerances introduced by the rest of the system.

REFRESH TIME

The maximum time interval between accesses to memory cells (t_{REF}) is specified as 2 milliseconds for units on the BA201-B module, 1 milliseconds for units on the BA201-A module. To guarantee that data is retained within the memory, at least one read or write cycle must be executed for each row of cells within this refresh interval. As the rows are selected by address inputs A_0 through A_4 at least 32 memory cycles, one for each state of address lines A_0 through A_4 must be executed in each refresh interval. These cycles may result from normal accessing, as in a sequential-access mode of operation of the memory. In other cases special refresh cycles must be executed. In the Memory System (AB107 equipment) the cells are refreshed every 1.5 millisecond, in the Memory System (AB108 equipment) every 1.0 millisecond.

CHIP SELECT

In operation, the Cenable clock also acts as a chip (memory unit) select. That is, Precharge and write signals may be applied at their normal times in the cycle, but if Cenable is not applied, the unit will neither deliver current to the output terminal nor will the contents of any cell be altered; no refreshing of memory content takes place during such a cycle.

POWER SUPPLY LEVELS

Signal and power supply levels are important to the proper operation of the unit. Speed is a function of both the V_{SS} level and clock amplitudes. In general, higher amplitudes or voltages result in faster operation. Substrate bias V_{BB} also has an effect on performance. This bias improves noise immunity and prevents parasitic interaction within the device.

INPUT CLOCK AMPLITUDES

To guarantee operation of the memory chip over the full temperature range at the speeds specified the clock amplitudes must be maintained at the specified values. These are:-

High: $V_{SS}+1V \geq V_{HIGH} \geq V_{SS}-0.7V$ at $70^{\circ}C$ to $V_{SS}-1.0V$ at $0^{\circ}C$

Low: $V_{SS}-15.0V$ at $70^{\circ}C$ to $V_{SS}-14.7V$ at $0^{\circ}C \geq V_{LOW} \geq V_{SS}-17V$

The value of the supply voltage (V_{SS}) determines that of the bias voltage V_{BB} (refer to Figure 4-13 of the Power Supply Regulator and Control Circuits).

SYSTEM CONSIDERATIONS

The memory units are used in a rectangular 18 x 4 array to provide storage units of 4096 (4K) words of 18 bits each. Such an array with its supporting circuitry is called a Memory Module, with the main addressing and control circuits for up to eight modules carried on the Memory Address and Memory Control units. These are described in other parts of this section and in Section 5.

Maintenance and safety precautions relating to the Memory Modules and to the memory units are given in Section 7.

The contents of the memory unit has to be refreshed periodically as it is a basically volatile store. The memory system, however, is made non-volatile for at least 8 hours with the use of a battery and a special Low Power Data Retention (LPDR) mode of operation. This is also described in other parts of this section.

MEMORY MODULE

The Memory Module is the basic unit of the AB107/AB108 memory system. It consists of a 4x18 array of memory units to give 4096 (4K) 18-bit words together with immediate supporting circuitry, all accommodated on a single 50-PAK printed wiring board. The block diagram of the Memory Module is given in Figure 4-7. The memory units are described in previous paragraphs. The following paragraphs give the description of the block diagram followed by the function of the auxiliary circuits listed in the table.

Circuit	Function
Level Shifters	adapt TTL logic levels to MOS levels
Cenable-Precharge delay	regulates the overlap (t_{OVL}, t_{OVH})
Auxiliary logic	generates internal control signals from available control signals
LPDR circuit	generates the switched supply (Vccs) used in Low Power Data Retention operation
Data Out Sense Amplifiers	convert the signals appearing on the open-collector of the memory unit data out lines to TTL signals (current to TTL logic conversion)

A description of these circuits is given in Section 5 (Memory Module).

THE MEMORY MODULE BLOCK DIAGRAM

The memory matrix provides the actual storage location within the memory system. It is an array of four rows of 18 memory units, forming four thousand words of 18 bits each.

The data flow to and from the memory matrix is on the 18 data-in and 18 data-out lines corresponding to the 18 bits of each kiloword. The data-in lines of the memory units of corresponding bits in the four rows are connected together in a wired-OR and the same is true of the data output lines. A level shifter is incorporated in each of the 18 data-in lines to adapt the TTL levels from the CPU to the MOS logic levels needed in the memory matrix. Similarly the data out lines from the memory matrix are buffered and level converted in the sense amplifiers.

Selection of a particular location in the matrix is achieved in two stages: first one of the four rows of 18 memory units (one kiloword) is selected by the corresponding kiloword selector signal (1K0 through 1K3). This allows the memory control signals (Precharge, Cenable) to reach the memory units of that word. In the second stage the row and column address signals, through the address level shifters, select a particular 18 bit word within the selected kiloword.

The memory control and timing signals perform functions as follows:

Cenable	Selects memory unit
R/W	Read or Write
Strobe	Strobes output data
MDX	Chooses memory module

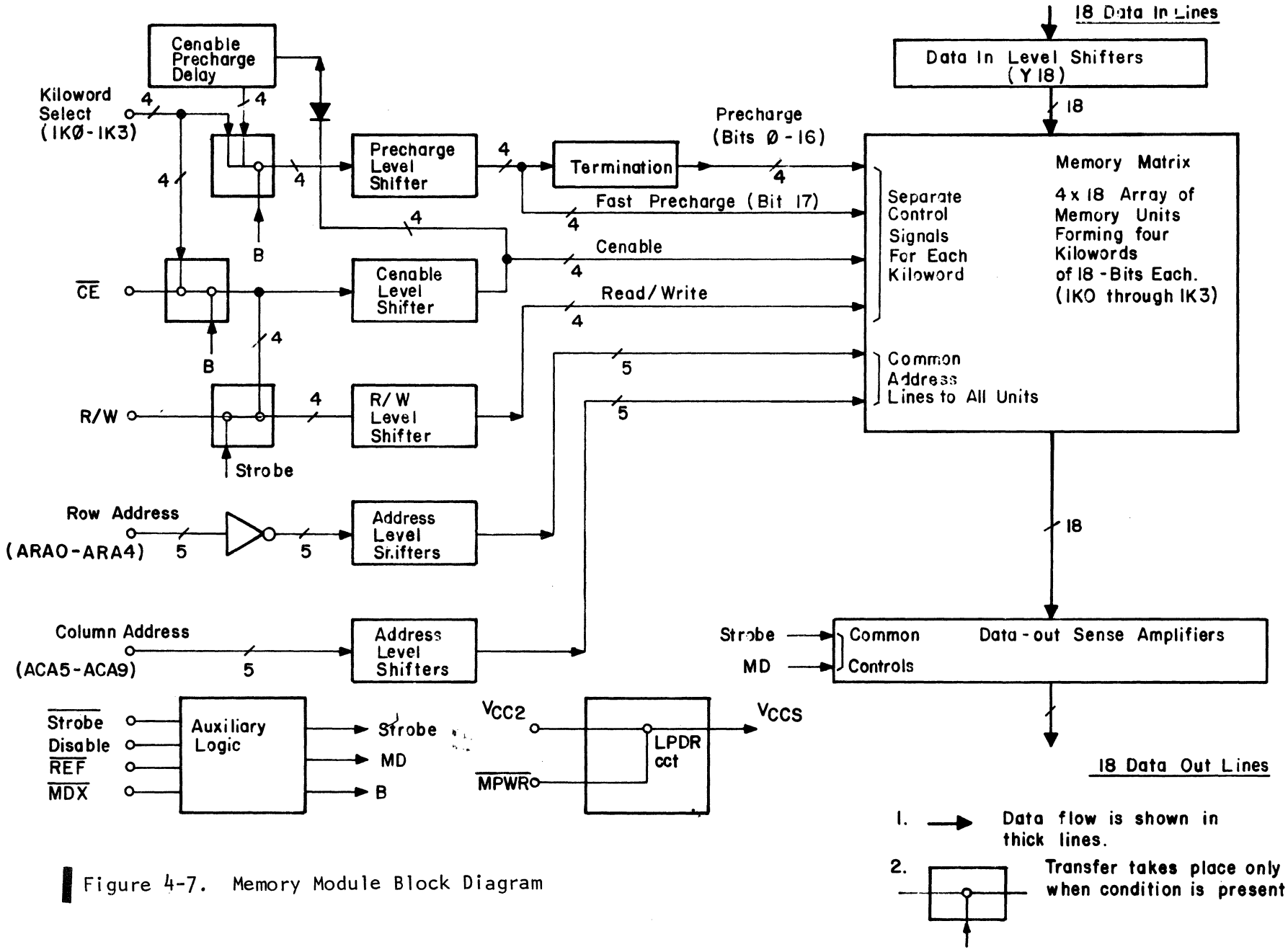


Figure 4-7. Memory Module Block Diagram

AUXILIARY CIRCUIT FUNCTIONS

Level Shifters: TTL to MOS

TTL logic levels are 0.7 volts (low) and 2.0 volts (high). MOS levels are approximately zero volts to V_{SS} (17 volts). A level shifter is needed to match the two kinds of logic circuits.

The following signals use identical control signal level shifters:

- Precharge
- Read/Write (R/W)
- Address

The Cenable signals use the same level shifter but with two components added. See page 5-23.

Level shifters are also used on the 18 data-in lines to adapt the TTL logic levels of the incoming signals to the MOS level of the memory circuits.

The Overlap Circuit (Cenable - Precharge Delay)

There is an overlap delay circuit in the precharge line of each kiloword unit on the Memory Module. It regulates the overlap timing t_{OVL} and t_{OVH} in the memory units (see Table 4-2 and the Detailed Operation of the Memory Unit), and consists of a diode switching network controlling RC delay circuit.

Low Power Data Retention

During power failure the computer reverts to Low Power Data Retention (LPDR) mode. During refresh cycle bursts in this mode none of the TTL logic circuits receive power. This circuit controls the V_{cc2} supply to produce the switched logic (V_{CCS}) supply, provided the optional power back-up sources battery equipment GD611-A is installed. This arrangement preserves the memory content for up to eight hours (see next subsection).

Data-Out Sense Amplifiers

The open collector outputs of the corresponding bits of the four kilowords on the module are wire-ORed to form 18 lines. These are amplified in and gated by the sense amplifiers to form the 18 TTL-compatible output lines of the memory module.

LOW POWER DATA RETENTION (LPDR) MODE

POWER BACK-UP

The memory chips are volatile: they will lose their stored charges if they are not refreshed periodically. To make the memory system non-volatile, it is designed to switch over to battery operation automatically in case of power failure. A back-up battery, optional equipment GD611-A when installed can supply power for the retention of the full memory contents for a period of up to eight hours.

When the utility power fails, the voltage on the dc power supplies begins to drop. The power supply senses this voltage drop, and raises the signal RGPWR to the Memory Control. Due to large storage capacitors in the power supply, the voltages remain in the uncritical region for at least one millisecond and the memory continues to function.

When the Memory Control receives the raised RGPWR signal, it continues to operate normally for half a millisecond. During this time the CPU performs a special interrupt subroutine. At the end of this one-half millisecond period the Memory Control switches to the back-up mode.

To retain the memory content in the back-up mode the Memory Control will not perform CPU or DSA cycles, but immediately performs a burst of 32 row refresh cycles in rapid succession and so refreshes the whole memory. The power supply switches to battery operation. All circuits which require constant power, such as the memory chips, continue to operate from the battery. All circuits that do not require power, such as the CPU, are allowed to fail as the utility power fails. All circuits which need power only during refresh burst, such as address drivers, are power switched by the Memory Control during refresh burst. Since 32 row refresh bursts require

only 14 microseconds to perform, and refresh bursts are performed once every 1024 microseconds, the power switched circuits are off for a considerable time, conserving a significant amount of power. In the back-up mode the memory chips use most of the power.

When the power supply senses that utility power has returned, it switches to utility power, and drops the RGPWR signal. The Memory Control performs one more refresh burst, and then switches to normal mode operation.

During LPDR operation the Memory Hold Battery (optional equipment GD611-A) supplies power. During normal operation the battery is recharged from the power supply.

PROGRAMMER'S CONSOLE

The equipment front panel serves as the Programmer's Console: it carries the switches and indicator lights which enable the operator to control and monitor computer operations.

The front panel controls and indicators are described in the 1784 Computer Reference Manual, publication number 89633400. Their layout is shown in Figure 2-2 of this manual.

The circuits on the Programmer's Console can be grouped in three functional areas:

* Control switches and indicators and associated circuits;
* Register selectors;
* Data-bit selection circuit.

These circuits are described in Section 5 of this manual.

INPUT/OUTPUT

Any peripheral controller that uses the A/Q channel or the DSA channel may be accommodated in the AB107/AB108 equipments. The following table is a partial list. See the preface for more information.

CONTROLLER EQUIPMENT No.	CONTROLLER DESIGNATION
Part of AB107/AB108	Teletypewriter (TTY)
FA716-A	Cartridge Disk Drive Controller (CDDC)
FA442-A	ICL Magnetic Tape Transport Controller (MTTC-ICL)
FV497-A	ICL Phase Encoding (PE) Formatter
FA446-A	LCTT Magnetic Tape Transport Controller(MTTC-LCTT)
FV618-A	LCTT Phase Encoding (PE) Formatter

The Teletypewriter (TTY) Controller forms part of the AB107/AB108 equipment; the other controllers are separate equipments and are accommodated in prewired slots within the main enclosure (AB107/AB108 equipment). Other controllers may be connected to the computer through one of the two access channels, the non-buffered AQ channel using the A and Q registers and the Direct Storage Access (DSA) channel.

In the following a short functional description of the TTY controller is given as well as the pin assignment and timing diagrams for the AQ and DSA channels. The TTY controller logic circuit diagrams are given and are described in detail in Section 5. Refer to the 1784 computer Input-Output Specification Manual, publication number 89637100 and appropriate peripheral controller manuals for further information.

THE TELETYPEWRITER (TTY) CONTROLLER

The TTY Controller can interface the computer CPU with a Teletypewriter Terminal and with a Conversational Display Terminal (CDT). It provides for communication at 9600, 1200, 300 or 110 bauds. The baud rate is selected by inserting a jumper plug in the appropriate location on the board.

DIRECT STORAGE ACCESS (DSA)

The DSA channel provides fast external access to the computer (equipment AB107/AB108). Access connections are available on identical pins of preassigned slots of the main enclosure (equipment AB107/AB108) and of the expansion enclosure, equipment BT148 (refer to Figures 3-1 and 3-2) Printed wiring boards conforming to 50-PAK specifications can be accommodated in these slots. Figure 4-8 shows the timing of the signals on the DSA channel. The pin assignment for the slots allocated to controllers using the DSA channel is given in Table 4-3.

DSA Circuit Connections

The DSA channel is designed to be used with TTL 2-input NAND buffers (IC 7438, PN62031200). Each DSA line is terminated by a 270 ohm pull-up resistor (to V_{cc}) in the CPU. Each input to the CPU loads the line with up to 20 TTL load units. DSA output lines should be loaded with one TTL load unit or less.

Scanner conditions are not prewired and should be made at the time of installation (refer to customer engineering manual for appropriate controller). See the list in the preface.

TABLE 4-3. DSA CHANNEL PIN ASSIGNMENTS

P_1		
A		B
SD05	1	SD01
SD06	2	SD02
SD00	3	SD07
SD12	4	SD08
SD11	5	SD09
SD03	6	SD10
SD04	7	
	8	
$\overline{MC}$	9	SD13
	10	SD14
	11	
$\overline{SRSM}$	12	$\overline{SS}$
	13	
	14	$\overline{SPI}$
$\overline{SRQ}$	15	$\overline{SRI}$
	16	$\overline{SCR\emptyset M}$ ($\overline{SR\emptyset}$)
$\overline{PEL}$	17	$\overline{SVIO}$
SD16	18	AUTOLOAD
$\overline{SFI}$	19	$\overline{SCF\emptyset M}$ ($\overline{SF\emptyset}$)
SD17	20	
32kW	21	$\overline{SWRITE}$
	22	
SA08	23	SA00
SA09	24	SA01
SA10	25	SA02
SA11	26	SA03
SA12	27	SA04
SA13	28	SA05
GND	29	
SA14	30	SA06
SA15	31	SA07

P_2		
A		B
	1	
	2	
GND	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	GND
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	
Vcc	31	

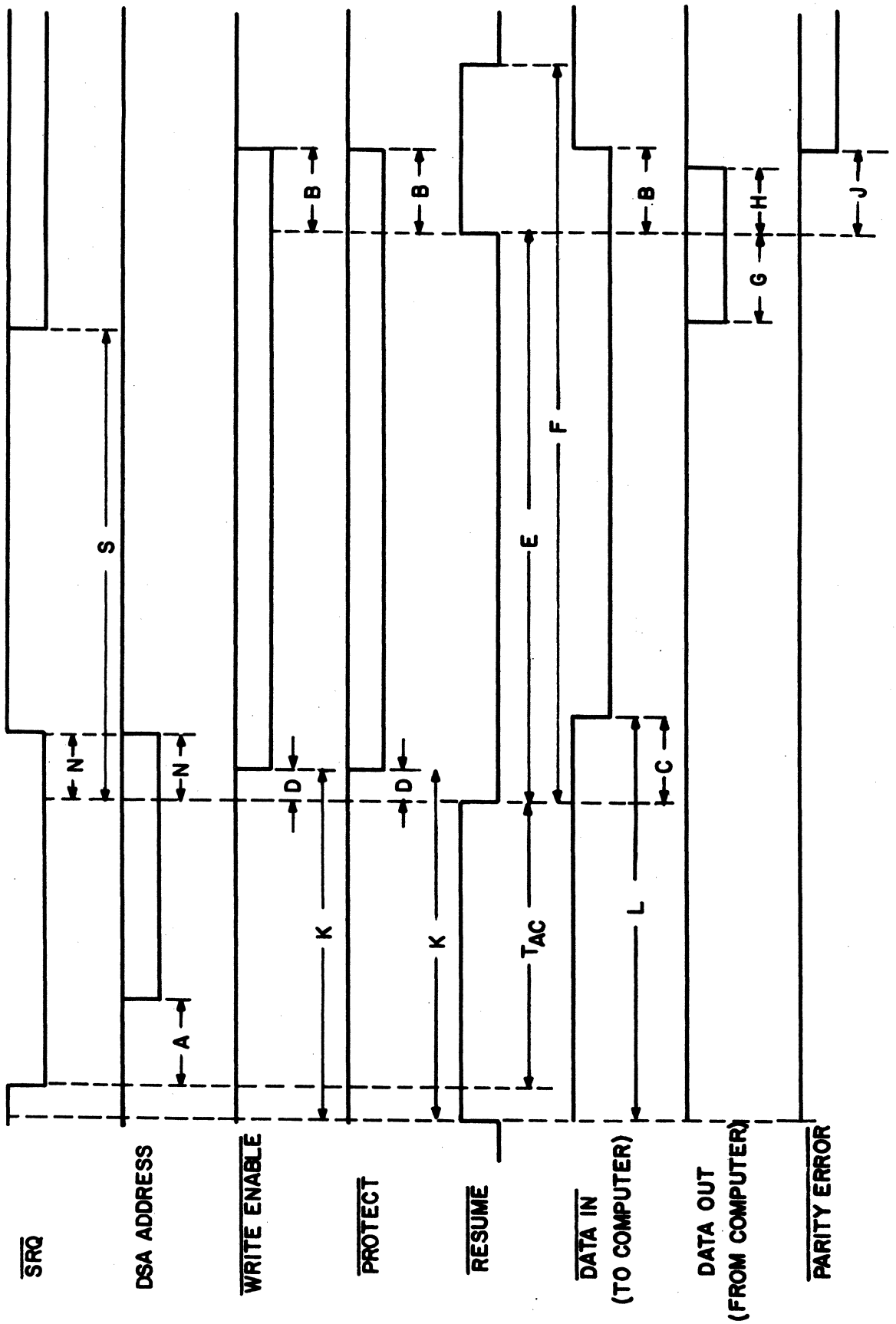
NOTES:

1. Signal polarity
   Address bits (SA00÷SA15) are active high.
   Data bits (SD00÷SD15) are active high for DSA transfers from the computer (Write).
   Data bits (SD00÷SD15) are active low for DSA transfers to the computer (Read).
   All other signals on the DSA bus are as indicated (overlined: active low).

2. Power Supply $V_{cc} = +5V$.

   Total usage of all controllers on A/Q and DSA buses should not exceed 30 amperes in each enclosure.

3. GND = logic ground.



Notes: refer to next page.

Figure 4-8. DSA Channel Timing

NOTES to Figure 4-8.

1. Signal names:

   T_{AC}: DSA Access Time

   SRQ: Memory Access Request from DSA channel.

2. Timing

	1784-1			1784-2			Remarks
	minimum (nsec)	typical (nsec)	maximum (nsec)	minimum (nsec)	typical (nsec)	maximum (nsec)	
A.	-	-	70	-	-	110	
B.	50	-	175	50	-	200	
C.	-	-	120	-	-	245	
D.	-	-	60	-	-	60	
E.	390	440	490	605	655	705	
F.	-	600	-	-	900	-	
G.	110	-	-	190	-	-	
H.	70	-	-	120	-	-	
J.	-	-	10	-	-	10	
K.	0	-	-	0	-	-	
L.	150	-	-	210	-	-	
N.	0	-	215	0	-	320	
S.	-	-	285	-	-	470	at maximum DSA access rate
T_{AC}	220	-	855	330	-	1240	with DSA Priority
			1455			2140	without DSA Priority

NOTES to Figure 4-8 (Cont'd.):

3. Refresh cycle time:

   490 nsec once every 32 microseconds (600 nsec Memory)
   735 nsec once every 48 microseconds (900 nsec Memory)

4. Modes of Operation

   Worst Case

   The maximum DSA access time (T_{AC}) occurs when the memory system performs CPU access cycles and successive Refresh cycles.

   DSA Priority signal active

   The memory system cannot perform CPU cycles. The DSA access time (T_{AC}) is minimum; it is increased by the regular occurrence of Refresh cycles.

   Successive DSA requests

   The memory system cannot perform CPU cycles on the memory bank addressed by the equipment on the DSA channel. The DSA cycle time is equal to the memory cycle time (600 nsec or 900 nsec). The DSA cycle time will be increased by the Refresh cycles. Note that on single-bank operation no CPU access can occur if the DSA requests are generated fast enough.

A/Q CHANNEL

This is the non-buffered bi-directional input/output (I/O) channel for the computer (equipment AB107/AB108). It utilizes the 16-bit A and Q registers of the CPU. The Q register contains the address of the peripheral equipment; the A register contains the data equipment status and director functions. Access connections are available on identical pins of preassigned slots of the main enclosure (equipment AB107/AB108) and of the expansion enclosure equipment BT148 (refer to Figures 301a, 301b). Printed wiring boards conforming to 50-PAK specifications can be accommodated in these slots (refer to AB107/AB108 Computer Input-Output Specification Manual, publication number 89637100).

Output on A/Q Channel

A single word is output from the A register whenever an output instruction is executed by the computer. The presence of the output data is signified by the active state of the write line. The peripheral equipment whose address is in the Q register should respond with a Reply or a Reject signal within 4 microseconds. The computer generates an internal Reject and reinitiates execution of instructions if no response is received from the device within 12.8µsec (AB108) or 19.2µsec (AB107). If a Reply is received by the computer, the next instruction executed is the one following the output instruction (P+1). If an external Reject is received, the next instruction executed is located at $P + 1 + \Delta$, where Δ is the lowest eight bits of the output instruction, the highest bit of Δ being a sign bit. If an internal Reject is generated the next instruction executed is located at $P + \Delta$. P is the address of the output instruction.

Input on A/Q Channel

A single word is input to the A register whenever an input instruction is executed by the computer. The request for data by the computer is signified by the active state of the read line. The peripheral device whose address is in the Q register responds with a Reply when data is available to the A register.

If no data is available, the peripheral device responds with a Reject. In either case, the peripheral device must respond with a Reject Reply within 4 microseconds. If no response is obtained in 12.8 μsec (AB108) or 19.2 μsec (AB107), the computer generates an internal Reject. Reply causes the computer to go to address P + 1, where P is the address of the input instruction. An external Reject causes the computer to go to address P + 1 + Δ, where Δ is the lowest 8 bits of the input instruction, the highest bit of Δ being a sign bit. Internal Reject causes the computer to go to address P + Δ.

Status on A/Q Channel

Each peripheral device must have one or more codes which can be loaded into the Q register. When the computer executes an input instruction the status of that device will be loaded into the A register. All devices must respond to status requests with a Reply since the status must always be available within 4 microseconds. If a no response is received by the computer, it generates an internal Reject after 6.4 μsec (AB108) or 9.6 μsec (AB107).

A/Q Channel Access

A/Q Channel accesses are available on identical backplane pins of prewired card slots of the equipments. Table 4-4 lists pin assignments for the various signals.

A/Q Channel Timing

Figure 4-9 describes timing restrictions of the A/Q channel. In addition to the signals shown, a timing pulse is generated 135 nsec (±40 nsec) before a Read or Write signal can appear on the A/Q channel. The timing pulse is active for 75 nsec (±20 nsec). For more detailed signal description and timing, refer to I/O Specification manual number 89673100.

A/Q Channel Loading Rules

Each signal (data or control), transmitted from a peripheral controller to the CPU in the A/Q channel, must be driven by an open-collector NAND buffer (IC Type 7438, CDC PN62031200). Each input line is terminated at the input to the receiver on the CPU by a 180 ohm pull-up resistor (to V_{cc}). The input loads the line with 20 TTL loading units.

Each device on the A/Q channel is allowed to load any line from the CPU by one TTL load unit. The data bus (A register) is bi-directional. Figure 4-10 gives examples of typical input, output and bi-directional lines.

TABLE 4-4. A/Q CHANNEL PIN ASSIGNMENTS

P_1		
A		B
$\overline{A05}$	1	$\overline{A01}$
$\overline{A06}$	2	$\overline{A02}$
$\overline{A00}$	3	$\overline{A07}$
$\overline{A12}$	4	$\overline{A08}$
$\overline{A11}$	5	$\overline{A09}$
$\overline{A03}$	6	$\overline{A10}$
$\overline{A04}$	7	$\overline{CMI}$
	8	
TP	9	$\overline{A13}$
	10	$\overline{A14}$
$\overline{A15}$	11	GND
Q00	12	Q01
Q02	13	Q03
Q04	14	Q05
Q06	15	Q07
Q08	16	Q09
Q10	17	Q11
Q12	18	Q13
Q14	19	Q15
$\overline{WEZ}$	20	
$\overline{READ}$	21	$\overline{WRITE}$
$\overline{REPLY}$	22	$\overline{REJECT}$
$\overline{PRTM}$	23	$\overline{MC}$
	24	
	25	
	26	
	27	
	28	
GND	29	
	30	
	31	

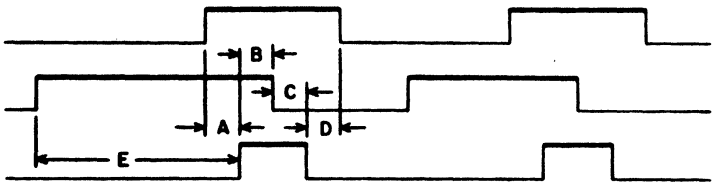
P_2		
A		B
	1	
	2	
GND	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	GND
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	
Vcc	31	

Notes: 1) Q00÷Q15 are active high; all other signals are active low.

2) Vcc = +5V. Total usage of all AQ and DSA controllers should not exceed 30 amps in each enclosure.

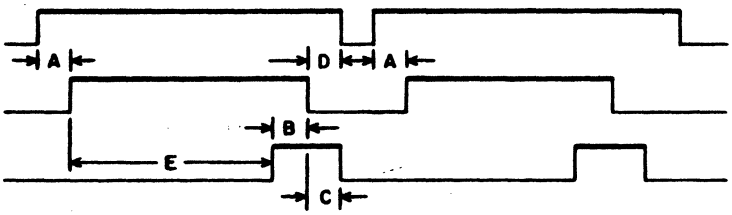
3) GND = logic ground

INPUT OPERATION



A = 0 μSEC MIN @ PERIPHERAL DEVICE
B = 0.0 μSEC MIN @ COMPUTER
C = 0.0 μSEC MIN @ PERIPHERAL DEVICE
D = 0 μSEC MIN @ PERIPHERAL DEVICE
E = 4.0 μSEC MAX @ PERIPHERAL DEVICE
0.2 μSEC MIN @ PERIPHERAL DEVICE

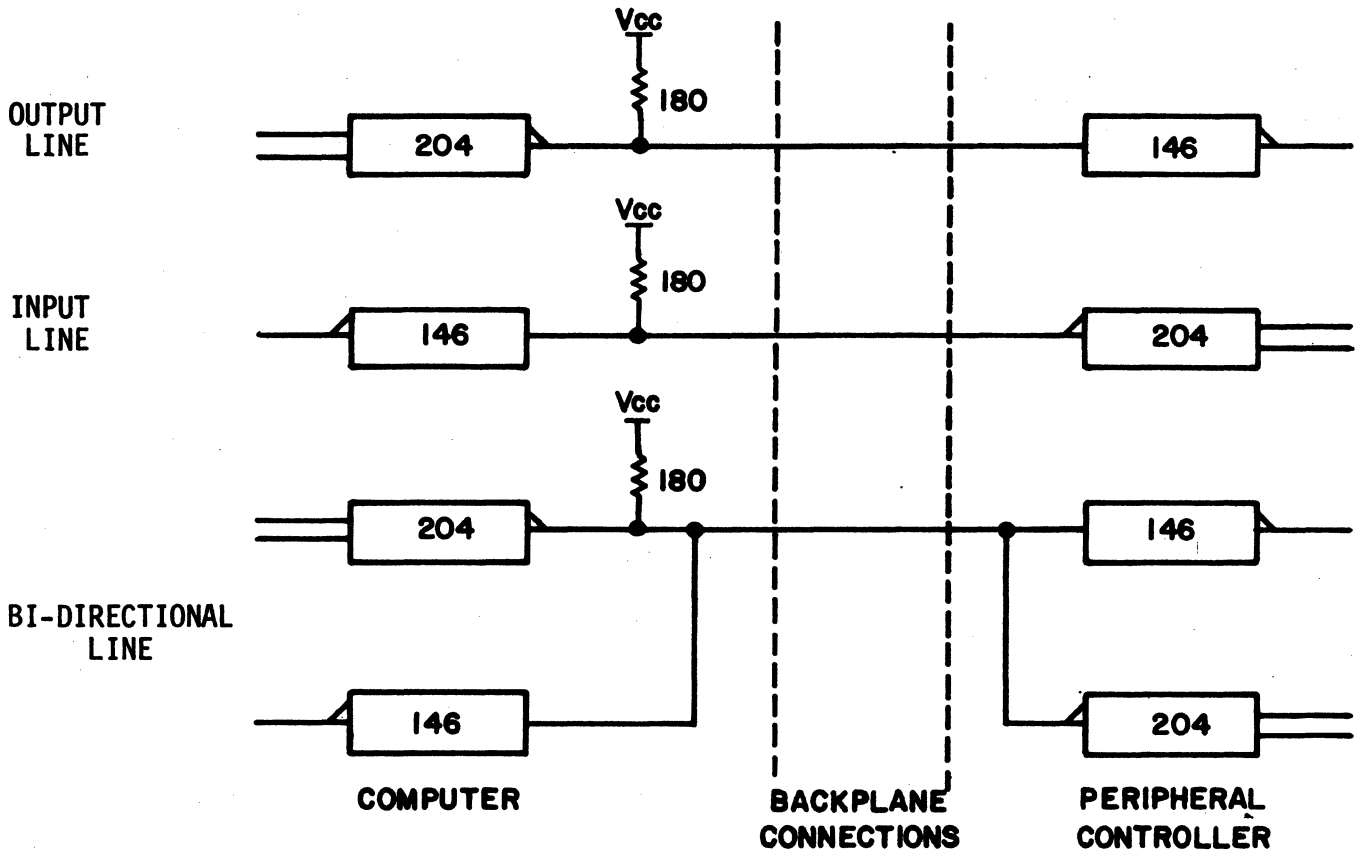
OUTPUT OPERATION



A = 0.1 μSEC MIN @ COMPUTER
B = 0.0 μSEC MIN @ COMPUTER
C = 0.0 μSEC MIN @ PERIPERAL DEVICE
D = 0.1 μSEC MIN @ COMPUTER
E = 4.0 μSEC MAX @ PERIPHERAL DEVICE
0.2 μSEC MIN @ PERIPHERAL DEVICE

NOTE:
THE ADDRESS BITS WILL BE ON THE CHANNEL A MINIMUM OF 0.1 μSEC BEFORE AND AFTER THE READ OR WRITE SIGNAL.

Figure 4-9. A/Q Channel Timing



NOTE: 146 can be replaced by any TTL logic circuit gate providing that the line is loaded by only one load unit.

Figure 4-10. A/Q Channel Input/Output Lines

INTERRUPTS

There are 15 external interrupt positions provided, each brought out on an individual backplane pin. These are used to interrupt the computer program on specified conditions arising in the peripheral devices. The computer program determines the interrupt priorities, that is, the order in which the interrupt requests are dealt with in the computer. The program acts through the computer mask (M) register. Should two interrupts occur simultaneously, the hard-wired order of interrupts will determine priorities (refer to table 4-5).

Interrupt Access

The 15 external interrupts are accessible on the backplane pins of the main enclosure. A single wire (part number 89724702) is required to connect an interrupt source to the appropriate interrupt level. Table 4-5 lists the pin assignments for the interrupt levels. Interrupt signals are active low. See section 3 for the installation procedure of the interrupt cable. For the interrupt connections for controllers installed in the BT148 expansion enclosure, refer to Hardware Maintenance Manual publication number 89758600 of the AT310 TTL A/Q-DSA Bus Expander.

TABLE 4-5. INTERRUPT ACCESS PIN ASSIGNMENT

Line	AB107/AB108 Card Slot	Pin
0	-	-
1	25	P1B10
2	25	P1A07
3	25	P1B07
4	25	P1A05
5	25	P1A06
6	25	P1B06
7	25	P1B05
8	26	P1A10
9	26	P1B10
10	26	P1A07
11	26	P1B07
12	26	P1A05
13	26	P1A06
14	26	P1B06
15	26	P1B05

NOTE: Interrupt priority levels are in reverse order of interrupt line numbers.

Timing Considerations for Two Bank Operation

The computer can have one or two memory banks (see paragraphs on Memory System in this section), each with a maximum of 32K words. The two banks work independently. Any memory request using an address of $7FFF_{16}$ or less will access the lower bank. Any memory request using an address of 8000_{16} or above will access the upper bank. The two banks have identical control logic.

Each bank can perform three types of memory cycles: refresh cycle, DSA cycle or CPU cycle. The DSA has priority over the CPU and refresh cycles have priority over the other two. DSA and CPU cycles are initiated by external signals while refresh cycles are initiated by internal timing logic.

If the CPU accesses one bank, the DSA can simultaneously access the other bank. In this case, the CPU and DSA can work at maximum speed subject to refresh cycle requirements.

If the CPU and DSA access the same bank, then memory cycles are shared between them. If the CPU requests a memory access while a DSA cycle is in progress, it must wait until the DSA cycle is finished. If a refresh cycle is pending when the DSA cycle ends, the CPU must also wait for that refresh cycle to be completed.

Similarly, if the DSA requests access while a CPU cycle is in progress, it must wait until the CPU cycle is finished. If a refresh cycle is pending when the CPU cycle ends, the DSA must also wait for that refresh cycle to be completed.

Successive DSA cycles: if a DSA cycle is followed by another one within the maximum delay specified after the start of RESUME (see Figure 4-8, note 2) and the CPU is waiting to reference the memory, then the second DSA request will be taken and the CPU forced to wait. This is because the memory system gives the DSA priority over the CPU. Thus the DSA can obtain continuous memory cycles and block CPU memory accesses by sending memory requests at a high enough rate. This does not apply in two bank operation because the CPU can access the upper bank while the DSA sends a request to the lower bank. If the DSA then tries to access the upper bank it has to wait until the CPU access ends.

The DSA can unconditionally block all CPU memory accesses with the signal $\overline{\text{PRIORITY}}$. This allows the DSA to access both banks at maximum speed, except when it has to wait for a refresh cycle.

Note that the speed of data transfer is a function of the computer clock in the Timing circuits. This clock is 1.5 times faster in the AB107 equipment than in the AB108 allowing proportionally faster DSA access.

POWER SUPPLY

The following paragraphs describe the functions and organization of the power supply unit. The power supply unit is part of the main computer enclosure (equipment AB107/AB108) and the expansion enclosure (equipment BT148) Detailed circuit and connection diagrams are given in Section 5 of this manual.

ELECTRICAL

The power supply receives the main line-voltage through the three-conductor flexible power cord which plugs in the socket at the rear of the enclosure. The AC POWER switch and input fuse are located adjacent to the input socket (Figure 2-1). The power supply unit provides all the operating supplies for the equipment within the enclosure, including the charging and protection circuits for the backup source, Memory Hold Battery, equipment GD611-A.

The supplies, with brief characteristics, are listed in Table 6-1. The input ac line specifications are as follows:

104 - 127 vac, 49 - 60.6 Hz, single phase, up to 600 VA
or 198 - 264 vac, 49 - 60.6 Hz, single phase, up to 600 VA

Note: the equipment is normally supplied for nominal 110V operation. It can be field converted to nominal 220V (refer to Section 3).

MECHANICAL

The power supply unit is mounted on the hinged front door of the computer and expansion enclosures (Figure 3-2). Access to it may be obtained by opening the front door of the enclosure. It is cooled by a blower mounted immediately beneath it (in the door). The power supply may be field calibrated (refer to Section 6).

The memory hold battery (equipment GD611-A) when installed, is situated on the inside of the equipment rear cover. The battery fuse is part of the input circuit situated at the rear of the enclosure (Figure 2-1).

WARNING

The power supply does not use a main isolating line-transformer at its input; its circuits between the ac line input and the isolating networks are therefore at line voltage. Do not handle the power supply unit while the computer line cord is connected to the ac supply.

GENERAL DESCRIPTION AND BLOCK DIAGRAM

The power supply unit is described below, the explanation being based on the simplified block diagram of Figure 4-11. More detailed block diagrams follow. Detailed circuit diagrams are given in Section 5.

The ac input power is taken to the computer enclosure through the power line cord. This plugs into the ac power socket of the Input Unit mounted at the top rear of the computer enclosure (Figure 2-1, 3-5). The Input Unit contains the computer main circuit breaker (AC POWER switch), the input fuse (F1), the battery fuse (F3) and the line filter. Note that the input unit is not part of the power supply unit.

The computer chassis (frame) is connected to the third conductor of the line cord; the conductor must be connected in turn to the ground (refer to Control Data Mini Computer Systems, Site Preparation Manual, publication number 60437000). The logic ground is brought out on a separate pin and should be connected to the logic ground of the installation (refer to Section 3).

The equipment is switched on in two stages: first the ac line power is applied to the power supply unit of the enclosure by switching ON the AC POWER switch on the rear panel (part of the Input unit); in the second stage the power supply unit is activated by turning on the dc POWER switch on the Programming Console.

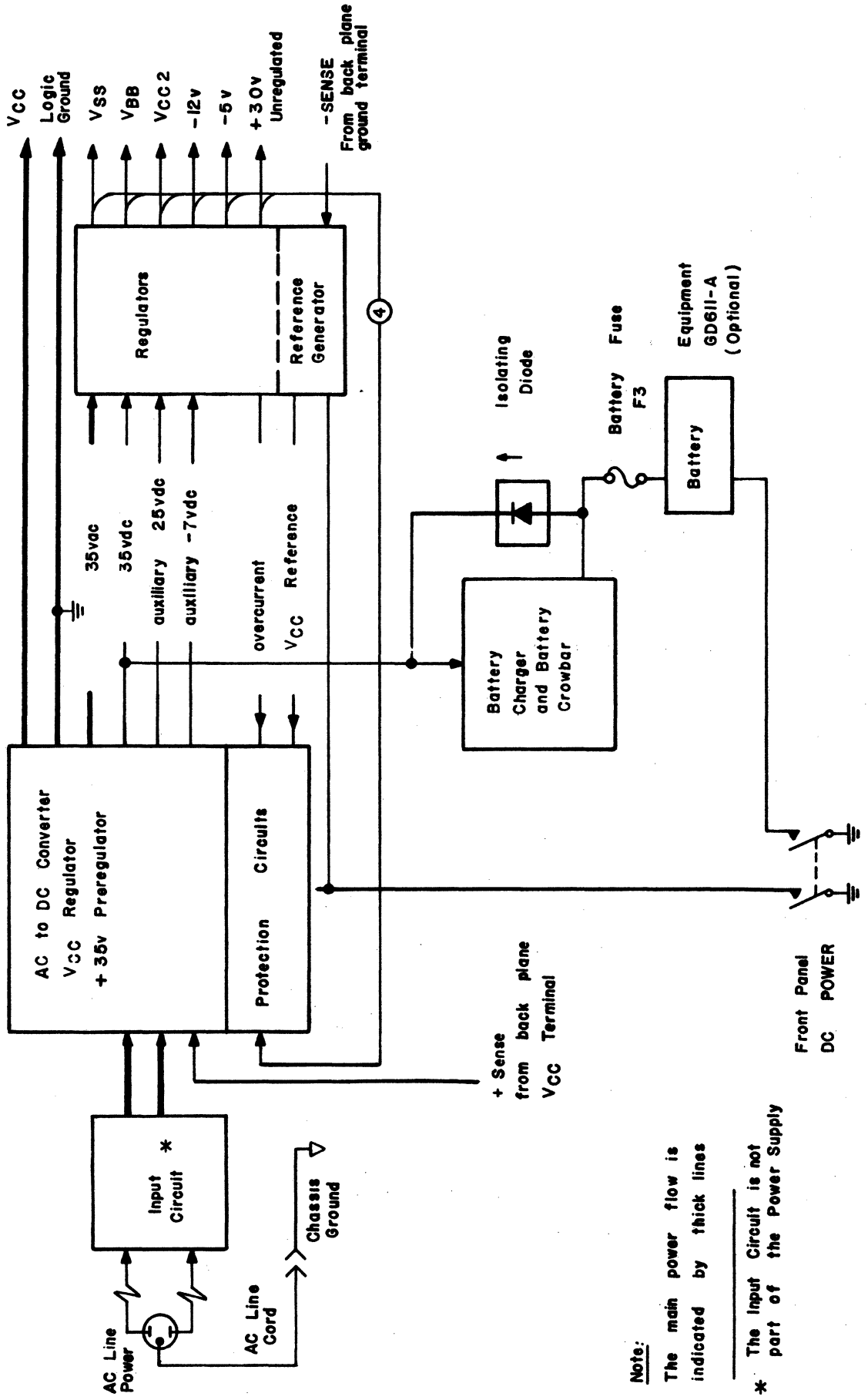


Figure 4-11. Power Supply: Simplified Block Diagram

The main source of dc power is the ac-to-dc converter. This provides the main unregulated logic supply of the computer (V_{cc}) and the internal auxiliary supplies (+35V, +25V, -7V). The circuit uses a high frequency switching regulator to generate V_{cc}. This circuit serves as preregulator for the other supplies which are derived from the +35V supply through the regulator section.

Closely associated with the converter are the overvoltage and overcurrent protection circuits which switch off the whole of the unit, should preset fail conditions be exceeded on any one of the supplies. One of the auxiliary independent supplies (+25V) provides the voltage for the reference generator of the regulators to aid in operation of the circuits on switching on.

On failure of the ac line power the +35V internal supply fails and the backup power source, optional memory hold battery equipment GD611-A (if installed), supplies the regulators througn an isolating diode, connecting it to the +35V line. In this case the computer switches to Low Power Data Retention (LPDR) mode of operation and only the memory power supplies are active. The LPDR operation is described in paragraphs on the operation of the Memory in this section and in Section 5. Note that the front panel DC POWER switch must remain ON during LPDR operation.

The battery charge circuit charges the memory hold battery during normal operation of the equipment. The battery is protected by its fuse both against excessive charging current and against overload. The battery fuse is blown also through the battery crowbar (SCR) circuit when an overvoltage is detected on any one of the power supplies used during emergency (LPDR) operation. The front panel dc POWER switch controls the power supply: with the rear panel AC power ON, the DC POWER switch disables the power supply circuits when off and enables them when on.

The AC-to-DC Converter and Protection Circuits

Figure 4-12 shows the block diagram of the main dc generator circuits with their controls and the power supply protection circuits.

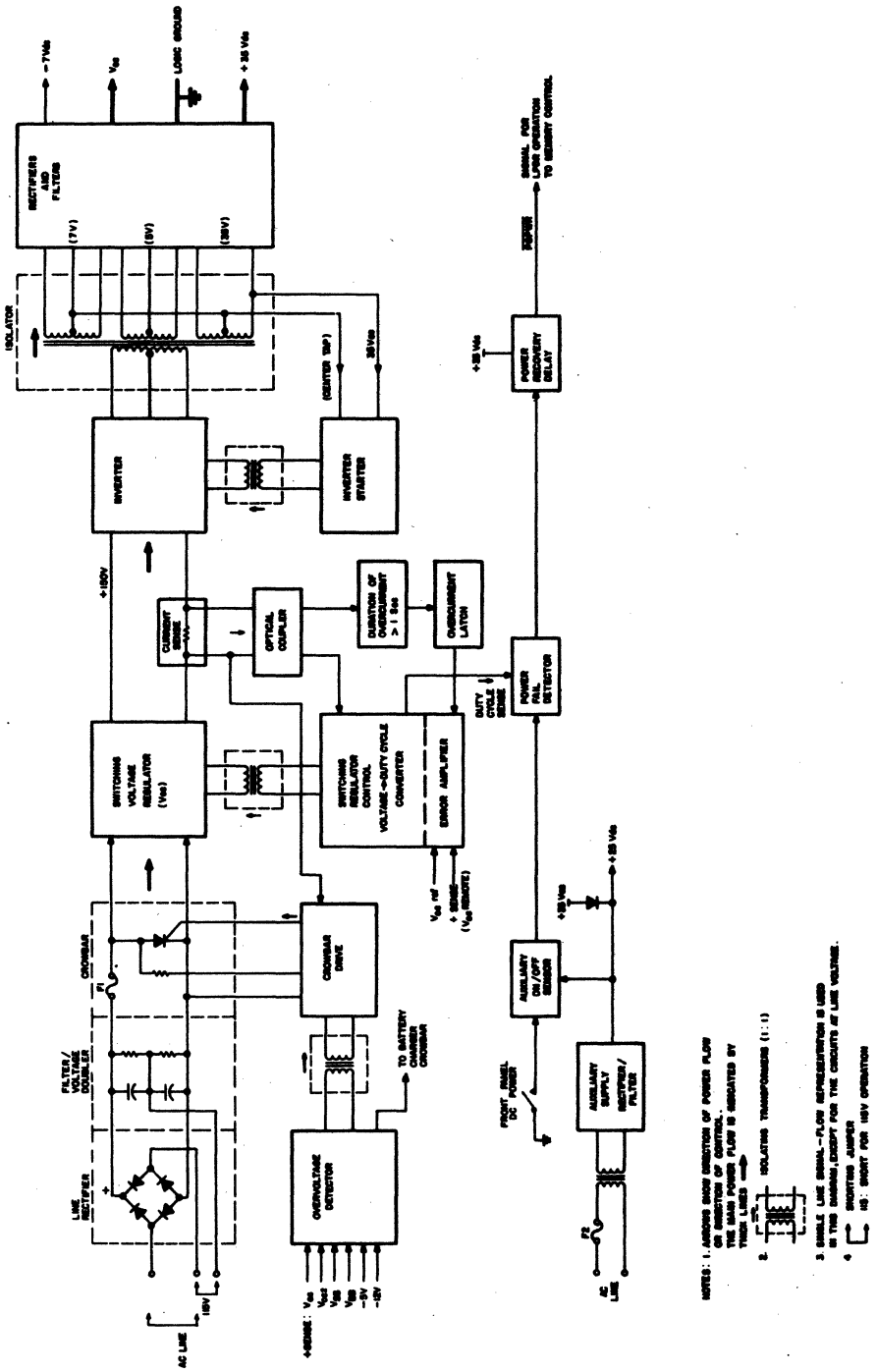


Figure 4-12. AC-to-DC Converter and Protection Circuits: Block Diagram.

A feature of the power supply main power path is that the main isolating transformer works at a frequency of about 20 kHz. Its bulk is therefore drastically reduced compared to the input transformer of a more conventional solution working at 50Hz. The line rectifier is connected directly to the ac input line and its slightly filtered dc output taken through a voltage regulator to a 20kHz inverter. The isolating transformer can handle substantial powers in a small volume because of its high frequency of operation.

This frequency allows also high efficiency final filtering with comparatively small components, resulting in a dc output with very small ripple-content.

The technique of employing an isolator removed from the direct input makes it necessary to employ small isolators in the control paths. Signal transformers serve in the alternating and interrupted current paths, and an optical coupler is used where the coupling signal is dc (switching regulator cur-current sense circuit).

The main switching regulator regulates the logic supply (V_{cc}). Its control circuit compares the V_{cc} reference voltage from the reference generator to the V_{cc} voltage sensed at the computer circuits. The regulator therefore compensates both for input and for load changes on the V_{cc} line. As this carries typically 35 amperes, the load regulating feature with remote sensing is particularly important. The remote sensing points (+ SENSE, - SENSE) are at the backplane of the enclosure.

The switching regulator serves as a preregulator for the +35V and -7V internal dc supplies, though load changes on the V_{cc} supply will show as regulation noise on these. As they feed the final regulators, this noise does not appear on the power supplies, except the +30V unregulated supply.

An auxiliary supply (+25V) is generated by a conventional line transformer and rectifier filter directly from the ac line input. This supply is used in the reference generator and the regulators which get their supply from the +35V line: when the ac line is applied to the computer (AC POWER switch on the rear of instrument) this connection allows the regulators to stabilize before the front panel dc POWER switch enables the circuits in the main power path. The auxiliary supply is protected by a separate fuse (F2: 100mA).

The Low Power Data Retention (LPDR) mode of operation is initiated when the main logic supply (V_{cc}) fails, due to any one of several conditions (see Protection circuits below). The failure of the V_{cc} supply is sensed in the Power Failure Detector by the absence of the switching signal to the V_{cc} switching regulator while the front panel dc POWER switch is ON. During LPDR operation, only the circuits are supplied which are needed to retain the content of the memory within the enclosure, provided the power back-up source (memory hold battery, equipment GD611-A) is installed (refer to paragraphs on memory operation in this section). To avoid hunting on momentary recovery of the ac supply, the power recovery delay allows the computer to return to normal operation only when the ac supply has been established for some seconds. Note that the power fail detector is actuated also by failure of the switching regulator control circuit: when the duty cycle of the switching regulator tends to 100% (continuous current) the power fail detector initiates an LPDR signal.

Protection Circuits

The power supply is protected against both overvoltage and excess current. Over-current occurrring on any one of the supplies, the whole power supply shuts down. When an overcurrent condition occurs in the main power path, the main voltage regulator (switching regulator for V_{cc}) is shut down. This is done by stopping its switching signal through the overcurrent protection circuits. Should the overcurrent condition last for more than one second, the overcurrent latch reduces the voltage of the switching regulator and so activates the power fail circuit. The overcurrent latch is set also if any of the circuits in the regulator section detect an overcurrent condition. In this case, the LPDR mode of operation is initiated.

If the overcurrent protection circuit fails to shut down the main power path, the crowbar drive is activated directly through its isolating transformer and so fires the SCR of the main crowbar circuit. This in turn blows the main fuse (F1). Each of the supply voltages is connected to the overvoltage detector. Should a preset voltage be exceeded on any one of the supplies, the detector actuates the crowbar circuits, which in turn blow both the main fuse (F1) and the battery fuse (F3).

Regulators and Control Circuits

The computer supplies, other than the main logic supply (V_{cc}), have individual control and regulator circuits. Table 4-6 summarizes these.

TABLE 4-6. SUMMARY OF REGULATED POWER SUPPLY CIRCUITS

Supply Designation	Type of Regulator	Overcurrent Detector	Supply from
V_{cc2}	switching	yes	+35V dc
V_{SS}	switching	yes	+35V dc
V_{BB}	series	no	+35V dc
-12V	series	no	35V ac
- 5V	series	yes	-7V dc
+30V	none	yes	+35V dc

Figure 4-13 is a block diagram showing these circuits. All regulators receive their reference voltage from the reference generator, except the V_{SS} supply, whose reference is a tap of a potentiometer divider on the V_{BB} supply. The reason for this arrangement is that the memory unit bias and supply voltages must be applied together and at a definite differential between them, to avoid possible overheating of the unit. Note that the +30V supply has no regulator but relies on the regulation from the V_{cc} regulator acting on the +35V internal supply.

The reference generator uses the sense line (the remote computer logic ground, -SENSE) as its reference ground, thus compensating for current in the ground circuit between the power supply and the computer. The reference generator is actuated as soon as the AC power switch on the rear panel is switched on. It is thus stabilized whenever power is applied to the computer and is ready for operation as soon as the front panel dc POWER switch is thrown ON.

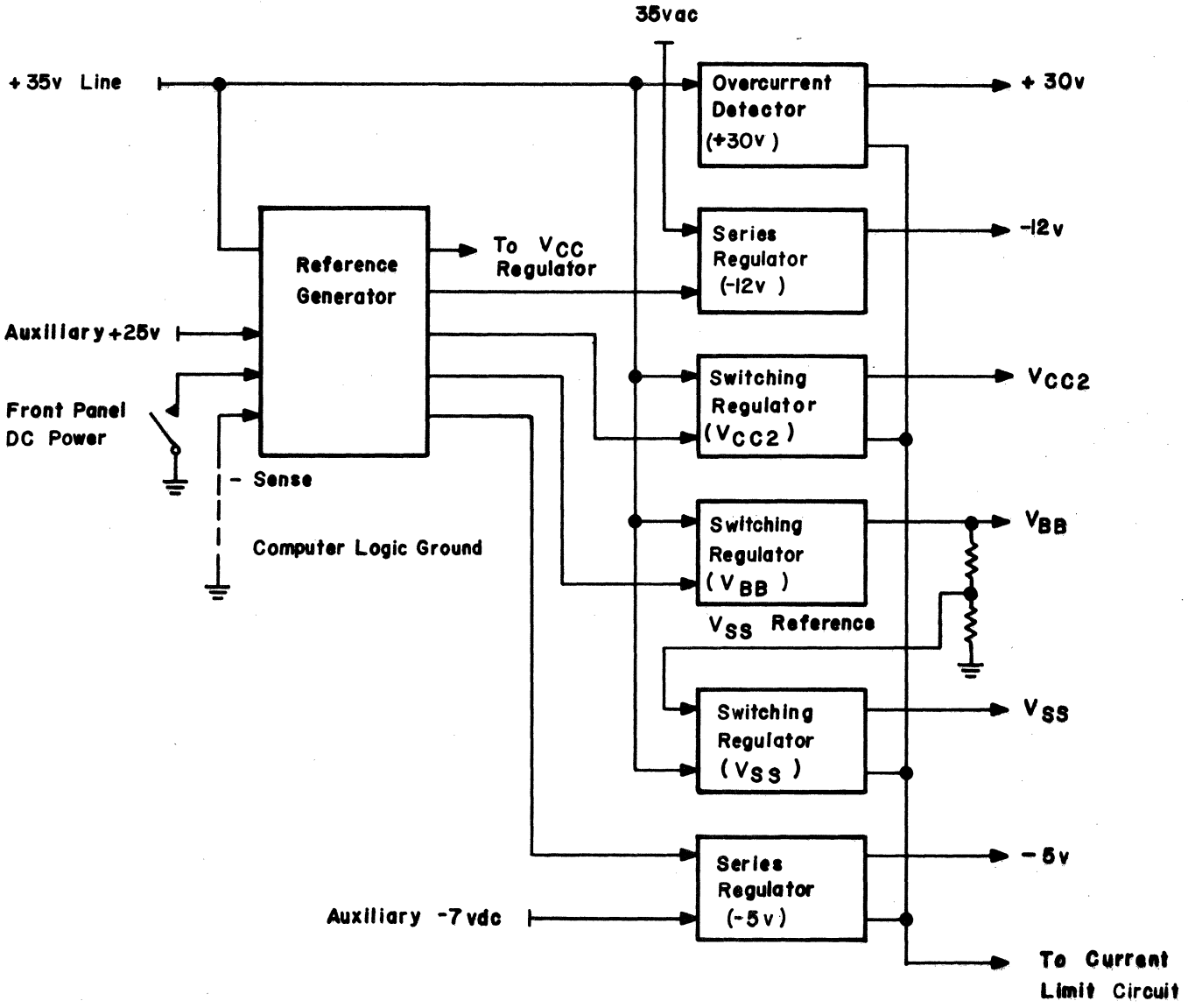


Figure 4-13. Power Supply Regulator and Control Circuits: Block Diagram (see also page 5-448)

The Switching Regulator

Figure 4-14 illustrates the basic principles of the voltage conversion circuit which is at the heart of the switching regulator. Transistor Q1 is a switching transistor in the main load path. It is switched on and off by a pulse waveform generated in the switching network.

The voltage and current waveforms are shown in part b of Figure 4-14. This voltage is smoothed by the LC filter to give dc output with very little ripple. Diode D1 is a catching diode to complete the inductor circuit when the transistor is off.

The output voltage of this circuit is thus the average of the switched waveform V_D:

$$V_{out} = V_{in} \frac{t_{on}}{T}$$

and it is substantially independent of the load current. The dissipation in the transistor is determined by the difference in input and output voltages and the load current, as in a series regulator, but is reduced by the duty cycle factor (t_{on}/t_{off}) compared with the conventional series regulator. The output voltage can be changed for a particular input by varying the duty cycle of the switched waveform.

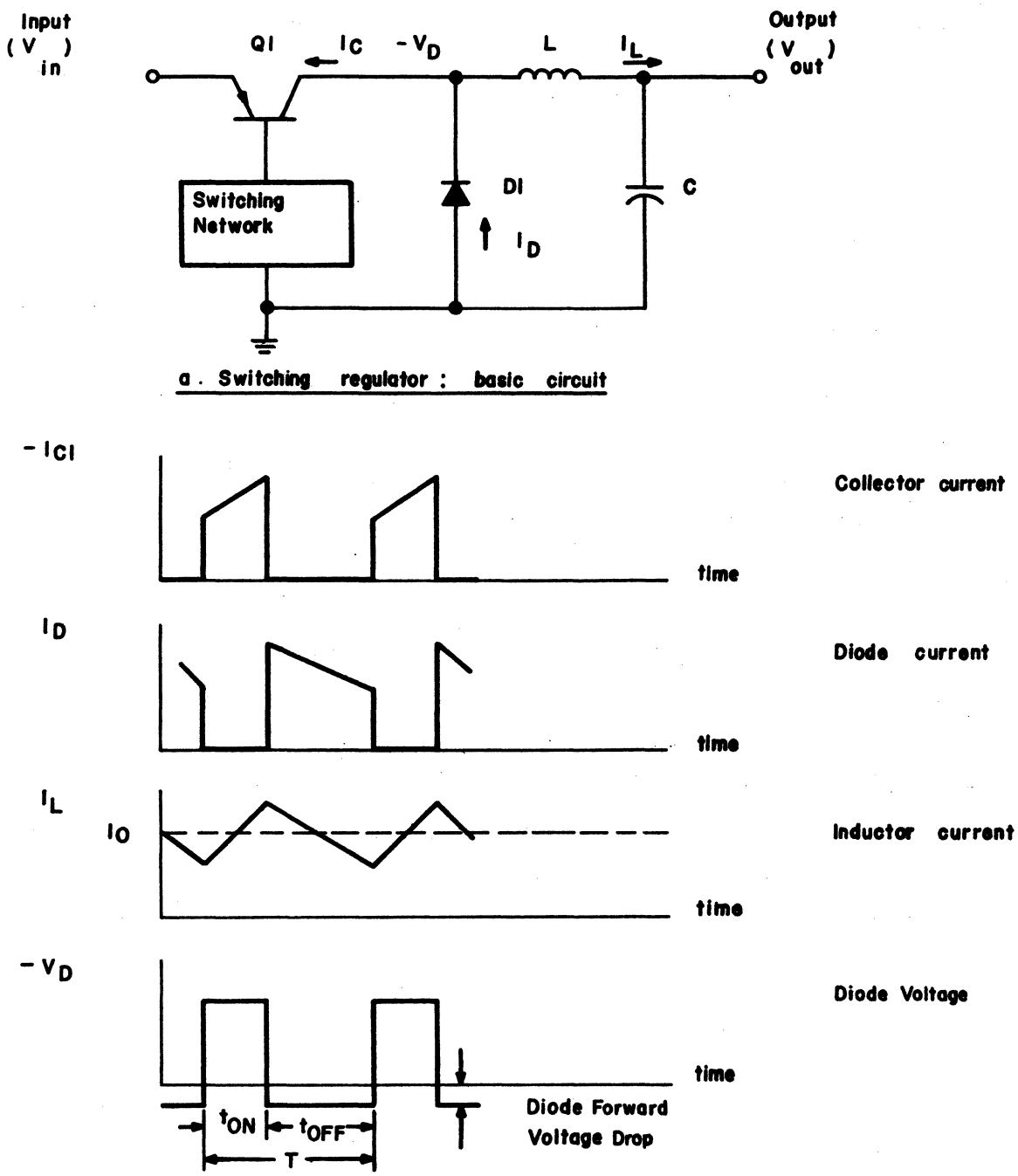


Figure 4-14. Switching Regulator: Basic Circuit and Waveforms.

THE CENTRAL PROCESSING UNIT

The Central Processing Unit (CPU) consists of the printed wiring boards (PWB) listed in the following table:

Designation	Remarks
Programmer's Console	Carries the front panel controls
Arithmetic and Logic Unit (ALU)	Two identical PWB's
Decoder	
Timing	
Input/Output (I/O) Interface	
Console Interface	
TTY Controller	Breakpoint Logic is also accommodated on this card.

Note:

The whole of the CPU is part of the AB107/AB108 equipment.

PROGRAMMER'S CONSOLE

Controls and Indicators

The Programmer's Console circuits are on a single printed wiring board which also carries the controls and indicators of the computer. In type identifiers C and D, a set of 29 pushbutton switchcaps, part number 89764900, is a spare part for the console.

Anti-Bounce Circuit

All PWA's require anti-bounce circuitry for the GO and MANUAL INTERRUPT pushbutton switches. The anti-bounce circuit includes two one-shots and associated resistors, capacitors, and inverters. PWA's P/N 89985400 and 89602069 have anti-bounce in the printed circuit. See logic drawing 89640500 sheet 4, zones D-4 and C-2 on page 5-157.

PWA's P/N 89987600 and 89987700 have no anti-bounce circuit on the board. They therefore use a separate small PWA P/N 89982800 for anti-bounce, which is mounted piggy-back and connected to the Console by four wires. Note that the encircled numbers 1,2,3,4 in the Anti-Bounce PWA on page 5-159 indicate connections to the GO switch and to the MANUAL INTERRUPT switch in logic drawing 89640501 sheet 4 on page 5-163 and in logic drawing 89640502 sheet 4 on page 5-167.

Cables

PWA P/N 89640300 (series A12 down) has an integral cable assembly which is soldered to the board. This is also true of PWA P/N 89987600. All other PWA P/N's connect to the CPU circuits through a plug-in cable assembly P/N 89893800.

TYPE IDENTIFIER (AB107,AB108)	CONSOLE PWA	LOGIC DRAWING	PAGE NUMBER
A17-A19	P/N 89985400	LD 89640500-B	5-145
A04-A12	P/N 89987600	LD 89640501-A	5-159
A13-A16	P/N 89987700	LD 89640502-A	5-164
C01-C03	P/N 89602069	LD 89640500-B	5-145
D01	P/N 89602069	LD 89640500-B	5-145

The description of the logic applies to all the above PWA part numbers.

EQUIPMENT	CONSOLE PWA P/N	LOGIC DRAWING	PAGE NUMBER
AB107/8-C/D,BT148-C/D	89602069	LD 89640500	5-145, 151, 154, 157
AB107/8-A, BT148-A	89985400	LD 89640500	5-145, 151, 154, 157
AB107/8-A, BT148-A	89987600	LD 89640501	5-160, 161, 162, 163
		LD 89982800	5-159 (anti-bounce PWA)
AB107/8-A, BT148-A	89987700	LD 89640502	5-164, 165, 166, 167
		LD 89982800	5-159 (anti-bounce PWA)

MAIN CIRCUIT BLOCKS

The principal blocks of the circuit are the pushbutton switches, data-bit selectors and control switches and indicators. The circuits and the signals are described in detail on pages facing the corresponding sheet of the logic diagram.

Pushbutton Switches (sheet 2)

The seven pushbutton switches allow the selection of one of the six internal registers or the Breakpoint register.

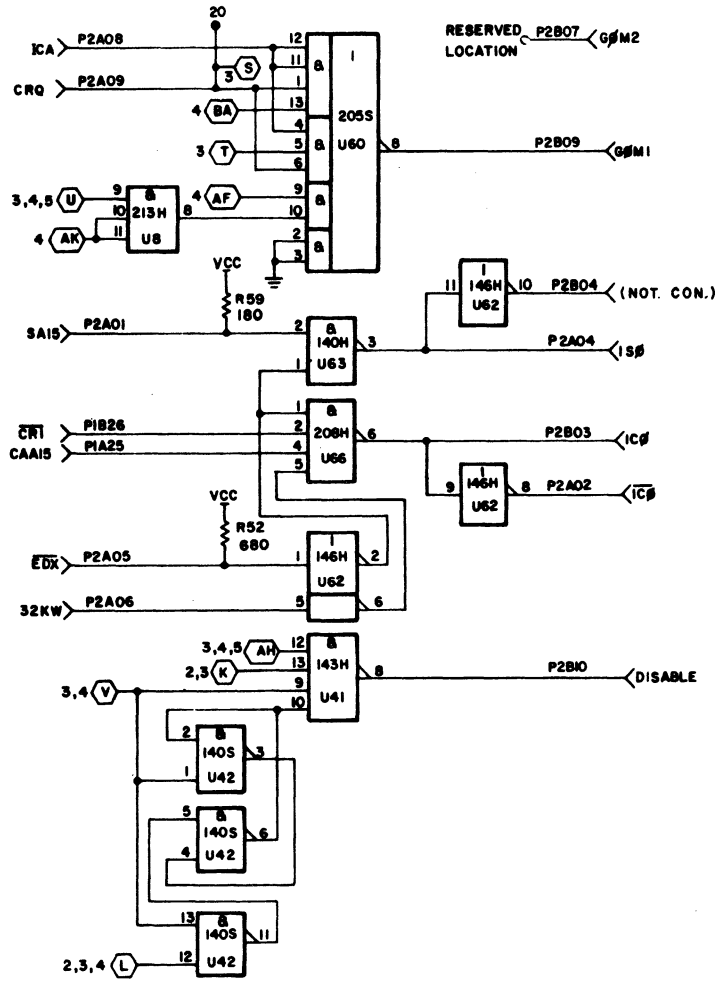
Data-Bit Selectors (sheet 3)

The data-bit selectors allow the manual input of data to each of sixteen bits of the computer from the programmer's console when the computer is stopped.

Control Switches and Indicators (sheet 4)

The control switches and indicators are the programmer's means of manual communication with the computer. They are described in the CONTROL DATA® 1784 Computer System Reference Manual, publication number 89633400.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM MEMORY CONTROL	CODE IDENT C	DWG NO 89619100	REV A
			SHEET 6	

"Pages 5-132 to 5-140 are unassigned".

MEMORY CONTROL

MEMORY CONTROL BANK ADDRESS (Drawing number 89619100, sheet 6)

Function: To determine which memory bank the CPU or DSA is addressing.

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	NAME OF SIGNAL	LOCATION SHEET	SQUARE
SA15	P2A01	DSA address Line 15	6	C-3
$\overline{EDX}$	P2A05	More than 32K of memory are available	6	B-3
$\overline{CRI}$	P1B26	CPU Index address 00FF	6	C-3
CAA 15	P1A25	CPU address line ALU15		
32KW	P2A06	32KW Switch on Mainframe front panel.	6	B-3
CRQ	P2A09		6	D-3
ICA	P2A08		6	D-3
Outputs:				
IC$\emptyset$	P2B03	Lower-bank CPU address correct	6	C-1
$\overline{IC\emptyset}$	P2A02	Lower-bank CPU address incorrect	6	B-1
IS$\emptyset$	P2A04	Lower-bank DSA address correct	6	C-1
$\overline{IS\emptyset}$	P2B04	Lower-bank DSA address incorrect	6	C-1

Description of Operation

The outputs of this circuit are connected via the back-plane of the computer enclosure to the appropriate CPU and DSA address function. The circuit decodes the CPU and DSA address information to determine if the memory bank is correctly addressed.

MEMORY CONTROL

Signal Functions (Drawing number 89619100, sheet 6, cont'd).

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
ICØ	U66/6	Lower-bank CPU address correct If any of U66/6 inputs are Low, the CPU requests access to the lower memory bank. Otherwise the memory request access to the upper memory bank.	6	C1
$\overline{\text{ICØ}}$	U6/8	Lower-bank CPU address incorrect. The inverse of ICØ.	6	C1
ISØ	U63/3	Lower-bank DSA address correct. If any of U63/3 inputs are Low, the DSA requests access to the lower memory bank. Otherwise the memory requests access to the upper memory bank.	6	C1
ISØ	U62/10	Lower-bank CPU address incorrect. The inverse of ISØ.	6	C1

Interconnections:

The Bank address is connected to the Access Selector via the back-plane wiring as follows:

Lower-memory bank:

ICØ ---- ICA

$\overline{\text{ICØ}}$ ---- $\overline{\text{ICA}}$

ISØ ---- ISA

ISØ ---- NOT CONNECTED

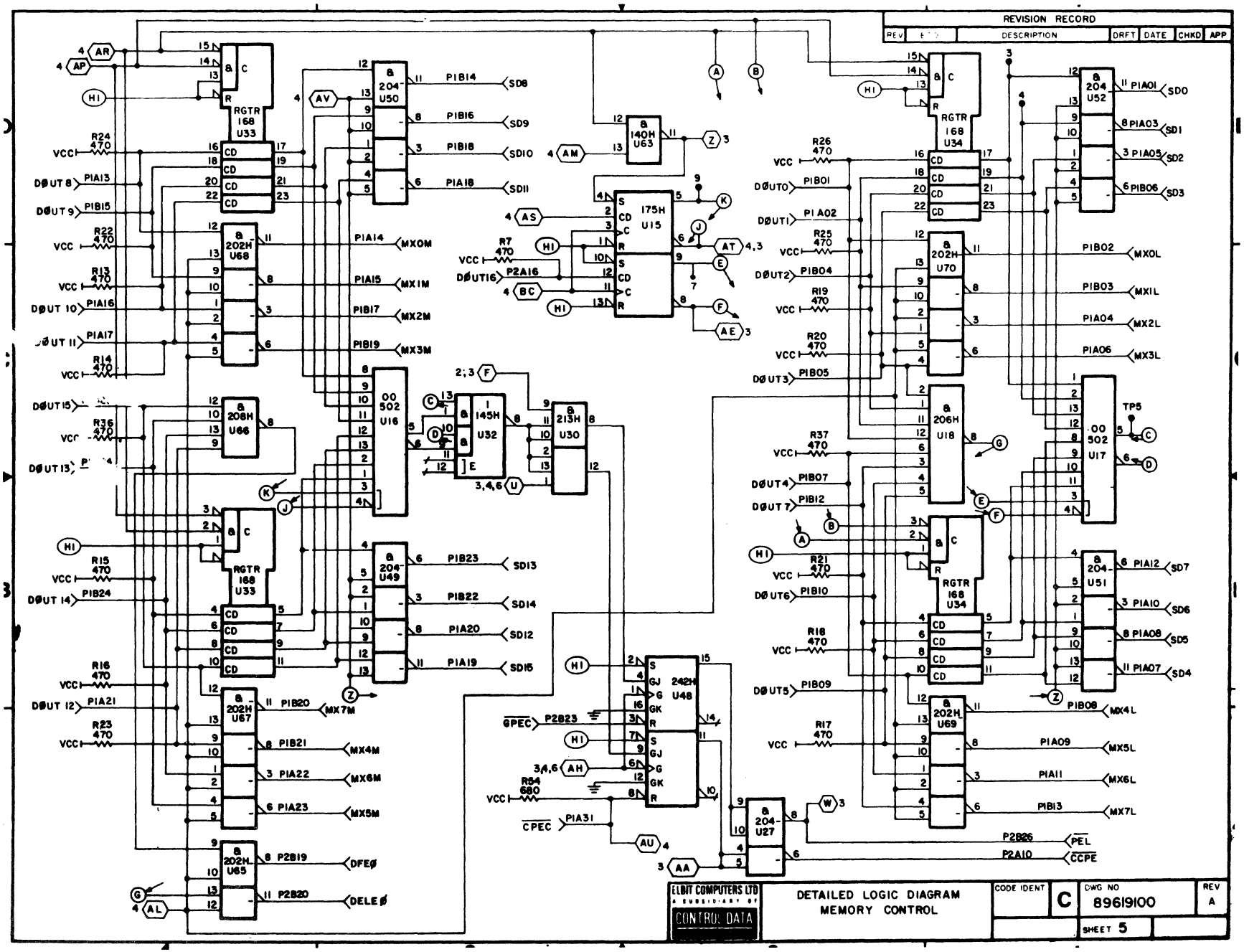
Upper-memory bank:

ICØ ---- $\overline{\text{ICA}}$

$\overline{\text{ICØ}}$ ---- ICA

ISØ ---- NOT CONNECTED

$\overline{\text{ISØ}}$ ---- ISA


REVISION RECORD
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APP
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
MEMORY CONTROL
CODE IDENT
C
DWG NO
89619100
REV
A
SHEET 5
RGTR 168 U33
RGTR 168 U34
RGTR 168 U34
204 U50
204 U52
204 U49
204 U51
204- U27
140H U63
175H U15
145H U32
213H U30
242H U48
00 502 U16
00 502 U17
202H U67
202H U68
202H U70
202H U69
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PIA21
PIB01
PIB04
PIB07
PIB12
PIB10
PIB09
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PIA31
P2B23
P2B26
P2A10
PIB14
PIB16
PIB18
PIA18
PIA14
PIA15
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PIB05
PIA12
PIA10
PIA08
PIA07
PIB08
PIA09
PIA11
PIB13
SD8
SD9
SD10
SD11
MX0M
MX1M
MX2M
MX3M
SD13
SD14
SD12
SD15
MX7M
MX4M
MX6M
MX5M
DFEØ
DELEØ
SD0
SD1
SD2
SD3
MX0L
MX1L
MX2L
MX3L
SD7
SD6
SD5
SD4
MX4L
MX5L
MX6L
MX7L
PEL
CCPE

MX17 [P1A26]
This signal is connected to CXD and D17 from the Memory Address card (P1B27). It sends the status of the protect bit to the CPU on read and write cycles. If the CPB signal is active, MX17 will be low. If the SPB signal is active, MX17 will be high. If the CPB and SPB signals are inactive, and the memory location is unprotected, MX17 will be low. If the CPB and SPB signals are inactive, and the memory location is protected, MX17 will be high. For MX17 truth table see table at end of this part.

$\overline{\text{CVIOT}}$ [(L) P1A28]
This signal is connected to CXD and Protect Fault. When a protect fault occurs during a CPU cycle, this signal is low, otherwise it is high. The signal is high during a read cycle because protect fault only occurs on write cycles.

SXD [U20/7]
This signal is active high for 5 clocks of a DSA cycle, beginning at clock 8.

SXRD [U21/6, 8]
This signal is active high for 5 clocks of a DSA read cycle only, beginning at clock 8.

SD00-SD15 (H)
These signals are connected to SXRD and the data out latches after DØUT lines. They transmit stored-buffered memory data to the DSA on read cycles only. The true state of this data is active high.

Data to the DSA is transmitted by powerful open collector 2-input NAND buffers. Pull-up resistors are located on the DSA lines. These NAND gates are opened by one of two signals, SXD or SXRD. All data to the DSA lasts for 4 clocks beginning at clock 9.

SD16 (odd) [P2A21]
This signal indicates the parity of data read from or written into memory of the DSA lines. It is connected to SXD and a parity selector U14/6.

SD16 is active such that the sum of the data on SD00-SD17 (18 bits) will be odd. During a read cycle, SD16 is determined by the parity register U15/8. During a write cycle, SD16 is determined by D16 P2B06 from the Memory Address card.

SD17 [(L) P2A18]

This signal indicates the status of the protect bit during a DSA read or write cycle. It is connected to SXD and the protect register U15/6. If the location in memory is protected, SD17 is low, otherwise SD17 is high.

SVIØ [(L) P2B24]

This signal is connected to SXD and the Protect Fault. When a Protect Fault occurs during a DSA cycle, this signal is low, otherwise it is high. This signal is high during a read cycle because protect fault can only occur during write cycles.

TRUTH TABLE FOR MX17

CPB	SPB	LOCATION PROTECTED	MX17
H	X	X	L
X	H	X	H
L	L	L	L
L	L	H	H

NOTES: H = High, L = Low, X = irrelevant.

Parity error is indicated by the data registers and parity checker circuit.

Because the DØUT lines are stable on clock 8, and because DØUT may change after clock 8 on a write cycle, the data must be stored on clock 8.

Between clocks 6 - 8 the data latches U33, U34 are opened. The first 16 bits of data pass through these latches during this time, and enter the parity checker. The parity checker for the first 16 bits (U16, U51, U32) is relatively slow (100 nsec). It requires stable data to be present before clock 8 and to continue until clock 10 in order to allow the parity checker to be stable by clock 10.

Bit 16, (DØUT16), the Parity bit, and bit 17 (DØUT17), the Protect bit, are stored in D-flip-flops (U15) on clock 8. The outputs from U15/8, 9 and U15/5, 6 do not have to stabilize until after clock 8 because the parity checker is relatively fast (50 nsec) for these two bits.

The parity checker is designed so that if the binary sum of DØUT00÷DØUT17 is even, the parity checker output U32/8 will be high indicating a parity error. Otherwise U32/8 will be low (i.e. parity error did not occur).

The DØUT lines come from the open collector sense amplifier outputs on the memory modules. The pull-up resistors are located on the DØUT lines in the MC assembly. Only one of the possible eight memory modules sense-amplifier outputs can be active, as determined by the module selector MDX and the signal STRØBE.

Protect Fault [(H) U28/6] - refer to sheet 3

Protect fault [condition 1] occurs when an unprotected instruction (U28/5) attempts to write (U28/3) into a protected location (U28/4). Protect fault U28/6 is active high. The protect register is preset (U15/4 low) on clock 5 to deactivate U28/4. This prevents unnecessary spikes between clocks 6 - 8 when the other two inputs are stable and CXD or SXD are stable. It also prevents unnecessary spikes on SD17, the DSA protect bit. Protect fault is valid between clocks 8 - 5 after the protect register is stable.

Note that the memory system recognizes protect fault condition 1 only. Conditions 2 and 3 are conditions within the CPU and are not related to the memory or DSA operations.

Both the parity flip-flop clock (U15/11) and the protect flip-flop clock U15/3) are positive edge triggered on clock 8.

Data to the CPU (MX) and to the DSA bus (SD) is transmitted by high speed open collector 2-input NAND gates. Pull-up resistors for these signals are located in the CPU. These NAND gates are opened by the signals, CXD (CPU) or CSRD (DSA). All data to the CPU is valid at clock 9.

CXD (U31/6,8) CXRD [U13/6,8] - signal origin: sheet 4.

These signals are active high between clocks 6-10 for CPU cycles only. They are to gate the memory data for CPU cycles.

MX00-MX15 (H)

These signals are derived from the DØUT lines gated by CXRD. They transmit buffered memory data to the CPU during read cycles. The true state of this data is active high.

DELEØ [(L) P2B20]

This signal is sent to the CPU on a read cycle only. The signal is low when MX00÷MX07 are all at logic low.

DFEØ [(L) P1B20]

This signal is sent to the CPU on a read cycle only. The signal is low when MX12-MX15 are all logic low.

MPRY [P1A27]

This signal is PAR (P1B28) from the Memory Address assembly gated by CXD. It is a special parity bit to the CPU on write cycles (bit 16). If the sum of the 16-bit data sent from the CPU to the memory is even, MPRY is low. Otherwise it is high. Information on MPRY during CPU read cycles is meaningless and is not used by the CPU.

MEMORY CONTROL

MEMORY CONTROL DATA OUTPUT LINES (Drawing number 89619100, sheet 5)

Function:

To transmit data to the CPU and to the DSA

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN		LOCATION SHEET	SQUARE
$\overline{E}$	[U11.7]	Clock signals		
$\overline{B}$	[U10/7]			
$\overline{CMDR}$	P2B02	$\overline{E \cdot B}$	4	B-1
clock 6	[U63/11]		5	D-2
$\overline{GPEC}$	P2B23		5	A-3
D16	P2B06		3	B-1
D17	P1B27		4	D-4
PAR	P1B28	Parity	4	D-4
CX	[U7/8]			
$\overline{RX}$	[U24/6]			
F	[U45/6]	End of cycle (clock signal)		
clock 7	[U28/2]			
DOUT00+DØUT17	18 locations	Memory data output		
Outputs				
$\overline{CCPE}$	P2A10	CPU cyclic parity error	5	A-1
$\overline{PEL}$	P2B26	General parity error	5	A-1
$\overline{CPEC}$	P1A31		5	A-3
DELEØ	P2B20	MX00•MX01•MX02 ..... MX07 = 0	5	A-4
DFE0	P2B19	MX12•MX13•MX14•MX15 = 0	5	A-4
MPRY	P1A27	Parity information to CPU	4	D-3
MX17	P1A26	Protect bit status to CPU	4	D-3
CV101	P1A28	Protect fault	4	A-3

MEMORY CONTROL

Outputs (cont'd) (Drawing number 89619100, sheet 5, cont'd).

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
SD16	P2A21	Parity bit for DSA data	4	D-2
SD17	P2A18	Protect bit for DSA data	4	D-2
SVIØ	P2B24	Protect fault on DSA cycle	4	D-2
MX00-MX15	16 locations	Data to CPU		
SD00-SD15	16 locations	Data to DSA on read cycles		

Circuit Description

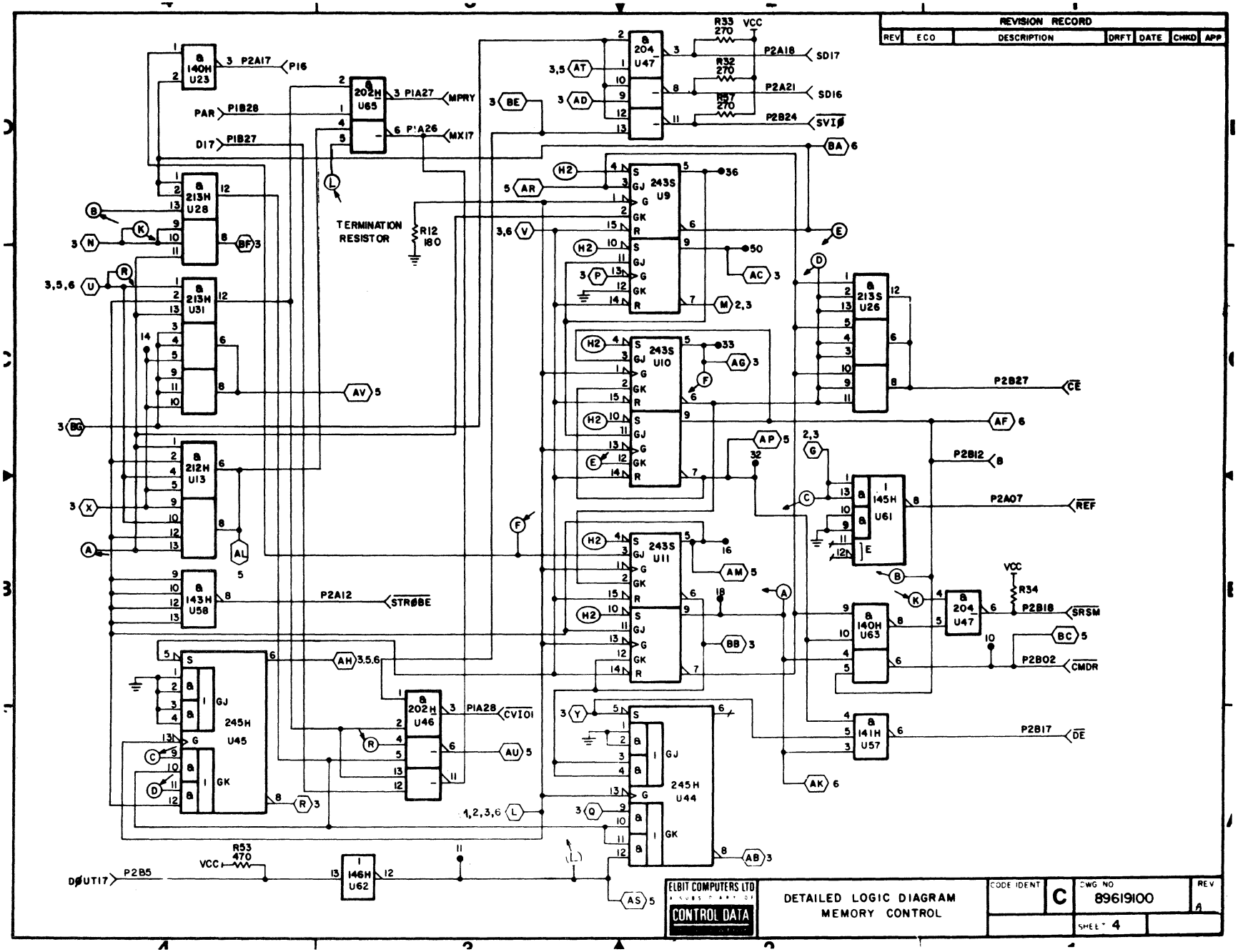
All the Data lines are open collector. Corresponding bits are connected to the same bus line for multi-bank operation.

Parity Error Checking is performed on CPU and DSA read and write cycles. If a parity error is detected, it is an indication that the memory is not working correctly. Parity error is detected when the summation of DØUT00-DOUT17 (data out bits 00-17) is not an odd number.

There are two types of indicators for parity error detection.

1. $\overline{\text{PEL}}$ [P2B26]
   General parity error: a parity error was detected. The J - K register (U48) continues to be active until U48/3 is cleared by the CPU signal GPEC(P2B23). The J input, U48/4 will detect a parity error, excluding the refresh cycle (RX U30/9 is not low) if U32/8 is high at clock 10. The clock (U44/1) is negative edge triggered at clock 10 by the F-register (U45).

2. $\overline{\text{CCPE}}$ [P2A10]
   CPU Cyclic Parity Error: a parity error was detected on the last CPU cycle. The J - K register (U48) continues to be active until $\overline{\text{CPEC}}$(P1A31) (a multibank output) clears U48/8 on clock 7 on the next CPU cycle. The J input, U48/9 will detect a parity error only on a CPU cycle (CX U30/12 is high if U32/8 is high at clock 10. The clock (U48/1) is negative edge triggered at clock 10 by the F-register output.


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
TERMINATION RESISTOR
R12 180
R33 270
R32 270
R57 270
R53 470
R34
VCC
P2A17
P16
PAR
P1B28
D17
P1B27
MPRY
MX17
P1A27
P1A26
P2A18
SD17
P2A21
SD16
P2B24
SVI
P2B27
CE
P2B12
P2A07
REF
P2A12
STROBE
P2B16
SRSM
P2B02
CMDR
P2B17
DE
PIA28
CVIOI
DOUT17
P2B5
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
MEMORY CONTROL
CODE IDENT
C
DWG NO
89619100
REV
A
SHEET 4

MEMORY CONTROL (Drawing number 89619100, sheet 3, cont'd).

R/WREG [(H) U44/8]

This register provides timing to the Read/Write (R/W) signal in memory. It also determines if the R/W signal should be activated.

This register is negative edge tirggered and is connected to the ØSC (U44/13). It is activated on clock 8 (U44/8 goes high) only if one or both of the AND-OR K inputs is active on clock 7. U44/10, 11 is active only on clock 7. If the instruction from the PROTECTREG is protected (U44/9 high), or if the protect bit from the memory location addressed was inactive (U44/12 high), then U44/8 can activate on clock 8. Thus, a write cycle will not occur if the location in memory is protected and the instruction is unprotected. The only other condition necessary for the R/WREG to activate is that the WRITEREG (U44/5) indicate that the memory cycle is a write cycle. If the memory cycle is a read cycle, the R/WREG is preset, (U44/5 is active low) and U44/8 will remain low on clock 8. If the R/WREG activated on clock 8, it will deactivate on clock 11 after $\overline{D}$ (U44/3, 4) activates the J input between clock 10 - 5. The J and K inputs can never be active simultaneously because of this timing.

Read/Write: R/W [(L) P2A20]

The R/W signal activates the R/W signal within the memory. If activated the R/W signal will go high between clocks 8 - 11 (U59/10 high). The R/W signal cannot activate if the $\overline{\text{INHIBITREG}}$ is active (U59/9 low), or if the system is in LPDR operation (Normal, U59/13 low).

$\overline{DE}$ [(L) U57/6]

$\overline{DE}$ activates the data-in lines on the Memory Address assembly. These lines transmit data to the memory on write cycles. It is desirable to activate these lines by clock 8 because these lines may create noise on the data out lines from the memory and interfere with parity checking on a Read/Write cycle. $\overline{DE}$ goes low on clock 8 when (U57/4) goes high. $\overline{DE}$ goes high on clock 12 which is approximately 50 nanoseconds after

register $\overline{E}$ went low as determined by the RC delay on U57/3.

The $\overline{DE}$ signal needs to be active until after the R/W signal within the memory has completely deactivated. If the WRITEREG register indicates that the memory cycle is a read cycle (U57/5 is low), $\overline{DE}$ will not activate.

WRITE CONTROL SIGNALS

Function

The memory system includes a protect system. The primary purpose of this feature is to protect the program in foreground from being destroyed by careless programming, or faulty memory operation. The protect feature is part of the write system within the memory.

The read/write and protect status of the memory cycle is determined by multiplexer-selector U64. The following table shows its input and output signals.

Input Controls		Outputs		Cycle Selected
RX (Pin 3)	SX (Pin 13)	WRITE cycle (Pin 2)	Unprotected Instruction (Pin 15)	
L	L	WE	$\overline{\text{PRTM}}$	CPU cycle
L	H	SWRITE	$\overline{\text{SPI}}$	DSA cycle
H	L	Low	Low	Refresh cycle
H	H	irrelevant	irrelevant	---

Signal Description

The following paragraphs describe each signal in detail: the signal name heads each paragraph together with the integrated circuit and pin number where it appears. The letter (H) and (L) indicate whether the signal at the corresponding pin is active High or active Low.

WRITEREG[(H) U12/5, (L) U12/6]
This register is positive edge triggered. On clock 6 it stores both during a read cycle (pin 5 low) and a write cycle (pin 5 high). Pin 6 is the inverse of pin 5. U12/4 (active low) is preset (pin 5 goes high) on clock 4. This is to prevent unnecessary spikes on the data out lines to the DSA and CPU lines.

MEMORY CONTROL (Drawing number 89619100, sheet 4, cont'd.)

PROTECTREG (H) U29/8, (L) U29/9

This register is positive-edge triggered. On clock 6 it stores whether the cycle is a protected instruction (U29/8 high) or an unprotected instruction (U29/8 low). P9 is the inverse of pin 8. U29/13 (active low) is cleared (P8 goes high) when the PRTSW (Protect Switch, P2B01) is low. In this case (protect switch low) all instructions appear as protected within the memory system. The protect switch is situated on the programmer's console (front panel)

$\overline{\text{INHIBITREG}}$ [(L) U29/5]

This register is positive edge triggered. On clock 6 it stores provided either one of two conditions occurred:
The first condition is that a parity error occurred on either memory bank while the instruction was unprotected.
The second condition is that during a CPU cycle a parity error occurred in the selected memory location and that the SPB or CPB (Set or Clear Protect Bit) is activated on this memory cycle.
The two conditions may be summed up: when an attempt is made to execute CPB or SPB instructions when a parity error exists in the selected memory location.

The procedure for recognizing condition 2 works because before CPB or SPB, the program must read from the location in memory, and immediately afterward perform the CPB or SPB in that same location.

If the $\overline{\text{INHIBITREG}}$ register recognizes either condition 1 or condition 2 or both conditions, U29/5 will go low. Otherwise U29/5 is high.

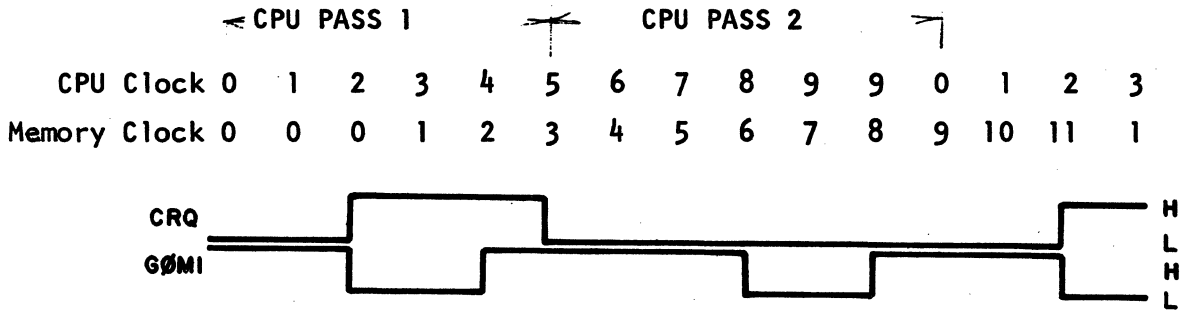
U29/4 (active low) is preset [U29/5 goes high when the PRTSW (Protect Switch, P2B01) is low]. When the protect switch is low, the protect feature of the system appears to be disabled.

3) The memory system is processing the CPU request, but has not yet reached clock 0. The combination of the following conditions define this:
the memory is processing a CPU cycle between clock 6-11(U60/10), and has not yet passed clock 8 because register B (U60/9(is active.

Two memory systems are used in systems having more than 32K word memories. A second signal (GØM2: P2B07) is employed in the expansion memory system; it is basically identical to GØM1 in its function.

Further explanation of the CPU memory request system.

Schottky TTL circuits are employed in this system because timings must remain synchronized with the oscillator. The CPU transmits the CPU request signal CRQ between its clock 2-5 of pass 1 only. Also, the signal GØM1 must be high for one clock at the end of a CPU pass, which is why GØM1 is released before memory system clocks 3 and 9. The timing relationships are shown below.



MEMORY CONTROL (Drawing number 89619100, sheet 4,6, cont'd).

Basic Control signals to the DSA

SRSM (L) P2B18

The SRSM synchronizes the DSA with the memory. Because the DSA is an asynchronous device, the SRSM does not have to be a fast signal. The SRSM appears at an open collector gate, and can be used as a wired-OR function. In multibank memory operation the SRSM of both lower and upper banks are connected together. This is an active low signal; normally the line will be high. When one of the memory systems wants to activate the SRSM line, it merely activates its own SRSM signal. The entire SRSM is then forced low until this same bank deactivates its SRSM signal.

When SRSM is high, at the beginning of a DSA cycle, it informs the DSA device that the memory has not accepted the DSA address, and that the DSA should continue to transmit the address.

When SRSM falls, it informs the DSA device that it has accepted the DSA request and address. The DSA should immediately clear the DSA request and address lines, and it can send a new DSA request and address if desired.

Further, for a DSA write-into-memory cycle, the low SRSM signal informs the DSA that the memory has not yet accepted data, and that the DSA should continue transmitting data to the memory.

Also, for a DSA read-from memory cycle, the rising edge of the SRSM signals informs the DSA device that data from the memory is now valid.

The SRSM is low between DSA cycle clocks 3-11.

Refer to DSA Timing Specification in Section 4 and the Input/Output Specification Manual.

CXP (L) (P2B16) SXP (L) (P2A11) HØLD (H) (P2B14)

These three signals provide initiate and hold signals for the selector/latches on the memory address assembly.

Before a memory cycle begins, HØLD is High to hold the old memory address. SXP and CXP are also high. When the CX access selector activate at clock 1, CXP goes low, which allows a new ALU address into the MA address selectors. The CXP signal is also fed into U23/10, so U23/8 goes high and HØLD (U42/8) goes low. This overlap of CXP and HØLD is important, because it allows the outputs of the MA address selector/latches to change only once. On clock 2.5 the signal AP5 (U58/4,5) goes low and HØLD goes high. This holds the address in the MA address selector/latches. The HØLD signal and AP5 are fed into a NAND gate whose output (U23/11) causes CXP to go high. This overlap of HØLD and CXP prevents the MA address selector/latch from changing during this transient period. In other words, CXP and HØLD behave like the Q and $\overline{Q}$ of an R-S flip-flop; except HØLD is $\overline{Q}$ inverted.

For a DSA cycle, SXP behaves like the CXP signal during the CPU cycle. During the DSA cycle, CXP always remains high.

HØLDW (H) (P2A24)

The MA address selector/latches for the kiloword decoder do not have the same requirements as the other address bits. This decoder can have transients when the Disable signal is inactive between clocks 1 - 1.5. However, it is desirable to have the kiloword decoders completely decoded before the Disable signal activates at clock 1.5. For this reason, a special hold signal called HØLDW is used for the MA kiloword decoder. It is the signal AP5 inverted, and is active high between clocks 2.5 - 11. No time is wasted in the kiloword decoder when CXP goes low at clock 1 because HØLDW is already low on clock 1.

MEMORY CONYROL (Drawing number 89619100, sheet 4,6, cont'd).

Basic control signals to the CPU

GØM1 (H) P2B09

The CPU and memory are both synchronous devices using the same oscillator. However, the memory system is not always ready for the CPU because it may be performing DSA or Refresh cycles. When this happens, it is important to stop the CPU.

The CPU is a two pass machine. During pass 1 the ALU calculates address information and holds this information at the end of pass 1. During pass 2 the ALU calculates or receives data information and holds or accepts this information at the end of pass 2. Both ALU passes are 5 clocks long; therefore pass 1 and pass 2 together take 10 clocks. This causes a discrepancy, because the CPU memory cycle is 11 clocks long. When the CPU is performing a memory request, it must be stopped for one clock so that both the CPU and CPU memory cycle will have the same number of clocks, namely 11.

The CPU is stopped by the memory system with the signal GØM1. If this signal is low at the end of CPU memory request pass 1 or pass 2, it will stop at the end of that pass. Further, the memory system requires address information between CPU memory cycle clocks 1-3 and data information between clocks 3-9. The three conditions for lowering the GØM1 signal can now be defined.

1) The memory system is busy with a DSA or Refresh cycle. The combination of the following three conditions define this:
   if the memory is not processing a CPU cycle ($\overline{CX}$: U60/5),
   the CPU requested memory access (CRQ: U60/6),
   the address is in this memory bank (ICA: U60/4).

2) The memory system is processing the CPU request, but has not yet reached clock 3. The combination of the following conditions define this:
   the CPU requested memory CRQ (U60/1) for this memory bank ICA (U60/11, 12),
   the memory cycle has not passed clock 2 because register A (U60/13) is active.

MEMORY CONTROL (Drawing number 89619100, sheet 4,6, cont'd.)

Circuit description:

DISABLE (L) P2B10

Disable activates (low) when 1P5 (U41P10) goes high at clock 1.5. Disable deactivates when $\overline{F}$ (U41P12) goes low. One clock after $\overline{F}$ goes low, BUSY (U41P9) goes low. Then $\overline{F}$ goes high. When the next access selector activates, BUSY goes high. If LØADRA (U41P13) is low, Disable is inactive. LØADRA is used for LPDR operation.

CE (L) P2B27

This signal falls at clock 4 when register $\overline{C}$ falls, and rises when register $\overline{E}$ rises.

REF (L) P2A07

This is a 2-2 AND-OR gate. REF is low during refresh cycles because U61P1,13 is connected to RX. REF is low for DSA and CPU cycle until clock 3 when register $\overline{B}$ (U61P10) falls, and REF remains high until clock 11 when register $\overline{E}$ (U61P9) rises.

STROBE (L) P2A12

This signal is the inverse for register D.

Because Disable and CE are critical timing signals going to eight memory modules, they employ extra powerful buffers to be less noise susceptible. STRØBE is extra powerful because each of eight memory modules uses 2.5 TTL logged units from this signal.

Basic Control signals during refresh cycles.

SXA (L) P2B08

This active low signal informs the Memory Address (MA) assembly that a DSA cycle is being processed. It is the inverse of SX, active between clocks 1-11.

P16 (L) P2A17

Active low signal opens the 16 bit parity latch on the MA assembly; activates at clock 7 when $\overline{A}$ (U23/2) rises until clock 9 when C (U23/1) falls.

B (L) P2B12

Active low signal clocks the protect bit (bit 17) register on the MA assembly. Activates at clock 7.5 when ØSC rises. Deactivates at clock 8 when ØSC falls. B cannot activate during other time intervals.

CMDR (L) P2B02

Active low signal provides timing to the MA CPU data in memory latch. CMDR activates at clock 4 when E (U63/5) goes high and activates at clock 8 when B (U63/4) goes low.

MEMORY CONTROL (Drawing number 89619100, sheet 4,6, cont'd.)

Introduction

The Control unit processes a collection of control signals and can be divided into two parts:

1. Basic Control Signals

   Control signals necessary for all types of memory cycles, i.e., read or write cycles in protected or unprotected locations.

2. Write Control Signals

   Control signals for write memory cycles used with the protect system.

Note: For timing signals refer to Memory Control Timing (sheet 4).

BASIC CONTROL SIGNALS

DISABLE (L) P2B10

The falling edge of this signal activates the precharge signal in the memory. The falling edge starts at clock 1.5, giving the memory system half a clock period to select one of four kilowords on each memory card. As each kiloword has its own control signals (precharge, cenable, R/W) only one kiloword will be activated. Since the precharge signal consumes most of the memory power delaying the disable until clock 1.5 conserves power consumption without imposing critical set-up or hold time restrictions on other memory signals. The rising edge of the disable signal deactivates the cenable (cell enable signal) in the memory. This occurs at clock 10 for DSA and CPU cycles, and clock 8 for Refresh cycles.

CE (L) P2B27 (Cenable)

The falling edge of this signal at clock 4 activates the cenable signal in the memory. Also, within the memory, the canable signal forces the precharge signal to deactivate. The crossover of the cenable-active precharge-inactive is performed on the memory card (rather than the memory control card) because of critical overlap times required by some memory chip manufacturers. The CE signal deactivates at clock 11 for DSA and CPU cycles, and clock 9 for Refresh cycles. It is important to have the CE signal deactivate one clock after the Disable signal deactivates. If the CE signal deactivates earlier, the precharge signal may reactivate at the end of a memory cycle.

REF (L) P2A07

The REF signal blocks the module selector (MDX#) within the memory card. During Refresh cycles the REF signal is always activate low because a Refresh cycle must refresh all of the memory modules. During DSA and CPU cycles, this is low during clock 1 to 3 because the module selector decoding is slow and not stable during this time. The REF signal goes high between clock 3-11. For all unselected memory modules during this time, the precharge signal deactivates one clock before the Cenable signal, and the cenable with the memory card never activates. Only in the one memory module selected by the module selector does the precharge-cenable sequence continue.

STRØBE (L) P2A12

This signal is active low between clocks 5-10 for DSA and CPU cycles, and clock 5-9 for Refresh cycles. It enables the data out sense amplifiers within the memory card. It also deactivates the Read/Write (R/W) signal (see R/W signal later in this section) slightly faster than the cenable signal, helping meet an end of cenable - end of R/W specification for the memory chip of some manufacturers. This signal performs no useful function during refresh cycles.

MEMORY CONTROL (Drawing number 89619100, sheet 3,4,6).

MEMORY CONTROL BASIC CONTROL SIGNALS

Function: To provide all control signals to the memory, memory address, CPU and DSA devices.

Note: The following signal lists include a number of signals not directly connected to the circuits described here.

Inputs

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
PRTSW	P2B01		3	A-1
$\overline{\text{PRTM}}$	P1B30		3	D-2
$\overline{\text{SPI}}$	P1B29		3	C-2
$\overline{\text{WE}}$	P1A30		3	D-2
$\overline{\text{SWRITE}}$	P1B31		3	C-2
ØSCA	U38/6	Oscillator buffered		
CRQ	P2A09	CPU cycle Request	6	D-3
ICA	P2A08		6	D-3
PBC	P2A22		3	A-2

Outputs

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
GØM1	P2B09	$\overline{ICA \cdot CRQ + CX \cdot B \cdot E}$	6	D-1
GØM2	P2B07		6	D-1
DISABLE	P2B10	$\overline{LOADRA} \cdot \overline{F} \cdot BUSY \cdot IP5$	6	B 1
$\overline{SXA}$	P2B08	DSA active ($\overline{SX}$)	3	A-2
R/W	P2A20	Read/Write	3	C-2
$\overline{CXP}$	P2B16	$CX \cdot \overline{SX} \cdot \overline{HØLD} \cdot \overline{AP5}$	3	C-2
HØLDW	P2A24	AP5	3	C-2
HØLD	P2B14	$\overline{AP5}$ [SX + CX]	3	B-2
$\overline{SXP}$	P2A11	$SX \cdot \overline{HOLD \cdot AP5}$	3	C-2
$\overline{SRSM}$	P2B18	$\overline{SX \cdot [D + B]}$ DSA Synchronizing signal	4	B-1
REF	P2A07	$\overline{RX}$ [B + E]	4	B-1
$\overline{CE}$	P2B27	$\overline{\overline{E} \cdot \overline{C}}$ = C + E, (Cenable)	4	C-1
$\overline{DE}$	P2B17	Data-line Enable	4	A-1
P16	P2A17	$\overline{\overline{A} \cdot C}$	4	D-4
B	P2B12	Second Counter stage	4	B-1
$\overline{STRØBE}$	P2A12	Timed by D ($=\overline{D}$)	4	B-3
$\overline{CMDR}$	P2B02	$\overline{B \cdot E}$	4	B-1
CVI01	P1A28	(See sheet 5)	4	A-3

Detailed Circuit Description

The BUSY signal clears the five-stage ring-counter (U9, U10, U11). When this signal goes high the counter is free to run. Flip-flop A (U9/5) will be the first to toggle because outputs E and $\overline{E}$ are inversely connected to the J and K terminals of the A flip-flop relative to the other J and K connections. The ripple-through process shifts the toggling along the counter on the appearance of each clock pulse. The counter is clocked by the ØSC signal, the flip-flops being triggered on the negative going edge of the signal. The J input activates the flip-flops, the K input and the Clear input (Busy signal) deactivates them.

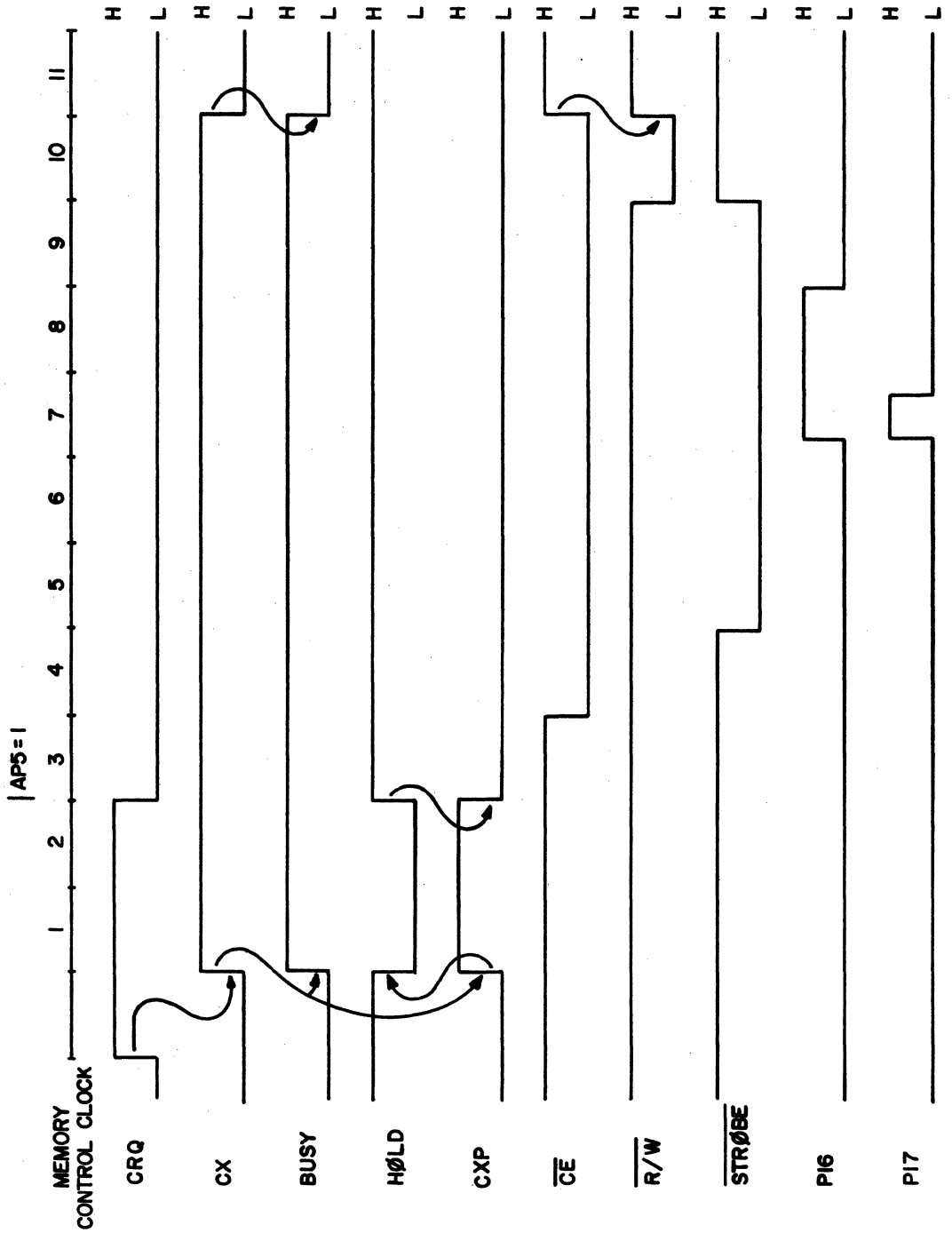
The K input activates Register F (U45). During DSA or CPU cycles, this register activates after inputs U45/11 ($\overline{C}$), and U45P12 (D) are activate. However, during Refresh cycles this register activates two clock cycles after inputs U45/9 (RX) and U45/10 ($\overline{A}$ and B) are active. The J inputs are grounded, so only the Preset input U45/5 (BUSY) can deactivate the Register. The clock U45/13 is connected to the ØSC and is negative edge-triggered.

Half of U9 (U9/7,9) is not part of the ring counter; it generates the timing signal AP5. It is activated on the half clock after the J input U9/11 is active. The K input (U9/12) is grounded, so this register can only be deactivated by the clear input U9/14 (BUSY). This register is negative-edge triggered, but because it is connected to $\overline{ØSCA}$ it operates between clock cycles.

The IP5 register consists of two NAND gates wired as on R-S flip-flop. When inputs U42/1,5 are high, the flip-flop holds its state. Both inputs will never be low at the same time because the BUSY signal is common to both of them but inverted in U42 5. After an access register activates, U42/1 (BUSY) goes high. On the half clock after the access register went high, U42/12 (ØSC) goes high, and U42/13 (BUSY) is high. U42/5 goes low, activating the IP5 flip-flop. At the end of the timing sequence, the BUSY signal (U42/1) goes low, deactivating the flip-flop. Since IP5 is connected to $\overline{ØSCA}$ and activates when $\overline{ØSCA}$ is high,

the IP5 activates during a half-clock.

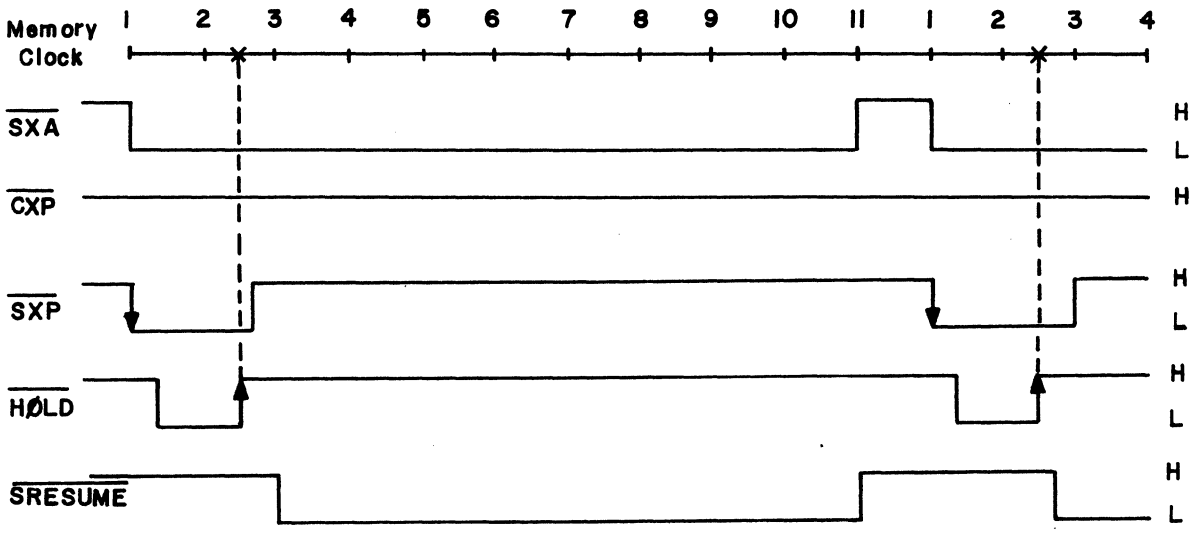
All the register, A, B, C, D, E, F, AP5 and IP5 are super high speed Schottky TTL devices to meet specifications in the high speed (600 nsec) memory system.



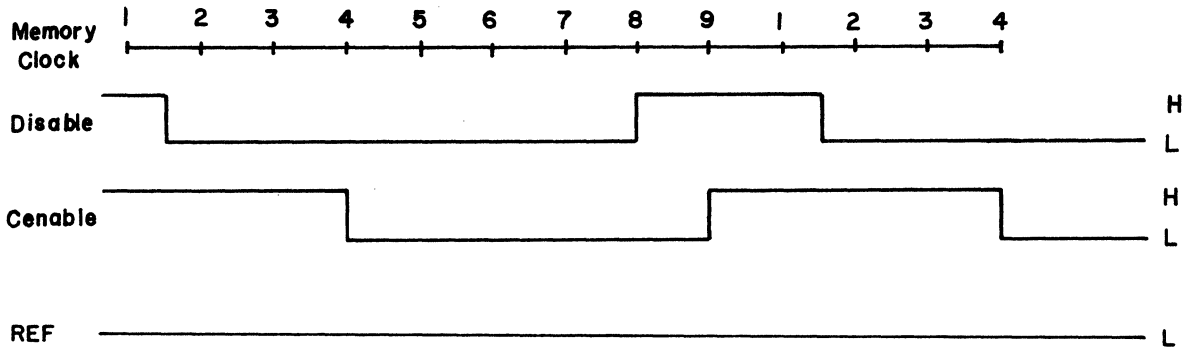
MEMORY CONTROL (Drawing number 89619100, sheet 4)

MEMORY CONTROL TIMING

Control Signal Diagram for DSA Cycles



Control Signal Diagram for Refresh Cycles



The advantage of the full ring counter is that only one of the five major timing signals (A, B, C, D, or E) can clock a cycle. Any timing sequence can be chosen from this pattern by simply ANDing or ORing one or two timing signals since only one timing signal can change at any time.

On clock 10 of DSA and CPU cycles register F (End of cycle) activates. This deactivates the Access Selector one clock later, and the Busy signal will fall, clearing the timing circuit.

There are two special purpose timing signals, IP5 and AP5. Both of these timing signals activate on half clocks (in between usual clock edge triggering) instead of full clocks. Both of them are cleared by the Busy signal. IP5 activates between clock 1 and 2 (referred to as clock 1.5). AP5 activates during clock 2 and 3 (referred to as clock 2.5).

For a Refresh cycle, the timing sequence is shortened two clock cycles. A Refresh cycle is shorter because data is neither read nor written during this cycle, so time need not be allowed for data from the memory to stabilize. The Refresh cycle is shortened by activating register F (End of cycle) on clock 8 instead of clock 10. When the Busy signal falls during the next clock, all timing signals are cleared.

The J input activates the Timing circuit registers. The K input or clear deactivates them.

A hazard may arise in the Refresh cycle timing sequence as registers D and E are asynchronously cleared. Any timing function combining registers D and E may have spikes in it. Care was taken not to use function D and E (or their inverses or combinations) in places where spikes might impair the behavior of the system.

MEMORY CONTROL TIMING (Drawing number 89619100, sheet 4)

Function: To provide all timing signals within the memory system.

Inputs

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	NAME OF SIGNAL	LOCATION SHEET	LOCATION SQUARE
$\overline{\text{ØSC}}$	[U56/6,8]	Clock	3	D4
$\overline{\text{ØSCA}}$	[U38/6]	Oscillator buffered	3	C1
BUSY	[U38/12]	One of access selectors active	3	C1
RX	[U24/8]	Refresh cycle selector	3	D3

Outputs

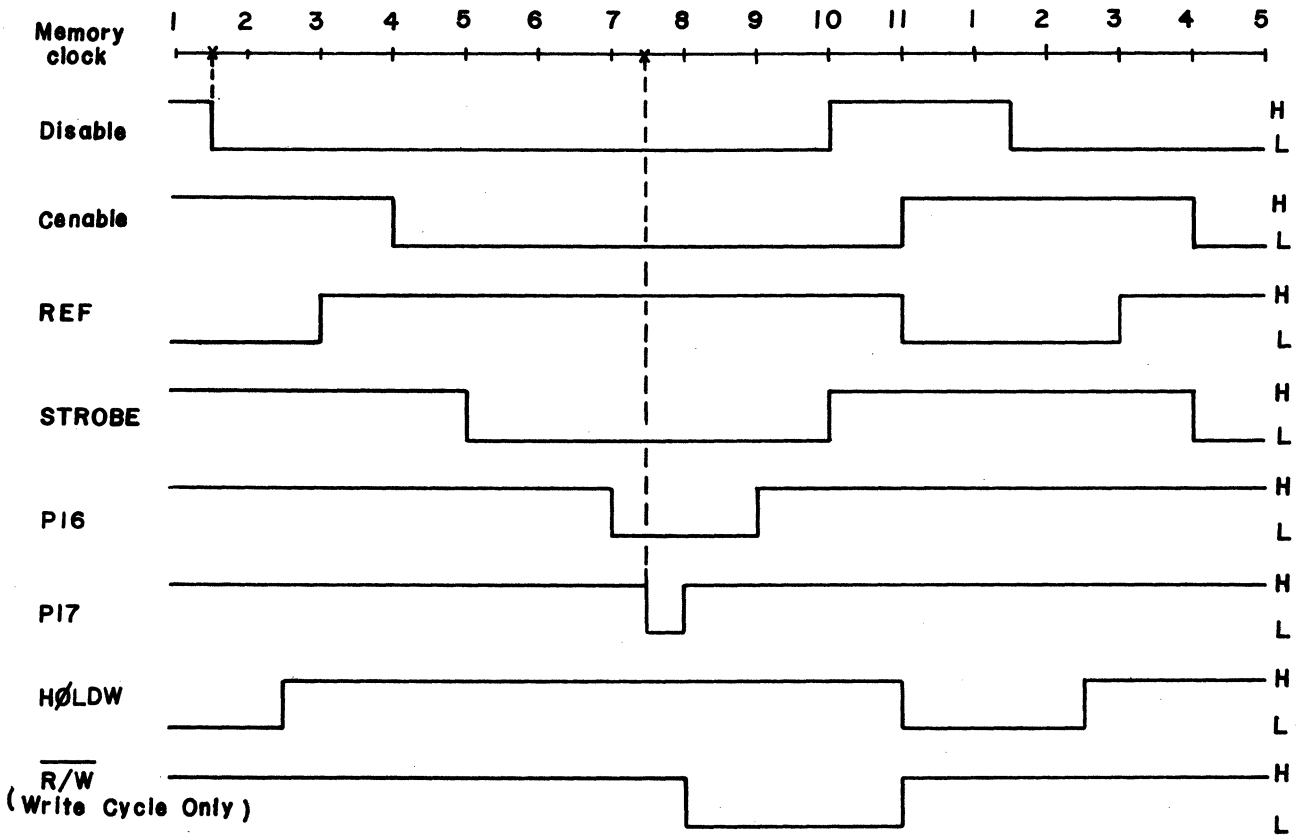
A	[U9/5]	Clock phase 1	4	D2
$\overline{\text{A}}$	[U9/6]		4	D2
AP5	[U9/9]	Clock 2.5	4	C2
$\overline{\text{AP5}}$	[U9/7]		4	C2
B	[U10/9]	Clock phase 2	4	C2
$\overline{\text{B}}$	[U10/7]		4	B2
C	[U10/5]	Clock phase 3	4	C2
$\overline{\text{C}}$	[U10/6]		4	C2
D	[U11/5]	Clock phase 4	4	D2
$\overline{\text{D}}$	[U11/6]		4	B2
E	[U11/9	Clock phase 5	4	B2
$\overline{\text{E}}$	[U11/7]		4	B2
F	[U45/8]	End of cycle	4	B4
$\overline{\text{F}}$	[U45/6]		4	A4
IP5	[U42/6]	Clock 1.5	6	A2

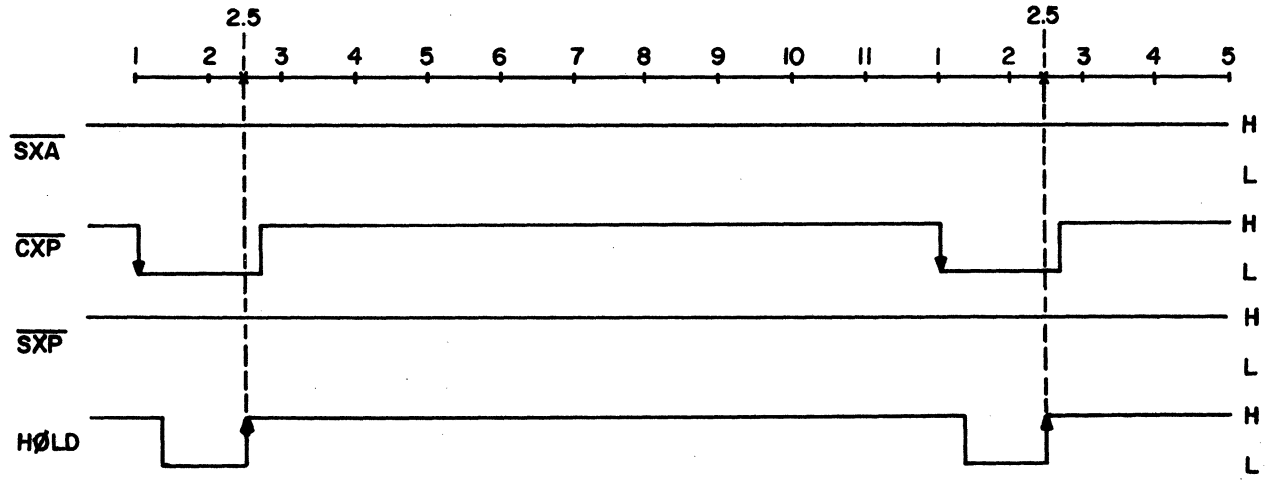
Description of Operation

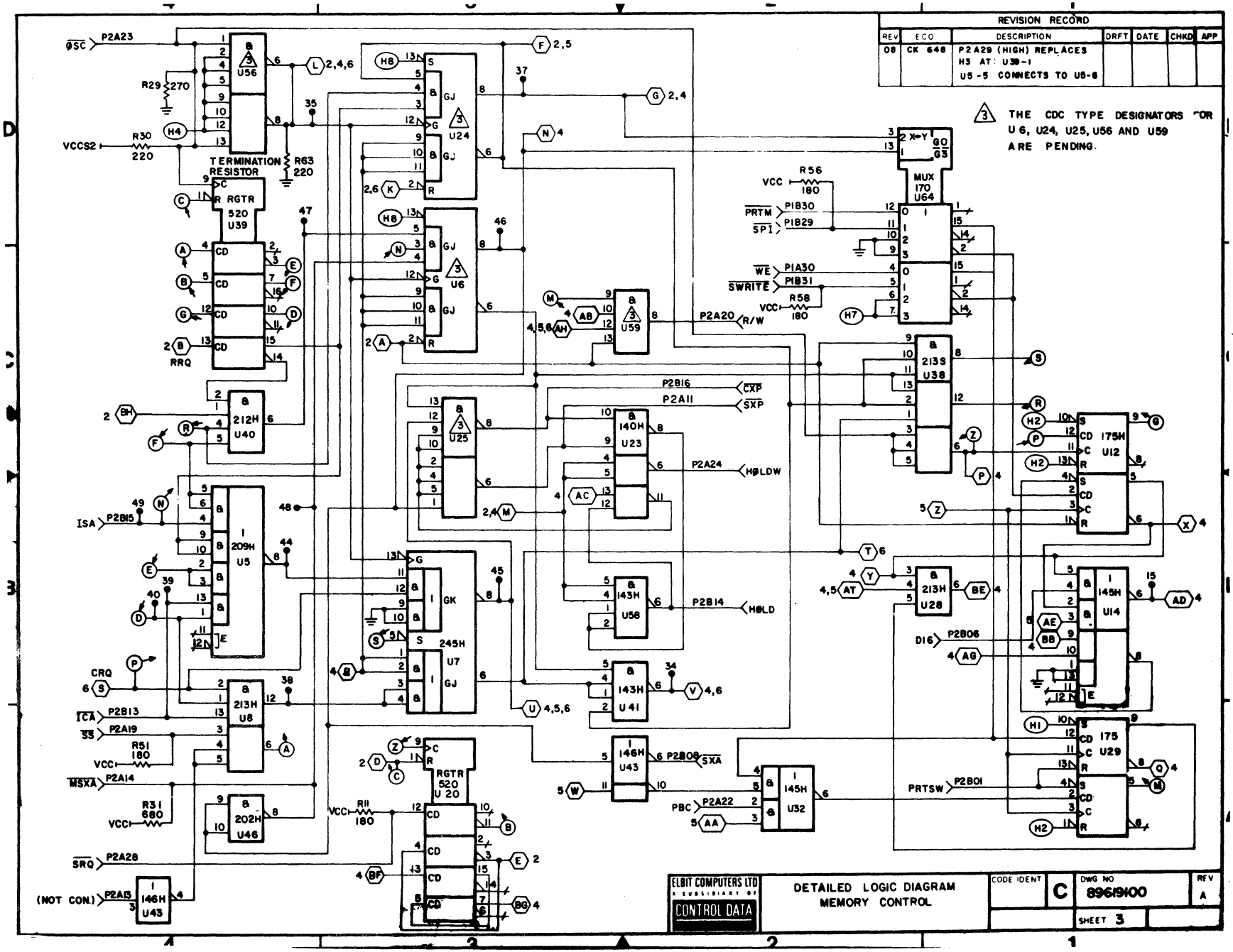
The heart of the memory timing circuit is a five stage ring counter (flip-flops contained in U9, U10, U11. This gives the main timing signals (A,B,C,D, and E). The counter is cleared by the BUSY signal (active low). The clock cycle is selected by the Access Selector when the BUSY signal goes high. This frees the counter which starts generating the clock pulses. The pattern of pulses is shown in the following two figures.

MEMORY CONTROL (Drawing number 89619100, sheet 4)

MEMORY CONTROL TIMING






REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
08 | CK 648 | P2A29 (HIGH) REPLACES H3 AT U39-1 U5-5 CONNECTS TO U5-6
3 THE CDC TYPE DESIGNATORS FOR U6, U24, U25, U56 AND U59 ARE PENDING.
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
MEMORY CONTROL
CODE IDENT C
DWG NO 89619100
REV A
SHEET 3

MEMORY CONTROL (Drawing number 89619100, sheet 3, cont'd.)

CX Selector Flip-flop (U7)

K inputs to CX activate CX, J inputs deactivate CX

K input to CX (U7)

This is a 2,2 AND/OR input gate.

U7/9,10 are grounded, reducing it functionally to a 2 input AND gate.

U7/12: Synchronized CPU request.

U7/11: Conditional activate CX if:

1) U5/9, 10 A (Sychronized) Refresh cycle is not requested.

or 2) U5/2,3 The (Synchronized) DSA priority or 32KW are not blocking the CX selector.

or 3) The CPU address is not valid and did not address this memory bank: -

a) U5/1: CPU request delayed 2 clock cycles. Sychronized.

and b) U5/3: Incorrect CPU address to this memory bank

or 4) A DSA cycle is not desired: -

a) U5/6: DSA request was activate for at least 2 clock cycles to allow time for the DSA address lines to stabilize. Synchronized.

and b) U5/4: Correct DSA address to this memory bank.

J input to CX

F(U7/1,2) End of cycle

or U7/3,4 Conditional

The CPU address is valid and it is found that the CPU did not desire usage of this memory bank:

1. U8/1: CRQ2 CPU requests delayed two clock cycles. Synchronized.

and 2. U8/2: CRQ CPU request. Synchronized.

and 3. U8/13: Incorrect CPU address to this memory bank.

MEMORY CONTROL (Drawing number 89619100, sheet 3, cont'd.)

Preset input to CX (Active Low)

U7/5: Conditional deactivate CX if:

1) U38/10: RX is active
2) U38/11: SX is active
3) U38/9: LPDR operation.

Clock input to CX

U7/13: $\overline{\text{Clock}}$ falling edge triggered clock connected to the oscillator.

$\overline{Q}$ output from CX

U7/8: CX CPU cycle

$\overline{Q}$ output from CX

U7/6: $\overline{\text{CX}}$ not a CPU cycle.

Indicating output signals

BUSY	(U41/6)	:	One of the 3 access selectors is active
ØSC	(U56/6,8)	:	Oscillator buffered. Usually used to clock falling edge triggered flip-flops.
$\overline{\text{ØSCA}}$	(U38/6)	:	Oscillator buffered. Usually used to clock rising edge triggered flip-flops.

Because the ØSC line is long, it is double buffered and terminated

Auxiliary Circuits

The signal at P2A29 is always high because a pull-up resistor R2 is attached to the line and the line is never connected in the computer. This line is used during manufacturing testing to pre-synchronize certain signals.

RX Selector Flip-flop (U24)

J inputs activate RX, K input deactivate RX

J inputs to RX

$\overline{RX}$(U24/5)

RRQ1(U24/3) Synchronized refresh request.

$\overline{BUSY}$(U24/4) The memory system is not busy with a DSA or CPU cycle (or redundantly with a Refresh cycle). Synchronized (with the clock).

K inputs to RX

F(U24/9, 10,11) End of cycle. Synchronized.

Clear input to RX Active low

LOADRA(U24/2) Master clear signal to deactivate RX before going into LPDR operation.

Q output from RX

RX(U24/8) Refresh cycle

$\overline{Q}$ output from RX

$\overline{RX}$(U24/6) Not a Refresh cycle.

Clock input to RX

$\overline{Clock}$(U24/12) Falling edge triggered clock connected to the Oscillator.

SX Selector Flip-flop (U6)

J inputs activate SX, K inputs deactivate SX

J inputs to SX

$\overline{\text{MSXA}}$(U6/4) The other memory bank is operating on a DSA request. Ignore DSA requests on this memory bank. Synchronized.

ISA(U6/3) Correct DSA address to this memory bank.

(U6/5) Conditional Activate SX if:

1) U40/1,2: Refresh Synchronized cycle is not requested. The double connections ensure that the condition is held when it occurs ($\overline{\text{RRQ}}$) and one clock after ($\overline{\text{RRQ1}}$).

and 2) U40/4 : The memory system is not busy with a Refresh, DSA or CPU cycle. Synchronized.

and 3) U40/5 : The DSA request was activated during the last clock cycle. This allows the DSA address lines to stabilize so that the SX selector will activate only on the correct memory bank. Synchronized.

K inputs to SX

U6/9,10, 11: F End of cycle. Synchronized.

Clear input to SX (active Low):

U6/2 Normal: When the memory system is in LPDR operation, the SX register is constantly deactivated.

Q output from SX

SX(U6/8): DSA cycle

Q output from SX

$\overline{\text{SX}}$(U6/6): Not a DSA cycle

Clock input to SX

$\overline{\text{Clock}}$(U6/12): Falling edge triggered clock connected to the oscillator.

Outputs

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	NAME OF SIGNAL	LOCATION SHEET	SQUARE
RX	U24/8	Refresh cycle	3	D3
$\overline{RX}$	U24/6			
SX	U6/8	DSA cycle	3	C3
$\overline{SX}$	U6/6			
CX	U7/8	CPU cycle	3	B3
$\overline{CX}$	U7/6			
ØSC	U56/6,8	Oscillator buffered	3	D4
BUSY	U38/12	Active of access selectors	3	C1
$\overline{OSCA}$	U38/6	Oscillator buffered	3	C1
$\overline{MSXA}$	P2A14	DSA cycle bank selector	3	A4
R/W	P2A20		3	C2
$\overline{CXP}$	P2B16		3	C2

MEMORY CONTROL (Drawing number 89619100, sheet 3, cont'd.)

Description of Operation

The basic units of this circuit are the three cycle selectors/registers RX, SX, and CX (U24, U6, U7). These correspond to Refresh cycle, DSA cycle, and CPU cycle respectively. Only one may be active at any time. After the cycle is over, all of the selectors must be inactive for at least one clock cycle. To assure this operation, all the registers are activated and deactivated synchronously (through their J or K inputs). The active low clear inputs of these registers are used for clearing them during LPDR (Low Power Data Retention on power failure) operation. The active low preset input on the CX register is used for LPDR operation and to assure that the CX register will not activate during a Refresh or a DSA cycle.

If simultaneously more than one access cycle is initiated at the beginning of an access cycle, only the one with the highest priority is selected.

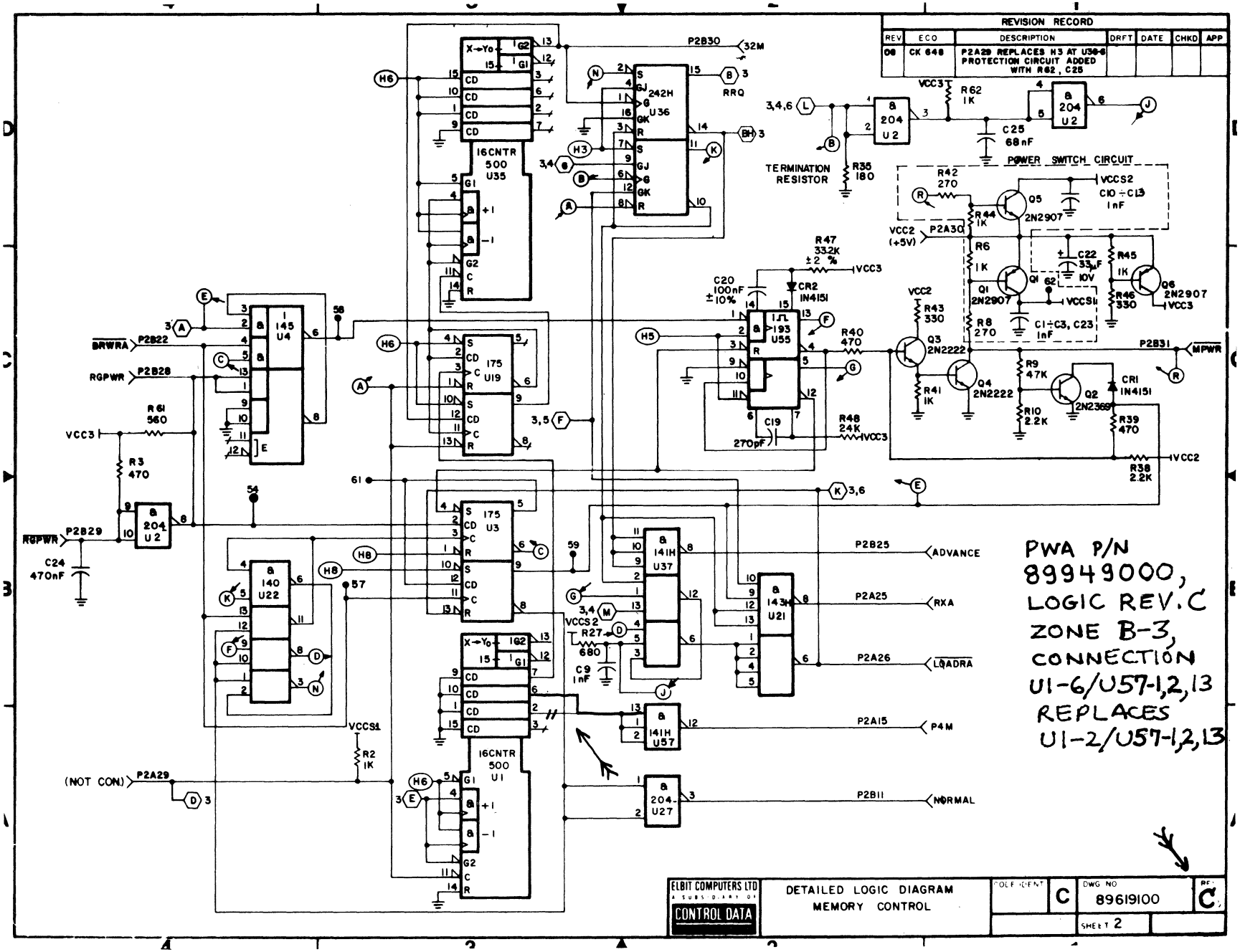
The order of priorities for the different cycles is as follows:

Refresh has the highest priority.
DSA has the next highest priority.
CPU has the least priority.

Because there can be two 32 kiloword memory systems, one in the main and one in the expansion enclosure, communication between these two units is essential. The signal $\overline{\text{MSXA}}$ prevents the DSA selector from being active simultaneously on both banks. The CPU selectors on both banks may be active simultaneously, but the improperly addressed bank may not reactivate until the next CPU is sent. The signal SRQE tells the CPU selector that the DSA request has been accepted by one of the memory banks and that the DSA address is no longer valid due to transients.

The DSA priority signal blocks the CPU access selector. The 32KWE signal blocks the CPU selector only on the upper bank if the CPU is in 32KW operation (a switch on the AB107/AB108 front panel). When the 32KW switch is active, the CPU never addresses the upper bank. Blocking the CPU access selector assures the DSA that its access time to the memory will not be delayed because the CPU selector is active.

On the lower memory bank in the main computer enclosure 32KWE is not connected to the 32KW switch. Instead it is permanently wired to ground so as to make it inactive.


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
08 | CK 648 | P2A29 REPLACES H3 AT U36-6 PROTECTION CIRCUIT ADDED WITH R62, C25
PWA P/N 89949000, LOGIC REV.C ZONE B-3, CONNECTION U1-6/U57-1,2,13 REPLACES U1-2/U57-1,2,13
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
MEMORY CONTROL
CODE IDENT C
DWG NO 89619100
REV C
SHEET 2
P2B30 32M
RRQ
TERMINATION RESISTOR
POWER SWITCH CIRCUIT
VCCS2
VCCS1
VCC3
VCC2 (+5V)
P2A30
P2B31 MPWR
P2B22 BRWRA
P2B28 RGPWR
P2B29 RGPWR
P2A29 (NOT CON)
P2B25 ADVANCE
P2A25 RXA
P2A26 LOADRA
P2A15 P4M
P2B11 NORMAL
16CNTR 500 U35
16CNTR 500 U1
242H U36
175 U19
175 U3
193 U55
145 U4
204 U2
140 U22
141H U37
141H U57
143H U21
204 U27
R61 560
R3 470
C24 470nF
R62 1K
C25 68nF
R35 180
R42 270
R44 1K
R6 1K
R8 270
R47 33.2K ±2%
C20 100nF ±10%
CR2 IN4151
R40 470
C19 270pF
R48 24K
R43 330
R41 1K
R9 47K
R10 2.2K
R39 470
R38 2.2K
CR1 IN4151
C22 33μF 10V
R45 1K
R46 330
C10÷C13 1nF
C1÷C3, C23 1nF
R27 680
C9 1nF
R2 1K

MEMORY CONTROL

MEMORY CONTROL ACCESS SELECTOR (Drawing number 89619100, sheet 3)

Function: To select one of three possible memory cycles; Refresh, DSA (Direct Storage Access) or CPU (Central Processing Unit).

Input

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	NAME OF SIGNAL	LOCATION SHEET	SQUARE
$\overline{\text{ØSC}}$	P2A23	Oscillator	3	D-4
$\overline{\text{SRQ}}$	P2A28	DSA request	3	A-4
ISA	P2B15	DSA address input	3	B-4
$\overline{\text{SS}}$	P2A19	DSA priority	3	A-4
32KWE	P2A13	32KW External	3	A-4
$\overline{\text{ICA}}$	P2B13	CPU address input	3	A-4
CRQ	P2A09	CPU cycle request	6	D-3
P	[U45/8]	End of cycle	4	A-4
$\overline{\text{LØADRA}}$	P2A26	Load Refresh Address	2	B-2
NØRMAL	P2B11	"Normal"	2	A-1
N	[U3/9]	"Normal"	2	B-3
RRQ	[U36/15]	Refresh request	2	D-2
PBC	P2A22		3	A-2
PRTSW	P2B01		3	A-1
$\overline{\text{SWRITE}}$	P1B31		3	C-2
$\overline{\text{WE}}$	P1A30		3	C-2
$\overline{\text{PRTM}}$	P1B30		3	D-2
$\overline{\text{SPT}}$	P1B29		3	D-2

MEMORY CONTROL (Drawing number 89619100, sheet 2, cont'd.)

Normal Refreshing:

A divide-by-64 counter (U20, U1, U19) divides the $\overline{\text{ØSC}}$ frequency between P2A23 and U19/6. A divide-by-nine counter (U35) further divides $\overline{\text{ØSC}}$ between U19/6 and 32M (P2B30). The signal 32M is thus $\overline{\text{ØSC}}$ divided 576 times. It is used by the CPU as a counter for a power failure condition. The falling edge of 32M also activates RRQ (U36/15 high) and advances the refresh address (U36/14 low). When the refresh cycle begins, U36/3 is cleared by RX1, and the refresh request ceases to be active.

Normal to LPDR Transition:

If during Normal operation a power failure occurs, the memory system has about one millisecond to process CPU and DSA requests before the memory system goes into LPDR operation. When a power failure occurs during normal operation, $\overline{\text{RGPWR}}$ (P2B29) rises, and U55/1 falls, activating monostable MM for 1 millisecond. However, because the Normal register is active (U3/9 high) $\overline{\text{MPWR}}$ remains Low, and V_{CCS} (switched supply) remains "on". At the end of one millisecond monostable MM falls, and monostable MP activates; MP clears monostable MM so that it will not reactivate. If the memory system is not in the middle of a memory cycle, or has not finished a refresh cycle on the previous clock, $\overline{\text{LØADRA}}$ is activated (through U37/3). The refresh cycle not being active previously is an important condition, because if $\overline{\text{LØADRA}}$ should activate too soon, the refresh address will change too soon, and memory unit specifications will not be met destroying the contents of the previous refresh address. It is permissible to activate $\overline{\text{LØADRA}}$ before $\overline{\text{CE}}$ is active (clock 4). The entire cycle from $\overline{\text{LØADRA}}$ active will repeat itself.

The Refresh Request is self starting and operates as follows:

If the memory system is in normal operation, a refresh request (RRQ) must occur every 576 clock cycles. If the memory system is in LPDR operation, monostables MM and MP will eventually become inactive. The RRQ must be active when this state occurs unless $\overline{\text{BRWRA}}$ is low. **But $\overline{\text{BRWRA}}$ is low only** on the 32nd refresh cycle. Because $\overline{\text{LØADRA}}$ must be active when the power is first initiated, $\overline{\text{BRWRA}}$ cannot then be low too. $\overline{\text{BRWRA}}$ can be low only during a series of rapid refresh cycles.

Signal P4M, (P2A15) is the oscillator (ØSC) divided 8 times. It is a timing signal to the CPU (front panel strobe).

Normal, (P2B11) is the status of the memory system to the CPU. It is wired-OR (open collector) from both memory banks. If either memory bank is not in normal operation (LPDR), this signal is low.

RXA (P2A25)

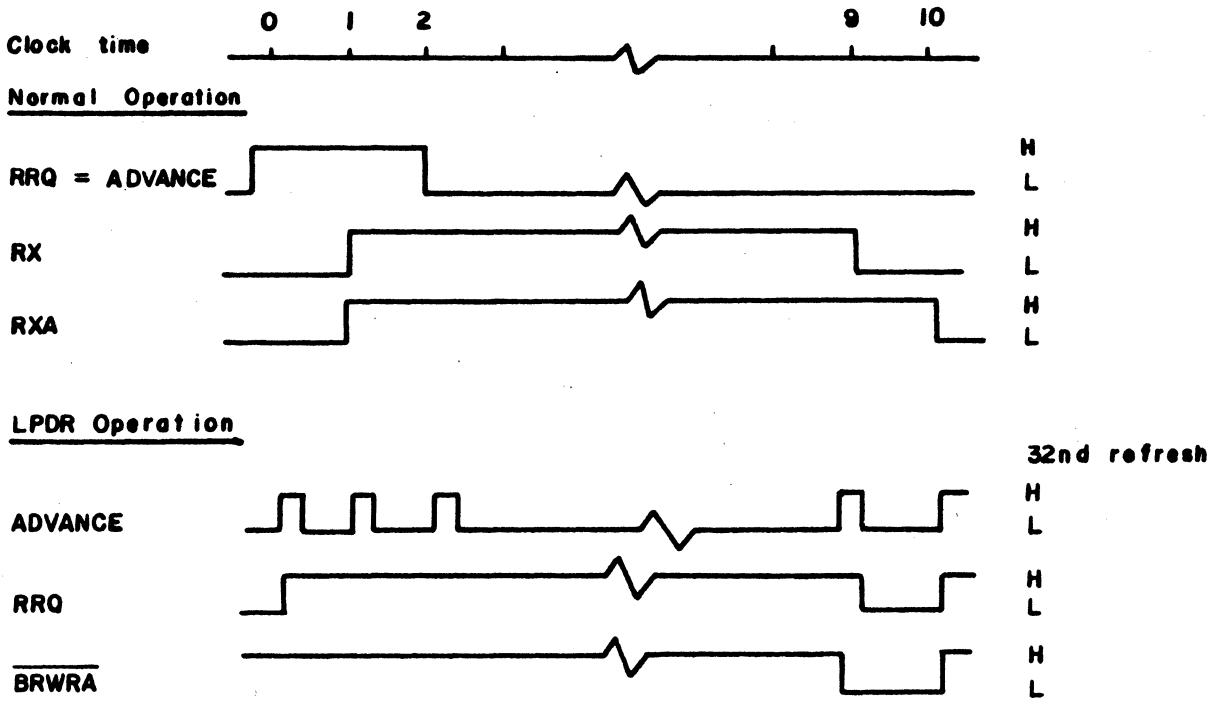
This active high signal informs the memory address card that a REFRESH cycle is being processed. It is active in LPDR operation, as well as from the beginning of a refresh cycle until one clock after RX deactivates.

High (P2A29)

Used for Manufacturing Testing of Memory Control Card, synchronizes the divide-counters. In use this line is always high and does not affect the counters.

Timing relationship between RRQ and ADVANCE:

RRQ (U36/15): active high; ADVANCE (P2/25): active high



MEMORY CONTROL (Drawing number 8961900, sheet 2, cont'd).

Detailed Description of LPDR Circuit

The memory system is self-starting. When the computer is first switched on, the memory system will be in the LPDR mode. It performs rapid refresh, tests the power supply status and depending on this, returns to LPDR or starts normal operation.

Transition from LPDR to Normal Operation:
Transients on the monostable MM input (U55/1,2) activate MM (U55/13 high) for a period determined by the RC delay at U55/14,15. After this period MM deactivates and the rising edge on U55/14,15 activates the monostable MP (U55/5: high), for a period determined by the RC delay at U55/6,7. Monostable MP (U55/12) clears MM (U55/3: low) preventing MM from reactivating. Some time during the active period of MP $\overline{\text{RXI}}$ (U37/2), MP (U37/1), and $\overline{\text{APS}}$ (U37/13) go high activating $\overline{\text{LØADRA}}$ (P2A26). When LØADRA is active (low), the following happen:

1. Normal register (U3/13) is cleared and put in normal operation:
2. PWRREG (U3/4) is preset to be active (U3/5 high)
3. Refresh Access Selector (U24/2 on sheet 3) is cleared to be inactive;
4. Disable signal (U41/13 on sheet 6) is forced high preventing memory cycles occurring in the memory.
5. The contents of the refresh address register on the memory address (MA) assembly is loaded to a particular address.

RXI is the RX register contents delayed one clock cycle.
$\overline{\text{BRWRA}}$ is a signal from the MA assembly. It is active (low) only on the 32nd refresh address after $\overline{\text{LØADRA}}$ was active.
If RXI (U22/5) is low, (as it must be since $\overline{\text{LØADRA}}$ clears RX), and Normal is inactive (22/1 high: it must be since $\overline{\text{LØADRA}}$ clears Normal at U3/13); then U36/2 is cleared, and RRQ (Refresh Request: U36/15) is active (high). RRQ is synchronized by U35/13, and requests a refresh cycle to the access selector. After its period monostable MP deactivates. MM cannot reactivate at this time because register N, (U3/9 to U4/2) is inactive, and $\overline{\text{PWRREG}}$ (U3/6 to U4/5) is also inactive. $\overline{\text{LØADRA}}$ deactivates when MP deactivates, and a refresh cycle is performed. Because $\overline{\text{BRWRA}}$ is inactive, (U22/13 high) RRQ continues requesting refresh cycles and rapid refresh occurs, refreshing all memory locations.

One clock after RX activates, RXI activates. U36/3 is cleared (low) forcing U36/14 high. U36/14 was previously low because U36/2 was preset (low).

When a flip-flop is simultaneously preset and cleared, both the Q and $\overline{Q}$ outputs will be active (high). When the refresh cycle is completed, $\overline{RXI}$ will go high, and U36/14 will go low. It is the negative edge of $\overline{RRQ}$ at U36/14 that advances the row address counter on the memory address assembly. If ADVANCE (P2B25), goes negative and LØADRA is inactive, the row address advances. On the 32nd row address, $\overline{BRWRA}$ goes low. After the 32nd refresh cycle begins, RXI activates. Because $\overline{BRWRA}$ is low, Preset (U36/2) is not active, but Clear (U36/3) is ative, and thus RRQ (refresh request) ceases to be active, terminating the rapid refresh.

Also on the falling edge of $\overline{BRWRA}$, the s atus of the power supply $\overline{RGPWR}$ is stored in the PWREG FF, U3/5,6. If there is a power-failure, $\overline{RGPWR}$ (P2B29) is high, otherwise RGPWR is low.

One clock after the 32nd refresh cycle finished, RXI inactivates, and RRQ FF preset (U36/2) activates while clear (U36/3) deactivates. The refresh address is advanced once more, and $\overline{BRWRA}$ goes high. The rising edge of $\overline{BRWRA}$ has two different conditions:

Condition 1: Power Failure

If the PWREG FF is active (U3/5 low, U3/6 high) when BRWRA rises, U55/1 falls and monostable MM is activated. The combination of $\overline{MM}$ (U55/4 low) and Normal (U3/9 low) is ORed into the master power switch and MPWR rises. When $\overline{MPWR}$ is high, V_{CCS} is off, conserving battery power. A switching circuit on Normal (U3/9 Q2) assures that this line will remain low when V_{CCS} switches off.
After the active period of $\overline{MM}$, U55/4 rises, and $\overline{MPWR}$ falls, V_{CCS} switches on. The RC on U37/5 assures that $\overline{LØADRA}$ is active. The entire cycle from $\overline{LØADRA}$ active will repeat itself.

Condition 2: Regular Power

If the PWREG FF is active U3/5 high, U3/9 (Normal) activates. Because RRQ was active before this happened one more refresh cycle is immediately performed.

MEMORY CONTROL

LOWER POWER DATA RETENTION (LPDR) (Drawing 89619100, sheet 2)

Function:

This circuit ensures that even under power fail conditions the data stored in the memory is retained, provided a power back-up source (battery equipment GD611-A) is connected to the equipment.

Input

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
$\overline{\text{BRWRA}}$	P2B22	Active on 32nd cycle	2	C4
$\overline{\text{RGPWR}}$	P2B29	Power fail	2	B4
	P2A29	Permanent high	2	A4
$\overline{\text{AP5}}$	[U37/13]	Clock 2.5	2	B2
$\overline{\text{RX}}$	[U36/9]	Refresh cycle select		
ØSC	[U36/6]	Basic timing signal	2	D3
$\overline{\text{ØSC}}$	P2A23		3	D4

Outputs

$\overline{\text{LOADRA}}$	P2A26	Load Refresh Address	2	B1
P4M	P2A15	ØSC/8	2	A1
NØRMAL	P2B11	"Normal"	2	A1
N	[U3/9]		2	B3
32M	P2B30	ØSC/512	2	D2
ADVANCE	P2B25	Address register Advance	2	B1
RXA	P2A25	CPU cycle processed	2	B1
$\overline{\text{MPWR}}$	P2B31	Master Power switch	2	C1
RRQ	[U36/15]	Refresh request	2	D2
RGPWR	P2B28	Regular power	2	C4

MEMORY CONTROL (Drawing number 89619100, sheet 2, cont'd).

Principles of Operation

Under power fail conditions the circuits essential to retaining the data stored in the memory may be operated from a battery (optional equipment GD611-A). This makes it essential to conserve the power used under such operation. The memory contents is retained by refreshing it periodically. The period is different for the 600 nanosecond cycle time and the 900 nanosecond cycle time and the 900 nanosecond cycle time memory options. To refresh the memory contents, all 32 row addresses must be refreshed within a specified period (1 millisecond for 600 nsec option, 2 milliseconds for 900 nsec option). During normal operation this is accomplished by refreshing one row address once every 512 clock oscillator periods.

This avoids long delays in DSA or CPU access time by performing short Refresh cycles at given intervals. During LPDR operation all 32 rows are refreshed sequentially every millisecond. Since it only takes 288 Oscillator periods (15.7 μsec for 600 nsec option, 22.0 μsec for 900 nsec option) to refresh 32 rows sequentially (called rapid refreshing), unnecessary control circuits can be turned off for about 98% of the time, conserving battery power. For this reason there are four separate supply lines on the memory control, memory address and memory cards.

These are:

V_{cc} +5 volts during normal operation only.
Those I.C. packages which do not need power at all during LPDR operation are connected to V_{cc}.

V_{CC3} +5 volts under all operating conditions.
Those I.C. packages which need power at all times, including LPDR operation are connected to V_{CC3}. V_{CC3} is V_{CC2} less a 0.7 volt transistor drop.

V_{CCS} (V_{CCS1}, V_{CCS2}) +5 volts switched.
Those I.C. packages which do not need power between LPDR rapid refreshing are connected to V_{cc} switched. Both V_{CCS} supplies are V_{CC2} less a 0.7 volt switching transistor drop.

V_{CC2} +5.3 volts under all operating conditions. V_{CC2} provides the power for V_{CC3} and V_{CCS}.

MEMORY CONTROL

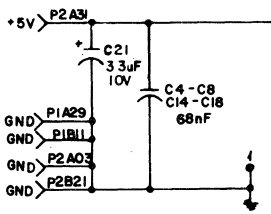
The Memory Control circuits are accommodated on a single 50-PAK printed wiring board. The logic circuit diagram is given in drawing number 89619100 sheets 1-6.

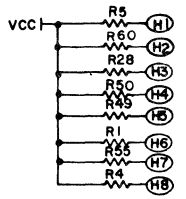
This page gives the designation and functions of the principal blocks of the circuit. Both the circuit and the signals are described in detail on pages facing the corresponding sheet of the circuit diagram.

Designation	Description	sheet
Low Power Data Retention	Guarantees proper memory refreshing for data retention during power fail conditions	2
Access Selector	Selects one of three possible memory cycles: Refresh, DSA or CPU	3
Timing	Provides all the timing signals within the memory system	4
Control Signals	Provides all control signals to the memory, memory address, CPU and DSA devices	4
Data Out Lines	Transmits the data to the DSA and the CPU	5
Bank Address	Determines which memory bank (main or expansion) the CPU or the DSA is addressing.	6

5-82

OFF SHEET REFERENCE LETTER	SHEET LOCATION				
	2	3	4	5	6
A	C - 4	C - 3			
B	B - 2	C - 4			
D	A - 4	A - 3			
E	A -33	A - 3			
F	C - 3	D - 3		C - 3	
G	D - 3	D - 2	C - 2		
K	B - 2	D - 3			B - 2
L	D - 2	D - 4	A - 3		A - 2
M	B - 3	B - 3	C - 2		
N		D - 3	D - 4		
P		B - 1	D - 3		
Q		A - 1	A - 3		
R		B - 3	A - 4		
S		B - 4			D - 2
T		B - 2			D - 2
U		A - 3	C - 4	B - 3	D - 3
V		B - 2	D - 3		B - 2
W		A - 3		A - 2	
X		B - 1	B - 4		
Y		B - 2	A - 3		
Z		B - 1		D - 2	
AA		A - 2		A - 2	
AB		C - 3	A - 2		
AC		B - 3	C - 2		
AD		B - 1	D - 3		
AE		B - 1		C - 2	
AF			C - 1		C - 2
AG		B - 1	C - 2		
AH		C - 3	B - 3	A - 3	B - 2
AK			A - 2		C - 3
AL			B - 4	A - 4	
AM			B - 2	D - 3	
AP			C - 2	D - 4	
AR			D - 3	D - 4	
AS			A - 2	D - 3	
AT		B - 2	D - 3	C - 2	
AU			A - 3	A - 3	
AV			C - 3	D - 3	
BA			D - 2		D - 2
BB		B - 1	B - 2		
BC			B - 1	C - 3	
BE		B - 1	D - 3		
BF		A - 3	D - 4		
BG		A - 3	C - 3		
BH	D - 2	C - 4			





NOTES:
1. ALL RESISTORSARE 1/4WATT, 5%.
2. R1,R4,R5,R28,R49,R55,R50,R60 ARE 1 KOHM.

U1 -VCC	U16 -VCC	U31 - VCC	U46 - VCC	U63 - VCC
U2 -VCC3	U17-VCC	U32 - VCC	U47 - VCC	U64 - VCC
U3 -VCCS1	U18 - VCC	U33 - VCC	U48 - VCC	U65 - VCC
U4 -VCCS1	U19 - VCC	U34 - VCC	U49 - VCC	U66 - VCC
U5 -VCCS1	U20 - VCC	U35 - VCC	U50 - VCC	U67 - VCC
U6 -VCCS1	U21 - VCCS1	U36 - VCCS2	U51 - VCC	U68 - VCC
U7 -VCCS1	U22 - VCCS1	U37 - VCCS2	U52 - VCC	U69 - VCC
U8 -VCC	U23 - VCC	U38 - VCCS2	U59 - VCC3	U70 - VCC
U9 -VCCS1	U24 - VCCS1	U39 - VCCS2	U56 - VCCS2	
U10 -VCCS1	U25 - VCC	U40 - VCC	U57 - VCC	
U11 -VCCS1	U26 - VCS1	U41 - VCCS2	U58 - VCC	
U12 -VCC	U27 - VCC	U42 - VCCS2	U59 - VCCS2	
U13 -VCC	U28 - VCCS1	U43 - VCC	U60 - VCC	
U14 -VCC	U29 - VCC	U44 - VCC	U61 - VCCS2	
U15 -VCC	U30 - VCC	U45 - VCCS2	U62 - VCC	

SHEET REVISION STATUS

1	2	3	4	5	6
05	05	05	05	05	05
07	07	07	07	07	05
08	08	08	08	08	08
09	08	09	09	09	09
10	10	10	09	09	09
11	11	11	11	09	09
12	12	11	11	09	09
13	13	11	11	08	09
A	A	A	A	A	A
B	A	A	A	A	A
C	C	A	A	A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
05	CK 290	REDRAWN PER CDC STD.	L.K	11.12.73	D.Tal	
06	CK 335	SH.2, R61 WAS ADDED +5V CHANGED TO VCC 3	S.D	5.4.74		
06	CK 741	DWG. ERRORS ON ALL SH. NON-STD SYMBOLS NON-STD SYGNAL FLOW MISSING CONNECTIONS WRONG CONNECTIONS	S.D	7.2.74	M.H.	
07	CK 618	DRAWING ERRORS ADDED TWO U2 INV GATES R62, C25	S.D	5.19.74	M.H	
08	CK 648	SEE REV RECORDS ON SHEETS 2 AND 3	S.D	5.19.74	M.H	
		PROTECTION OF MEMORY IC'S IN POWER FAIL				
		FASTER R/W RISE TIME				
		FACILITATE AUTOMATIC CARD TESTING				
09	CK 785	CORR. DWG. ERRORS	T.B	8.14.74	-	
10	CK 815	FREE U40-1 CONNECT U40-1 TO U36-14	T.B	8.15.74	-	
11	CK 992	NOTE 2 ADDED. FITS ASSY 89965400 REV 01. SH2: TERMINATION RES R35(180) ADDED AT U2-1, 2 (D-2); SH4: IN TABLE U24 U61 WERE R2 SH3: TERMINATIORES R63(220) ADDED AT U56-8 (D-4). NOTE 3 ADDED. SH4: TERMINATION RES R12(180) ADDED AT U9-1 (D-3). U62-12/U65-5 REPLACES P1B27, U65-5 (D-3) U13-6/U65-4 REPLACES U34-U, U65-4. DWG. ERROR CORRECTED SHTS2-4	M.L	3.9.75		
12	CK1133	FITS ASSY 89866400 REV 03. DWG UPDATED TO FIT PWB USED 89803000 REV 02: SH 2, A-3; CONNECTION VCCS1/R2 REPLACES VCC/R2. SH2, D-1: CONNECTION U2-4,5,6 REPL, U8-12,13,11 RESPECTIVELY.	Artist	3/19/75	Manuel	
13	CK 1185	SH2 ZONE C-2: C20 CHANGED FROM 100NF +100-0% TO 100 NF ±10% FITS ASSY R9935700 REV 01.	Parke	5/6/75		
A	CK1241	RELEASED CLASS A FITS ASSY R9935700 A	LK	11/4/75		
B	CK 1241	CK 1185 CANCELLED COMBINED WITH CK 1241 SAME CHANGES THAT APPEAR IN CK 1185 APPEAR IN CK 1241	S.D	June/76		
C	CK 1272	SH2, A-3: CONNECTION U1-6/U57-1,2,13 REPLACES U1-2/U57-1,2,13. FITS PWA 89949000-A				

AT 89949000 AW. DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES

3 PLACE ±	2 PLACE ±	ANGLES ±

DO NOT SCALE DRAWING

MATERIAL

FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

FIRST USED ON: AB 107-A, AB 108-A, BU 120-A

DWN	NOAMI P.	5.11.73
CHKD	S. DAYAN	11.18.73
ENGR	H. JOSEPH	11.18.73
MFG		
APPR	HAIM J.	3/19/75
QA		

TITLE

DETAILED LOGIC DIAGRAM

MEMORY CONTROL

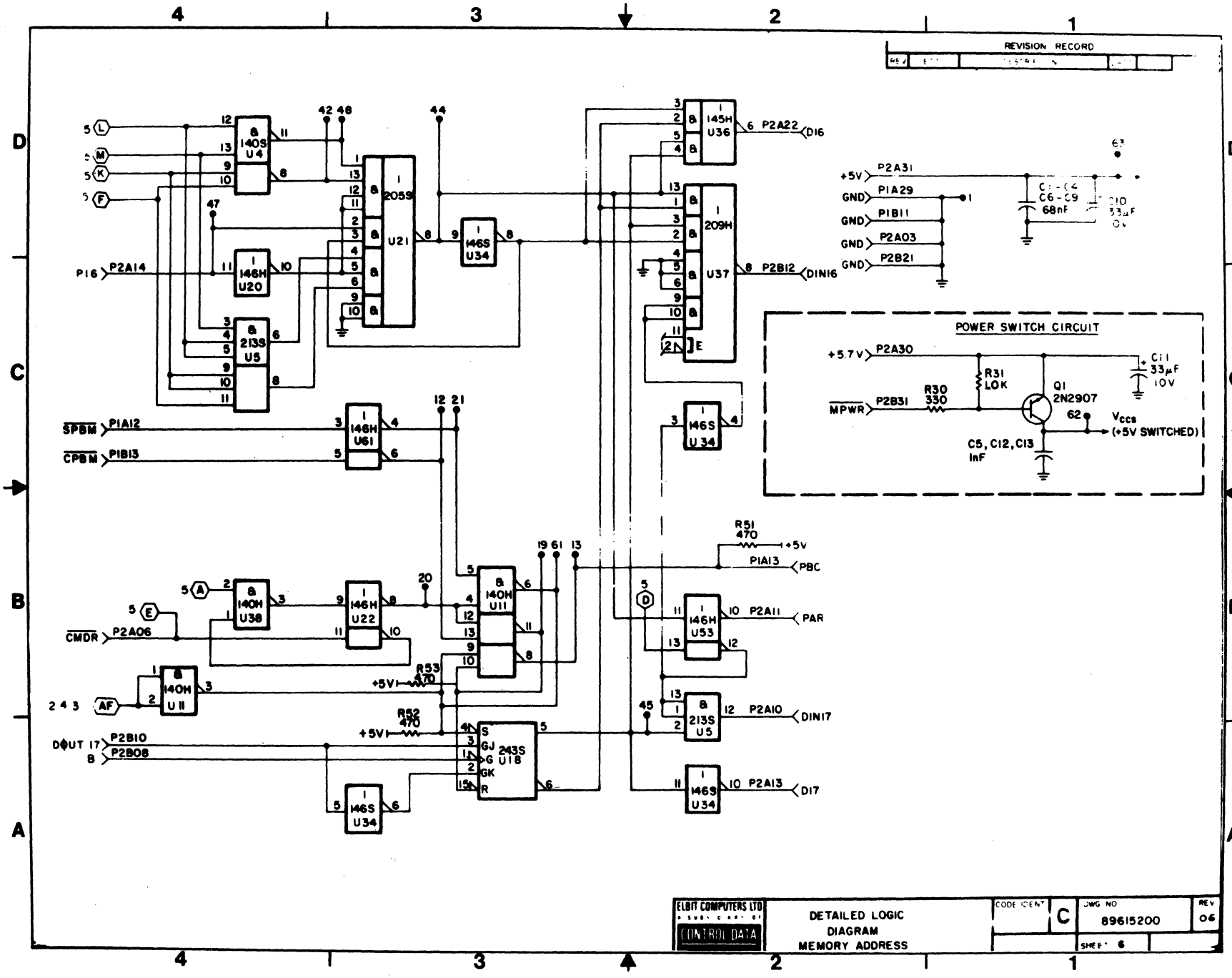
P/N 89949000

CODE IDENT	DRAWING NO
C	89619100

SCALE

SHEET 1 OF 6

89633300 E


REVISION RECORD
POWER SWITCH CIRCUIT
+5.7V P2A30
MPWR P2B31
R31 10K
R30 330
Q1 2N2907
C11 33µF 10V
C5, C12, C13 1nF
62 Vccs (+5V SWITCHED)
+5V P2A31
GND P1A29
GND P1B11
GND P2A03
GND P2B21
C1-C4 C6-C9 68nF
C10 33µF 10V
P16 P2A14
SPBM P1A12
CPBM P1B13
CMDR P2A06
DOUT 17 B P2B10 P2B08
P2A22 D16
P2B12 DIN16
P2A11 PAR
P2A10 DIN17
P2A13 D17
P1A13 PBC
R51 470
R52 470
R53 470
U4 U5 U11 U18 U20 U21 U22 U34 U36 U37 U38 U53 U61
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM MEMORY ADDRESS
CODE IDENT C
DWG NO 89615200
REV 06
SHEET 6

"Pages 5-72 to 5-80 are unassigned".

The protect bit can be modified on special CPU write cycles. During $\overline{SXA}$ high (non-DSA cycle) and $\overline{CMDR}$ low (clock 4 - 8) CPBM or SPBM active will override the DØUT17 line: if CPBM is active (low), DIN17 will be low after clock 8 of a CPU write cycle; if SPBM is active (low), DIN17 will be high after clock 8 of a CPU write cycle; if either CPBM or SPBM are active, a signal PBC (active high) is sent to the Memory Control (MC) assembly, between clocks 4 and 8.

Another special signal, D17 is generated. This signal becomes MX17 on the MC assembly and informs the CPU of the present status of the protect register. D17 is the opposite polarity of DIN17, that is, if the protect bit is set, D17 is low. If the protect bit is cleared, D17 is high. D17 does not include any timing while DIN17 does: it is simply the content of the protect register, buffered.

Circuit Description

The 16-bit parity is generated and stored in latch U21/8.

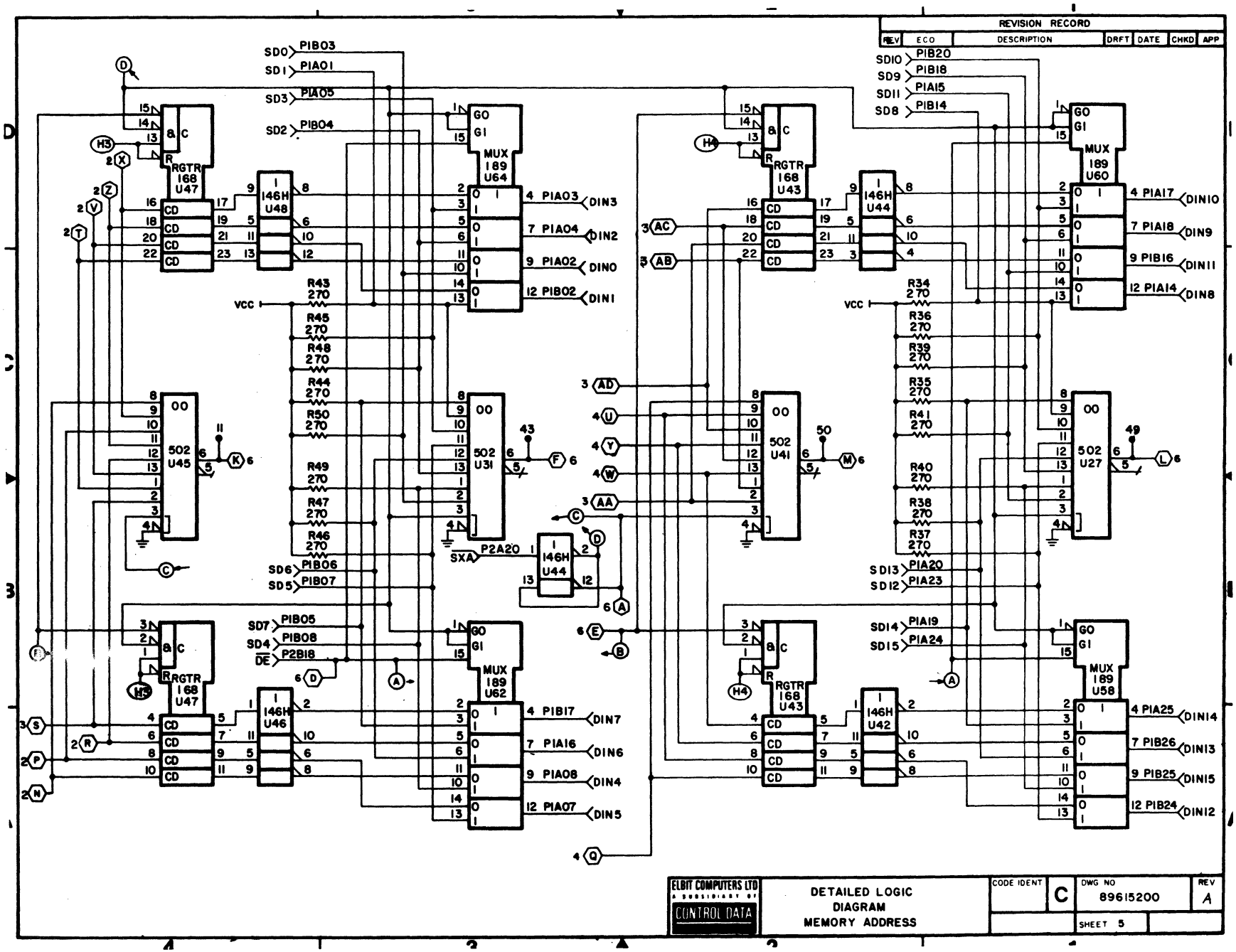
The 8 bit CPU parity, U45/6 (or U41/6), and the 8 bit DSA parity U31/6 (or U27/6) are ANDed in AND and a NAND gates (U4/8,11, U5/6,8). Since undesired outputs will always be high (that is, the 8-bit parity generators are their own selectors) only the correct parity passes through the AND and NAND gate. The outputs of the AND and NAND gate represent complementary 8 bit parity from the desired parity generator. The 8 bit AND outputs and their complementary NAND outputs are exclusively - ORed into U21. When P16 (P2A14) is low between clocks 7 - 9, the 16 bit parity passes through U21/8. Since output U21/8 is inverting it is reinverted and fed back into U21/3. On clock 9, P16 goes high and U21/2 latches the 16 bit parity.

Shortly afterward the 16 bit parity generator inputs are blocked, preventing the parity from changing. The 16 bit parity is transmitted to the MC assembly by PAR. PAR is active high when the ALU lines (carrying data to the memory) contain an even number of ones. PAR is transmitted to the CPU via MPRY on the MC assembly, so that the CPU can check the parity of the data it sent to the memory.

DIN16 is the 16 bit parity exclusively ORed with the protect register. DIN16 is wired so that when active (when $\overline{DE}$ is active) the total number of ones on DIN00-DIN17 will be odd.

Power Switch Circuit

When the signal $\overline{MPWR}$ goes active (low) on power failure, the switched logic supply (V_{CCS}) becomes active.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SD0 PIB03
SD1 PIA01
SD3 PIA05
SD2 PIB04
SD10 PIB20
SD9 PIB18
SD11 PIA15
SD8 PIB14
RGTR 168 U47
RGTR 168 U43
146H U48
146H U44
MUX 189 U64
MUX 189 U60
4 PIA03 DIN3
7 PIA04 DIN2
9 PIA02 DIN0
12 PIB02 DIN1
4 PIA17 DIN10
7 PIA18 DIN9
9 PIB16 DIN11
12 PIA14 DIN8
VCC
R43 270
R45 270
R48 270
R44 270
R50 270
R49 270
R47 270
R46 270
R34 270
R36 270
R39 270
R35 270
R41 270
R40 270
R38 270
R37 270
502 U45
502 U31
502 U41
502 U27
SXA P2A20
SD6 PIB06
SD5 PIB07
SD13 PIA20
SD12 PIA23
SD7 PIB05
SD4 PIB08
DE P2B18
SD14 PIA19
SD15 PIA24
RGTR 168 U47
RGTR 168 U43
146H U46
146H U42
MUX 189 U62
MUX 189 U58
4 PIB17 DIN7
7 PIA16 DIN6
9 PIA08 DIN4
12 PIA07 DIN5
4 PIA25 DIN14
7 PIB26 DIN13
9 PIB25 DIN15
12 PIB24 DIN12
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM MEMORY ADDRESS
CODE IDENT C
DWG NO 89615200
REV A
SHEET 5

MEMORY ADDRESS (drawing number 89615200, sheet 6)

DATA IN: PARITY AND PROTECT BITS

Function: This circuit generates the parity and protect bits for data into the memory. The Power Switch Circuit for LPDR operation is also shown here.

SIGNAL	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
Inputs				
U45/6	[K]	Parity Generator Outputs	5	C4
U41/6	[M]			C2
U31/6	[F]			C3
U27/6	[L]			C1
$\overline{SXA}$	[A]			B2
$\overline{DE}$	[D]		5	B4
P16	P2A14		6	C4
DØUT17	P2B10	Protect bit output		A4
$\overline{CPBM}$	P1B13			C4
$\overline{SPBM}$	P1A12			C4
$\overline{CMDR}$	P2A06			B4
B	P2B08		6	A4
Outputs				
DIN16	P2B12	Parity bit	6	C2
DIN17	P2A10	Protect bit		A2
D16	P2A22			D2
D17	P2A13			A2
PAR	P2A11			B2
PBC	P1A13		6	B2

Functional Description

DIN16 and DIN17 are the parity bit and protect bit into the memory respectively. Their outputs are always low if $\overline{DE}$ is high. The purpose of DIN17 is to rewrite the protect bit during write cycles. The protect bit read from memory (DØUT17 line) is stored into register U18/5, 6. The negative edge of B (P2B08) clocks this register on clock 7.5. On clock 8 of a write cycle, DIN17 will be the same polarity as DØUT17 was on clock 7.5.

MEMORY ADDRESS (drawing number 89615200, sheet 5)

DATA IN: 16 BIT DATA AND PARITY GENERATORS

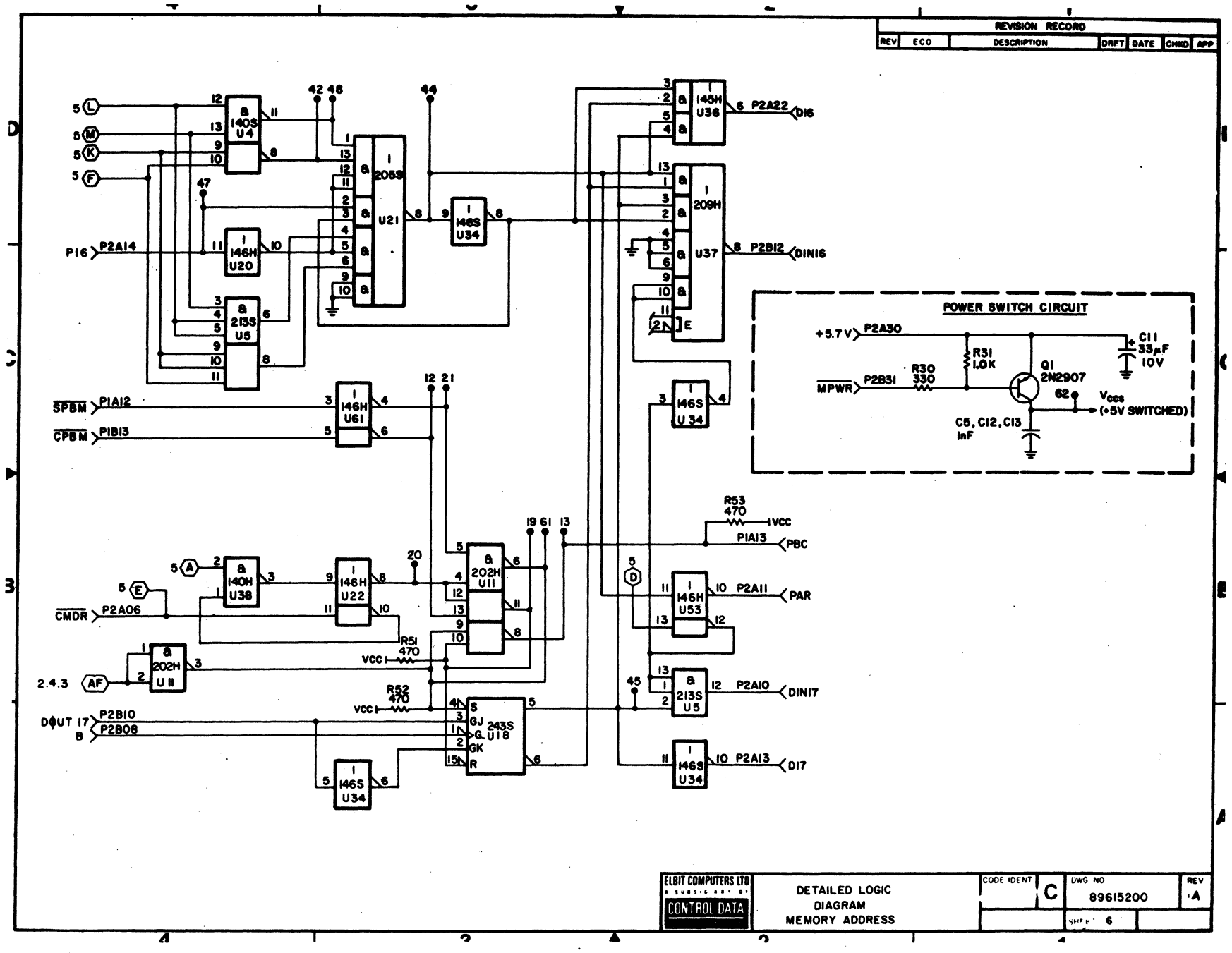
Function: To select data from the CPU or DSA lines and transmit this data to the memory.

SIGNAL	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
Inputs				
SD00 ÷ SD15		DSA bus	5	
ALU00 ÷ ALU15		ALU (CPU) bus		
$\overline{SXA}$	P2A20	DSA cycle selector		B3
$\overline{DE}$	P2B18	Data Enable	5	B4
$\overline{CMDR}$	P2A06		6	B4
Outputs				
DIN00 ÷ DIN15		Data Input to memory	5	
	[U45/6]	Parity Generator Outputs		C4
	[U41/6]			C3
	[U31/6]			C2
	[U27/6]		5	C1

Circuit Description

The CPU data enters the memory system on the ALU (ALU00÷ALU15) lines. These lines, buffered and inverted, go to the address latches. Because their polarity is wrong for data to the memory, they must be inverted again.

The ALU lines must be buffered because they may otherwise be overloaded, especially if the ALU lines are connected to both the lower and upper memory banks. The double buffered ALU lines enter data latches. These latches are opened if $\overline{SXA}$ (P2A20) is high and $\overline{CMDR}$ (P2A06) is low. Thus, data can enter the data latch during clocks 4 - 8 of a CPU or Refresh cycle. On clock 9 the latches are


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
POWER SWITCH CIRCUIT
+5.7V P2A30
MPWR P2B31
R31 1.0K
R30 330
Q1 2N2907
C11 33µF 10V
C5, C12, C13 1nF
Vccs (+5V SWITCHED)
R53 470 VCC
R51 470 VCC
R52 470 VCC
U4 140S
U5 213S
U20 146H
U21 205S
U34 146S
U36 146H
U37 209H
U61 146H
U38 140H
U22 146H
U11 202H
U53 146H
U18 243S
P16 P2A14
SPBM P1A12
CPBM P1B13
CMDR P2A06
2.4.3 AF
DOUT 17 B P2B10 P2B08
P1A13 PBC
P2A22 DI6
P2B12 DIN16
P2A11 PAR
P2A10 DIN17
P2A13 DI7
ELBIT COMPUTERS LTD
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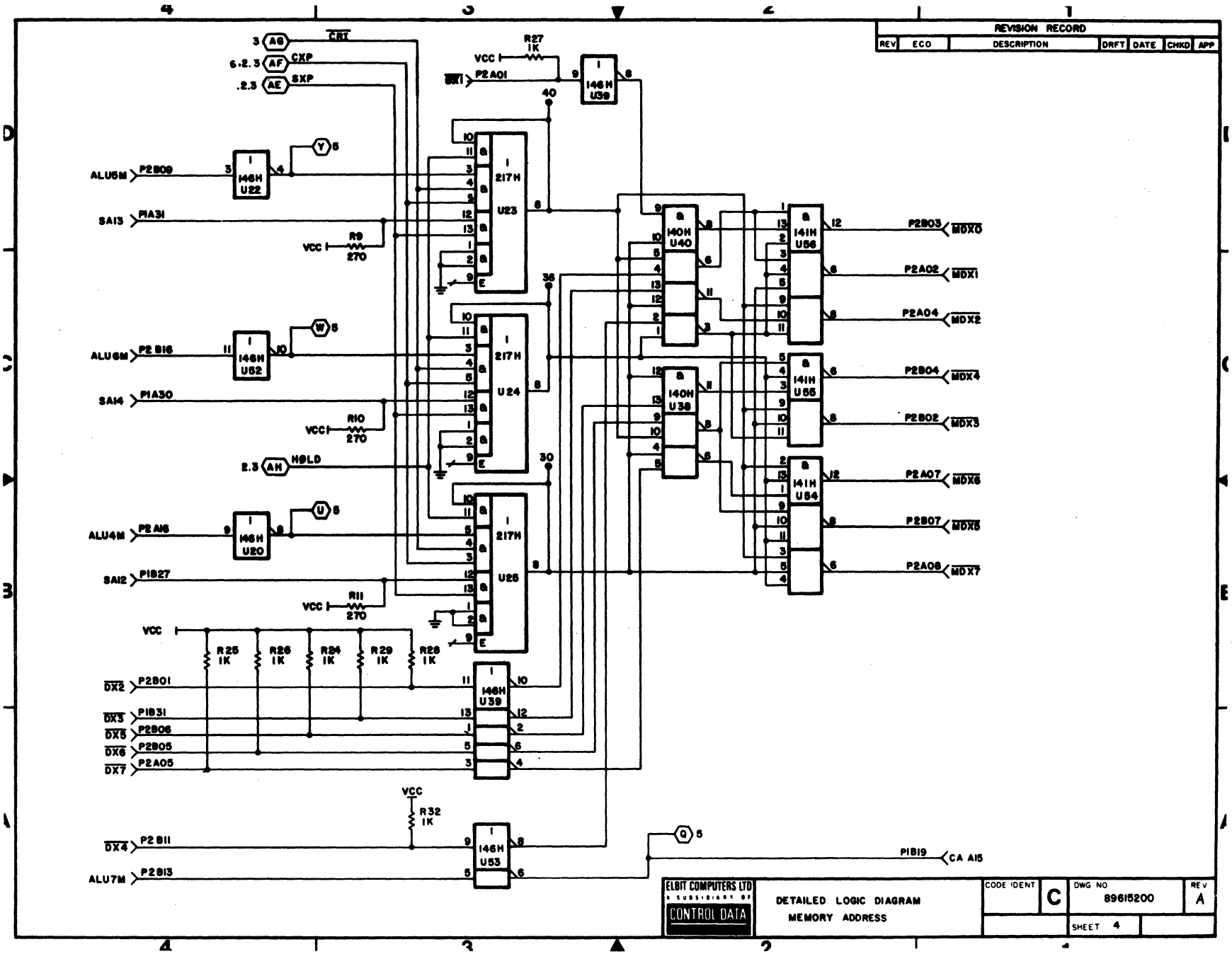
DETAILED LOGIC DIAGRAM MEMORY ADDRESS
CODE IDENT C
DWG NO 89615200
REV A
SHEET 6


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
CRT
CXP
SXP
HOLD
VCC
R27 1K
R9 270
R10 270
R11 270
R25 1K
R26 1K
R24 1K
R29 1K
R28 1K
R32 1K
146H U39
146H U22
146H U52
146H U20
146H U53
217H U23
217H U24
217H U26
140H U40
140H U38
141H U56
141H U55
141H U54
ALU6M
ALU4M
ALU7M
SAI3
SAI4
SAI2
P2B09
P2B16
P2A16
P2B11
P2B13
P1A31
P1A30
P1B27
P2B01
P1B31
P2B06
P2B05
P2A05
P2A01
P2B03
P2A02
P2A04
P2B04
P2B02
P2A07
P2B07
P2A08
P1B19
MDX0
MDX1
MDX2
MDX4
MDX3
MDX6
MDX5
MDX7
CA A15
DX2
DX3
DX5
DX6
DX7
DX4
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CONTROL DATA
DETAILED LOGIC DIAGRAM
MEMORY ADDRESS
CODE IDENT C
DWG NO 89615200
REV A
SHEET 4

MEMORY ADDRESS (drawing number 89615200, sheet 4, cont'd.)

Description

The module selector selects the address of one of eight memory modules according to either the DSA address or CPU address, and latches it. The CPU lines are active low, the DSA lines are active high. The selector outputs are active low. If a memory module assembly is installed in the computer, it pulls the $\overline{DX\#}$ signal corresponding to its location to ground. Otherwise the $\overline{DX\#}$ signal remains high. CPU and DSA addresses must correspond to each other. That is

ALU12 must correspond to SA12
ALU13 " " " SA13
ALU14 " " " SA14

$\overline{DX1}$ refers to module 1 (the second memory assembly location) and $\overline{MDX1}$ activates memory module 1. The sign # (DX#) represents one of the memory location numbers (1 ÷ 7). The first memory assembly location is always occupied.

No information is on the module selector during refresh cycles. The $\overline{REF}$ signal activates all the memory modules during a refresh cycle, so decoding of the module selector is not necessary. However, the module selectors remain stable during a refresh cycle and no spikes occur on them. This is a safeguard and not strictly necessary since the $\overline{REF}$ signal provides timing on the memory modules for the module selectors.

If all eight memory modules are installed the module addressed is the one that is used. If less than eight memory modules are available the module that is used is selected by the storage-wrap around table, built according to

a) how many modules are available
b) which module is addressed.

Formulas for this are given below: 12, 13 and 14 refer to address bits ALU12, ALU13 and ALU14 or SA12, SA13 and SA14. The wrap-around table resulting is also shown.

MEMORY ADDRESS (drawing number 89615200, sheet 4, cont'd.)

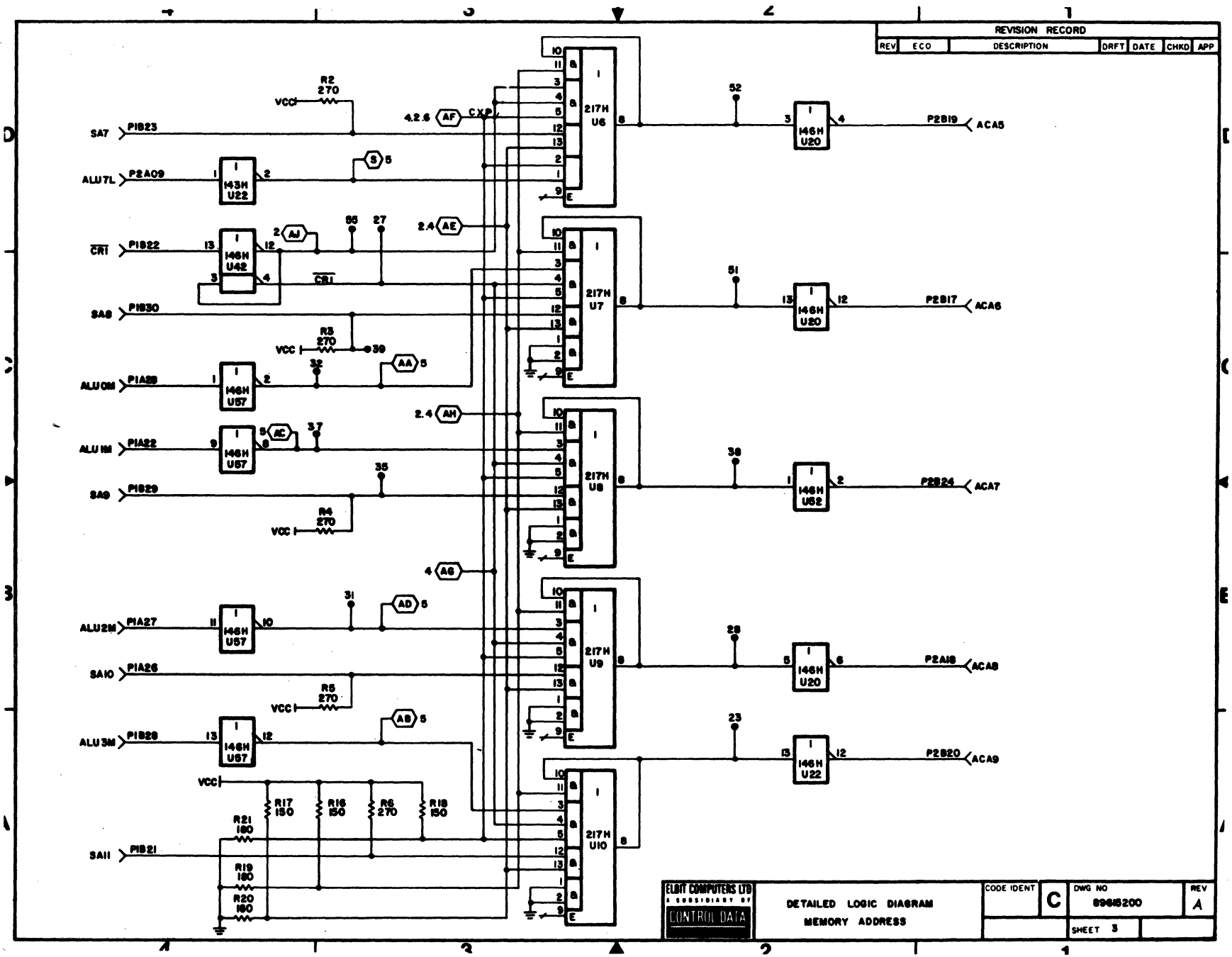
MDX0 = ($\overline{DX1.12}$) ($\overline{DX2.13}$) ($\overline{DX4.14}$)
MDX1 = (12) ($\overline{DX2.13}$) ($\overline{DX4.14}$)
MDX2 = ($\overline{DX3.12}$) (13) ($\overline{DX4.14}$)
MDX3 = (12) (13) ($\overline{DX4.14}$)
MDX4 = ($\overline{DX5.12}$) ($\overline{DX6.13}$) (14)
MDX5 = (12) (DX6.13) (14)
MDX6 = (DX7.12) (13) (14)
MDX7 = (12) (13) (14)

Storage Addressing Wrap-Around

STORAGE SIZE (K WORDS)	STORAGE MODULE ADDRESSED															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
12	0	1	2	2	0	1	2	2	0	1	2	2	0	1	2	2
16	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
20	0	1	2	3	4	4	4	4	0	1	2	3	4	4	4	4
24	0	1	2	3	4	5	4	5	0	1	2	3	4	5	4	5
28	0	1	2	3	4	5	6	6	0	1	2	3	4	5	6	6
32	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
36	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8
40	0	1	2	3	4	5	6	7	8	9	8	9	8	9	8	9
44	0	1	2	3	4	5	6	7	8	9	A	A	8	9	A	A
48	0	1	2	3	4	5	6	7	8	9	A	B	8	9	A	B
52	0	1	2	3	4	5	6	7	8	9	A	B	C	C	C	C
56	0	1	2	3	4	5	6	7	8	9	A	B	C	D	C	D
60	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	E
65	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

EFFECTIVE MODULE ADDRESSED

For example, if the computer has 16K ($16,384_{10}$) words of storage, the highest permissible address is $3FFF_{16}$. If the program attempts to address location 5040_{16} (located in a nonexistent storage module 5), it actually references location 1040_{16} in module 1.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SA7 P1B23
ALU7L P2A09
CRI P1B22
SA8 P1B30
ALU0M P1A28
ALU1M P1A22
SA9 P1B29
ALU2M P1A27
SA10 P1A26
ALU3M P1B28
SA11 P1B21
VCC
R2 270
R3 270
R4 270
R5 270
R17 150
R16 150
R6 270
R18 150
R21 180
R19 180
R20 180
143H U22
146H U42
146H U57
217H U6
217H U7
217H U8
217H U9
217H U10
146H U20
146H U52
P2B19 ACA5
P2B17 ACA6
P2B24 ACA7
P2A18 ACA8
P2B20 ACA9
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
MEMORY ADDRESS
CODE IDENT C
DWG NO 89685200
REV A
SHEET 3

MEMORY ADDRESS (drawing number 89615200, sheet 4)

MODULE SELECTOR

Function: To select one of eight memory module cards.

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
Inputs				
ALU12	P2A16	Memory Module Address from CPU	4	B4
ALU13	P2B09			D4
ALU14	P2B16			C4
ALU15	P2B13			A4
SA12	P1B27	Memory Module Address from DSA		B4
SA13	P1A31			D4
SA14	P1A30		4	C4
$\overline{CRI}$	[AG]	$00FF_{16}$ address from CPU	3	D4
$\overline{CXP}$	[AF]	CPU cycle selector	4	D4
$\overline{SXP}$	[AE]	DSA cycle selector		D4
HØLD	[AH]	Memory Module Presence Indicators		C4
$\overline{DX1}$	P2A01			D3
$\overline{DX2}$	P2B01			B4
$\overline{DX3}$	P1B31			A4
$\overline{DX4}$	P2B11			A4
$\overline{DX5}$	P2B06			A4
$\overline{DX6}$	P2B05			A4
$\overline{DX7}$	P2A05		4	A4
Outputs				
MDX0	P2B03	Memory Module Selector Signals	4	D1
MDX1	P2A02			C1
MDX2	P2A04			C1
MDX3	P2B02			C1
MDX4	P2B04			C1
MDX5	P2B07			B1
MDX6	P2A07			B1
MDX7	P2A08			B1
CAA15	P1B19		4	A1

MEMORY ADDRESS (drawing number 89615200, sheet 3)

COLUMN SELECTOR

Function: To select and latch the memory column address to the memory card.

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
Inputs:				
ALU07	P2A09	Memory Address Lines from CPU	3	D4
ALU08	P1A28			C4
ALU09	P1A22			C4
ALU10	P1A27			B4
ALU11	P1B28			A4
SA07	P1B23	Memory Address Lines from DSA		D4
SA08	P1B30			C4
SA09	P1B29			B4
SA10	P1A26			B4
SA11	P1B21			A4
$\overline{CR1}$	P1B22	$00FF_{16}$ address from CPU	3	D4
CXP	[U2/8]	CPU cycle selector	2	A4
HØLD	P2A25	Latch hold (row,column, module)	2	B4
Outputs:				
ACA5	P2B19	Memory Column Address Signals	3	D1
ACA6	P2B17			C1
ACA7	P2B24			B1
ACA8	P2A18			B1
ACA9	P2B20		3	A1

Circuit Description

Note: This circuit is similar to the Row Selector.

The column latch selects and latches the memory address from either CPU or DSA address. The output of this latch is sent without decoding to the memory chip column address inputs (A5-A9). The memory address inputs are arbitrarily wired.

MEMORY ADDRESS (drawing number 89615200, sheet 3, cont'd.)

However, CPU and DSA addresses must correspond. The CPU address must select the same location in the memory as the DSA address for that location.

Thus:

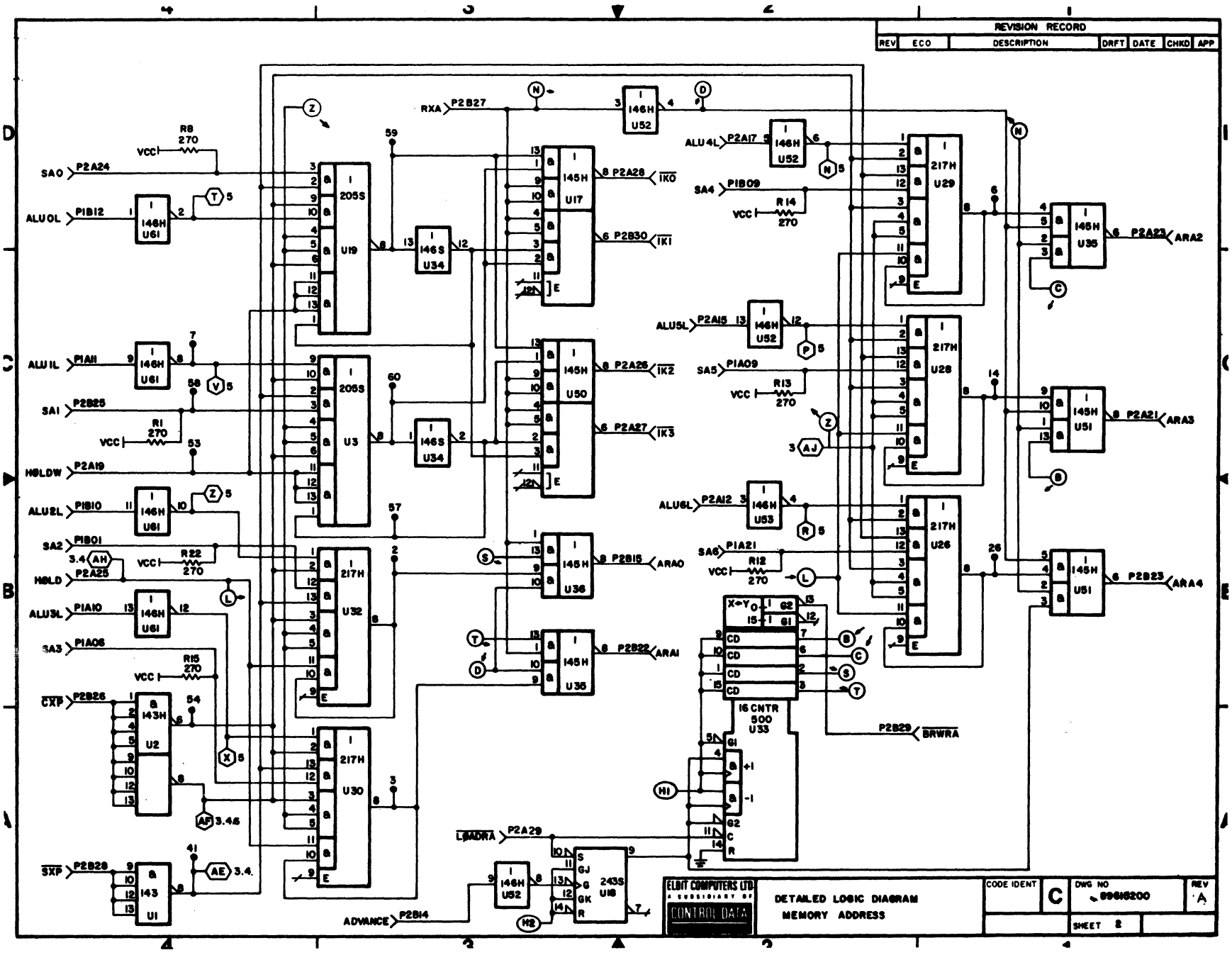
ALU07	must correspond	to	SA07
ALU08	"	"	SA08
ALU09	"	"	SA09
ALU10	"	"	SA10
ALU11	"	"	SA11

The DSA address inputs are active high. The CPU address inputs are active low.

When $\overline{CRI}$ is active (high) ALU07 appears as low, and ALU08-ALU11 appear as high.

During a refresh cycle there is no special information on the column address. However, the lines are held stable during this time to reduce system noise.

The latching circuit is similar for the row, column and module selectors. It is described opposite sheet 2.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
DETAILED LOGIC DIAGRAM
MEMORY ADDRESS
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
CODE IDENT C
DWG NO 89633200
REV A
SHEET 2
SA0 P2A24
ALU0L P1B12
ALU1L P1A11
SA1 P2B25
H0LDW P2A19
ALU2L P1B10
SA2 P1B01
H0LD P2A25
ALU3L P1A10
SA3 P1A06
CXP P2B26
SXP P2B28
RXA P2B27
ALU4L P2A17
SA4 P1B09
ALU5L P2A15
SA5 P1A09
ALU6L P2A12
SA6 P1A21
LOADRA P2A29
ADVANCE P2B14
P2B29 BRWRA
16 CNTR 500 U33
U19 U3 U32 U30 U1 U2 U17 U50 U36 U35 U29 U28 U26 U51 U52 U53 U61 U34 U18

MEMORY ADDRESS (drawing number 89615200, sheet 2, cont'd.)

Functional Description

The row latch selects and latches the DSA or the CPU addresses. The outputs of this latch, through the Refresh address Selector (ARA0 through ARA4), are sent without decoding to the memory unit row address inputs (A0 through A4). The memory address inputs are arbitrarily wired. However CPU and DSA addresses must correspond, i.e., the CPU address must select the same location in memory as the DSA address. That is

ALU02	must	correspond	to	SA02
ALU03	"	"	"	SA03
ALU04	"	"	"	SA04
ALU05	"	"	"	SA05
ALU06	"	"	"	SA06

The DSA addresses are active high; the CPU addresses are active low. When $\overline{\text{CRI}}$ is active (high) the ALU address output appears as all zeros. Although no decoding is performed, (the 5 to 32 conversion is performed in the memory unit) the latch does go through a Refresh Selector. When a refresh cycle is being performed, it is not the latch information that goes to the memory row address but the refresh row address from the refresh address counter (U33).

Circuit Description

The row refresh address is stored in a five bit binary counter circuit U33. $\overline{\text{ADVANCE}}$ (P2B14) advances the counter just before a refresh cycle is performed. $\overline{\text{LØADRA}}$ (P2A29) presets the counter so that $\overline{\text{BRWRA}}$ (P2B29) goes active (low) on the 32nd count advance after $\overline{\text{LØADRA}}$. $\overline{\text{BRWRA}}$ remains low only during the 32nd count. The outputs of the counter are arbitrarily wired with one exception. The memory units save power if the memory row address bit A4 goes low to high after the last Cenable was inactive.

This is very desirable for LPDR (Low Power Data Retention) operation. Thus, ARA4 is wired so that it will often be low on the 32nd rapid refresh cycle, and high after the 32nd rapid refresh is completed.

The row address information is taken through the Refresh Selector gates (AND-OR gates U36/8, U35/8, U35/6, U51/8, U51/6). The control inputs (U36/1 and U36/10 for ARA0 and corresponding terminals on the other gates) are driven from RXA and its inverse; RXA active selects a refresh cycle row address, $\overline{RXA}$ selects the outputs of the DSA/CPU address latches. This arrangement avoids spikes on the row address lines (ARA0 ÷ ARA4) when changing from a DSA or CPU cycle to a refresh cycle.

Row, Column and Module Selector Latching

The row, column and module selector register share a common latching system. This is described here.

The signals $\overline{SXP}$, $\overline{CXP}$ and HØLD from the memory control assembly are designed so that spikes will not occur on the row, column or module selectors. By overlapping signals so that SXP (U1/8) and HØLD on a DSA cycle or CXP (U2/6,8) and HØLD on a CPU cycle are never zero at the same time, the selectors will not generate unnecessary spikes by blocking all the information lines. HØLD overlaps with CXP (SXP) at the beginning of the cycle so that the new address can be fed into the latch before the old one is finished. CXP (SXP) overlaps with HØLD at the middle of the cycle assuring that the address is latched before it is blocked.

DSA Cycle ($\overline{SXP}$ low)

Input (Active High) SA01	SA00	Output (Active Low) 1K0	1K1	1K2	1K3
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

CPU Cycle ($\overline{CXP}$ low)

Input (Active Low) ALU01	ALU00	Output (Active Low) 1K0	1K1	1K2	1K3
L	L	H	H	H	L
L	H	H	H	L	H
H	L	H	L	H	H
H	H	L	H	H	H
$\overline{CRI}$ (High)		L	H	H	H

Refresh Cycle (RXA high)

Input --- RXA	Output (Active Low) 1K0	1K1	1K2	1K3
H	L	L	L	L

The kiloword selector must be stable at clock 1.5 so that only one kiloword will be activated by the Disable signal on the Memory module. Note that the critical kiloword selector circuits use super-high speed TTL circuits.

MEMORY ADDRESS (Drawing number 89615200, sheet 2)

ROW SELECTOR

Function: To select and latch the memory row address for DSA, CPU and Refresh cycles.

Input

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
ALU02	P1B10	Memory Address lines from CPU	2	B4
ALU03	P1A10			B4
ALU04	P2A17			D2
ALU05	P2A15			C2
ALU06	P2A12			B2
SA02	P1B01	Memory Address lines from DSA		B4
SA03	P1A06			B4
SA04	P1B09			D2
SA05	P1A09			C2
SA06	P1A21			B2
$\overline{CXP}$	P2B26	CPU cycle selector		B4
$\overline{SXP}$	P2B28	DSA cycle selector		A4
HØLD	P2A25	Latch hold (row, column, module)	2	B4
$\overline{CR1}$	P1B22	$00FF_{16}$ Address from CPU	3	D4
RXA	P2B27	Refresh cycle selector	2	D3
$\overline{LØADRA}$	P2A29	Load Refresh Address	2	A3
ADVANCE	P2B14	Advance refresh address counter	2	A3

Outputs

ARA0	P2B15	Memory Row Address Signals	2	B2
ARA1	P2B22			B2
ARA2	P2A23			D1
ARA3	P2A21			C1
ARA4	P2B23			B1
$\overline{BRWRA}$	P2B29	32nd Refresh Address count	2	A1

MEMORY ADDRESS (Drawing number 89615200, sheet 2)

KILOWORD SELECTOR

Function

This circuit selects one of four kilowords on a memory module.

Inputs

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
ALU00	P1B12	CPU address bits	2	D4
ALU01	P1A11	CPU address bits		C4
SA00	P2A24	DSA address bits		D4
SA01	P2B25	DSA address bits		C4
$\overline{CXP}$	P2B26	CPU cycle selector		B4
$\overline{SXP}$	P2B28	DSA cycle selector		A4
HØLDW	P2A19	Latch hold (Kiloword)		C4
RXA	P2B27	Refresh cycle selector	2	D3
CR1	U42/12	$00FF_{16}$ Address from CPU	3	D3

Outputs

$\overline{IK0}$	P2A28	Kiloword Selector Signals to Memory Module	2	D2
$\overline{IK1}$	P2B30	Kiloword Selector Signals to Memory Module		D2
$\overline{IK2}$	P2A26	Kiloword Selector Signals to Memory Module		C2
IK3	P2A27	Kiloword Selector Signals to Memory Module	2	C2

MEMORY ADDRESS (drawing number 89615200, sheet 2, cont'd)

Description

U19 and U3 select and latch the first two DSA or CPU address bits. This is achieved as follows (for timing diagram - clocks - refer to Figure 4-6) and to the timing diagram associated with sheet 4 of the Memory Control circuits.

Between clocks 1 and 2.5 either

$\overline{SXP}$ (for a DSA cycle) or $\overline{CXP}$ (for a CPU cycle)

will be active low while HØLDW remains low.

This allows SA00, SA01 (for a DSA cycle) or ALU00, ALU01 (for a CPU cycle) to pass through U19 and U3. At outputs U19/8 and U3/8 the signal is inverted. The signals are re-inverted and fed back into U19/1 and U3/1 in separate AND gates U34/1, 2 and U34/13, 12 forming a latch. At clock 2.5 HØLDW goes high, allowing U19/1 and U3/1 to pass through to the output (thus, the address is latched). After clock 2.5 $\overline{SXP}$ and $\overline{CXP}$ will be high so that their corresponding addresses can change without affecting the address that is latched. At clock 11 HØLDW goes down, losing the address-latch. The address is no longer needed after clock 10 because the Disable signal blocks the kiloword selector on the memory module assembly. Dropping the HØLDW signal at clock 11 decreases through-put time for a new address. The address selector must be stable by clock 1.5 of the next cycle when the Disable signal does not block the kiloword selector on the memory assembly.

The signal CR1 is inverted and ANDed into the CPU address lines (refer to sheet 3). When this signal is active (high) and $\overline{CXP}$ is active (low) and blocked, ALU00 and ALU01 appear low; CR1 is a signal used by the CPU to automatically address location $(00FF)_{16}$ in the memory (second Index Register).

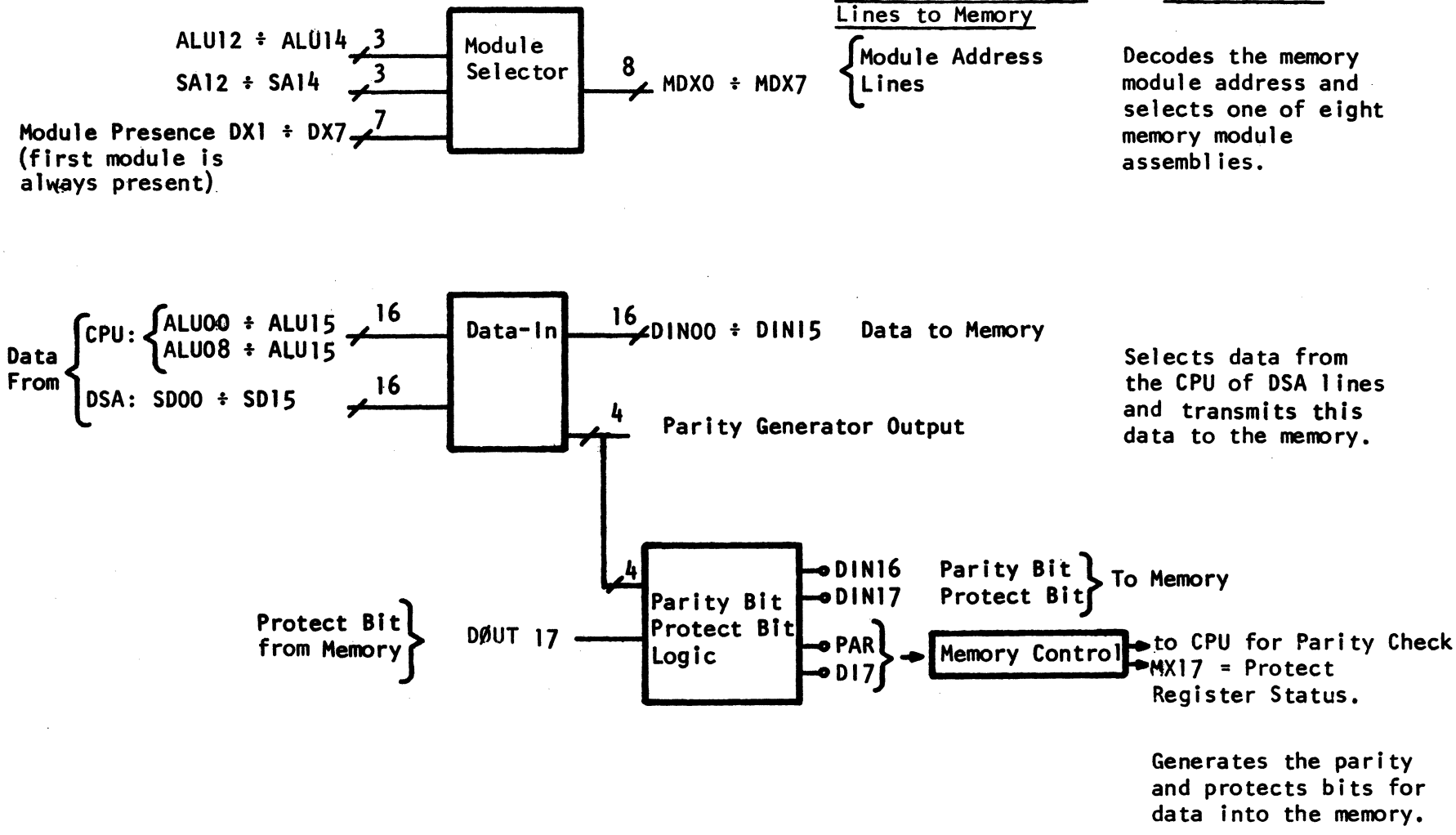
All inputs to U19 and U3 are active high. This implies that SA00, SA01 are active high.

Outputs U19/8 and U3/8 are used by the one-out-of-four decoder (U17, U50) to select one kiloword of the memory module (1K0 through 1K3). The kiloword selector output is active low. If the memory system is performing a refresh cycle, all the kilowords of the module are activated.

The following tables summarize the operation of these circuits (in tables; H = logic high, L = logic low).

MEMORY ADDRESS

continued from previous page



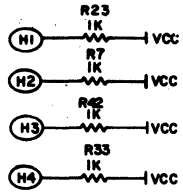
Memory Address Block Diagram

SHEET REVISION STATUS						
1	2	3	4	5	6	
05	05	05	05	05	05	
06	06	06	06	06	06	
07	06	05	06	06	06	
08	06	05	06	06	06	
09	06	06	06	06	06	
A	A	A	A	A	A	

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
05	CK356	REDRAWN TO CRC STD, C-SHEETS	SAKAL	9 MAY 73		
06	CK 625	DRAWING ERRORS ON: SH2: T.P 54 SH 4: U24-3, U24-5, R10, R11 SH 5: PIA05 SH 6: R51, R53, INVERTER U34-11, 10		April 17, 74		
07	CK 770	DETACHED LIST AY WAS PL				
08	CK785	CORRECT DWG ERRORS		AUG 18 74		
09	CK883	SH6 LL: R51 WAS R53. SH6 LR: R53 WAS R51. REF. DESIG. DID NOT FIT ASSY PWG.				
A	CK1427	RELEASED CLASS A. ALL +5V INPUTS CHANGED TO VCC. FILTER MOVED FROM SH6 TO SH1.				

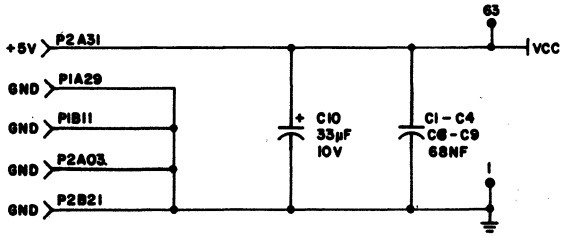
ØFF - SHEET REFERENCES

ØFF - SHEET REFERENCE LETTER	SHEET LOCATION				
	2	3	4	5	6
A				B2	B4
D				B3	B2
E				B3	B4
F				C3	D4
K				C4	D4
L				C1	D4
M				C2	D4
N	D2			A4	
P	C2			A4	
Q			A2	A3	
R	B2			A4	
S		D3		A4	
T	D4			D4	
U			B3	C3	
V	C4			D4	
W			C3	C2	
X	A4			D4	
Y			D3	C3	
Z	B4			D4	
AA		C3		C3	
AB		A3		D2	
AC		C4		D2	
AD		B3		C3	
AE	A4	D3	D4		
AF	A4	D3	D4		B4
AG		B3	D4		
AH	B4	C3	C4		
AJ	C2	D4			



NØTES:

1. ALL RESISTØRS ARE 0.25 WATT 5%
2. THE VØLTAGE SUPPLIED TØ ALL THE INTEGRATED CIRCUITS IS Vcc EXCEPT FØR: U17, U18, U33, U35, U36, U50, U51, AND U52 TØ WHICH Vccs IS SUPPLIED



AY 89615000	DETACHED LISTS	UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES 3 PLACE ± 2 PLACE ± ANGLES ±	ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	FIRST USED ON AB107-A AB108-A BV120-A	TITLE DETAILED LOGIC DIAGRAM MEMORY ADDRESS
		DO NOT SCALE DRAWING	DWN AUBREY KAGAN 8 DEC 72		
		MATERIAL	CHKD 6 Kagan DEC 9 73		CODE IDENT C
		FINISH	ENGR D Tal DEC 12 73		DRAWING NO 89615200
			MFG [illegible]		
			APPR [illegible]		SCALE
			Q.A [illegible]		SHEET 1 OF 6

MEMORY ADDRESS

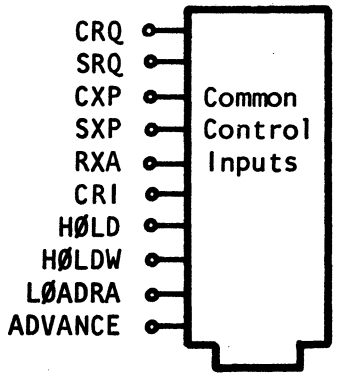
The Memory Address circuits receive the address buses from the DSA channel and from the CPU and generate the addressing signals for the whole memory system. They also generate the data parity and protect bits. The memory data input is routed through this assembly, it also accommodates the switching circuit for the switched +5V supply (V_{CCS}) used during LPDR (Low Power Data Retention) operation.

This page lists the principal blocks of the Memory Address. Its block diagram is given on the next two pages.

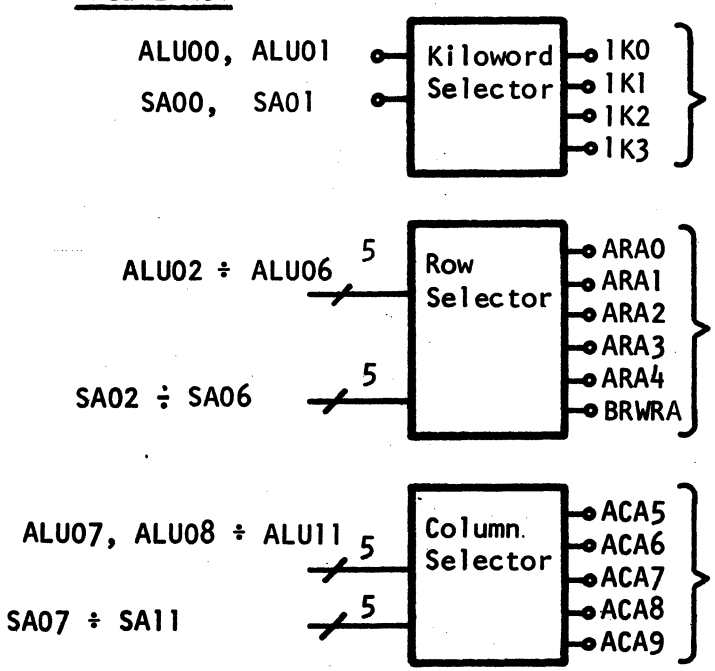
THE MAIN FUNCTIONAL BLOCKS

Designation	Shown on sheet
Kiloword selector	2
Row selector	2
Column selector	3
Module selector	4
Data in: 16 bit data and parity generators	5
Data in: parity and protect bits	6

MEMORY ADDRESS



The Memory Address circuits are accommodated on a single 50-PAK printed wiring board. The logic circuit diagram is given in drawing number 89615200, (sheets 1-5). These pages show the principal blocks making up the Memory Address together with the main input and output signals. Both the circuit and the signals are described in detail on pages associated with corresponding sheet of the circuit diagram.

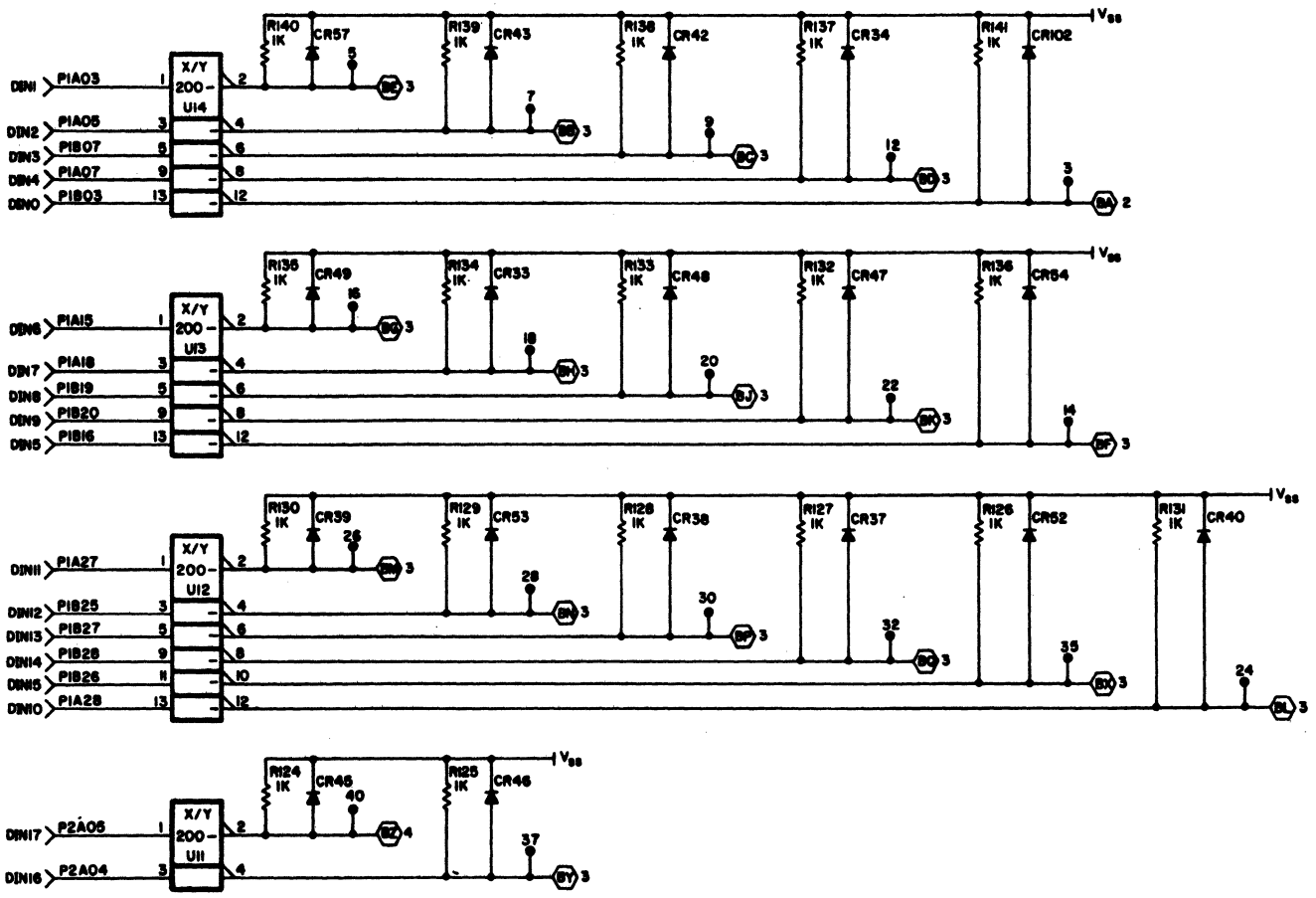


Memory Address Block Diagram

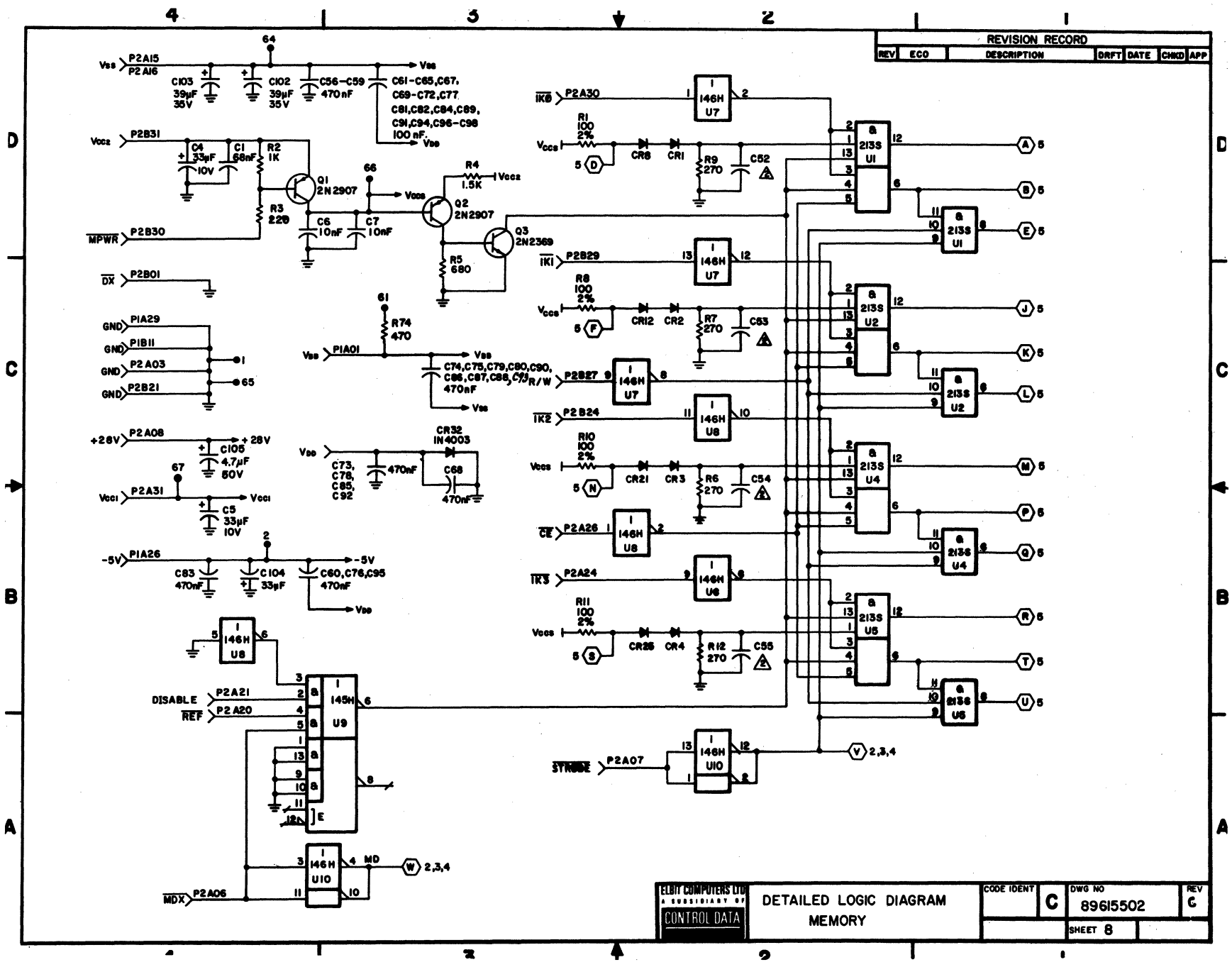
(diagram continued on next page)

"Pages 5-40 to 5-44 are unassigned"

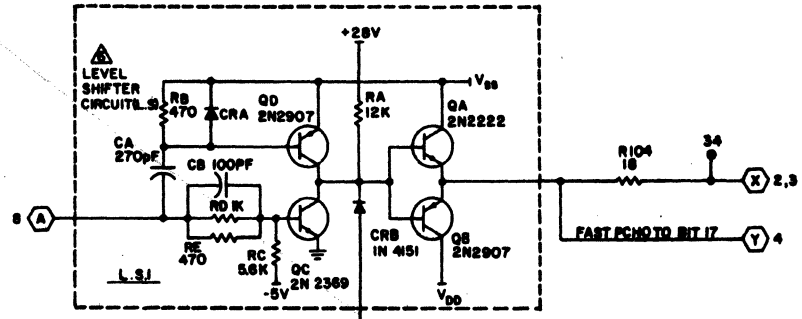
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM MEMORY (INPUTS CIRCUIT)	CODE IDENT C	DWG NO 89615502	REV A
			SHEET 7	


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
Vss P2A15 P2A16
C103 39µF 35V
C102 39µF 35V
C56-C59 470nF
C61-C65,C67, C69-C72,C77 C81,C82,C84,C89, C91,C94,C96-C98 100 nF.
Vcc2 P2B31
C4 33µF 10V
C1 68nF
R2 1K
R3 220
Q1 2N2907
Q2 2N2907
Q3 2N2369
R4 1.5K
R5 680
C6 10nF
C7 10nF
MPWR P2B30
DX P2B01
GND P1A29
GND P1B11
GND P2A03
GND P2B21
R74 470
P1A01
C74,C75,C79,C80,C90, C86,C87,C88,C93 470nF
+28V P2A08
C105 4.7µF 50V
Vcc1 P2A31
C5 33µF 10V
-5V P1A26
C83 470nF
C104 33µF
C60,C76,C95 470nF
CR32 IN4003
C73, C78, C85, C92 470nF
C68 470nF
IK0 P2A30
IK1 P2B29
R/W P2B27
IK2 P2B24
IK3 P2A24
CE P2A26
R1 R8 R10 R11 100 2%
CR8 CR1 CR12 CR2 CR21 CR3 CR26 CR4
R9 R7 R6 R12 270
C52 C53 C54 C55
146H U7 146H U8 146H U6
213S U1 213S U2 213S U4 213S U5 213S U6
DISABLE P2A21
REF P2A20
145H U9
MDX P2A06
146H U10
MD
STROBE P2A07
ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM MEMORY
CODE IDENT C
DWG NO 89615502
REV C
SHEET 8

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

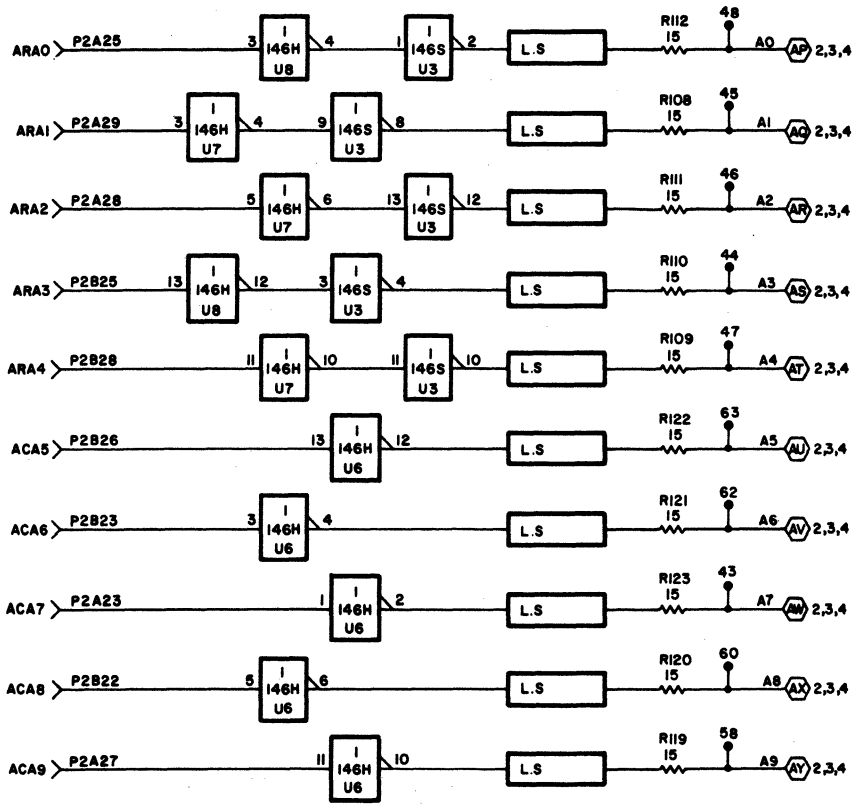


⚠ THE COMPONENTS ENCLOSED IN DASHED LINES FORM A LEVEL SHIFTER(L.S.) THE REF. DESIG. OF IT COMPONENTS FOR THE DIFFERENT LEVEL SHIFTER CIRCUITS SHOWN ON THIS SHEET ARE GIVEN IN THE TABLE. DESIG. "NC" IN TABLE MEANS: COMPONENT AND LINE NOT CONNECTED IN THE SPECIFIED L.S

L.S. NO.	OUTPUT SIGNAL	REFERENCE DESIGNATIONS IN LEVEL SHIFTER CIRCUITS													
		QA	QB	QC	QD	RA	RB	RC	RD	RE	CA	CB	CRA	CRB	RL
L.S.1	PCH0	Q72	Q50	Q6	Q28	R82	R59	R15	R17	NC	C10	C32	CR7	NC	NC
L.S.2	CEN0	Q71	Q49	Q5	Q27	R81	R58	R14	R16	R34	C9	C31	CR6	CR 106	D
L.S.3	R/W0	Q70	Q48	Q4	Q26	R80	R57	R13	R35	NC	C8	C30	CR5	NC	NC
L.S.4	PCH1	Q75	Q53	Q9	Q31	R85	R62	R18	R40	NC	C13	C35	CR11	NC	NC
L.S.5	CEN1	Q74	Q52	Q8	Q30	R84	R61	R17	NC	R39	C12	C34	CR10	CR 104	P
L.S.6	R/W1	Q73	Q51	Q7	Q29	R83	R60	R16	R38	NC	C11	C33	CR9	NC	NC
L.S.7	PCH2	Q83	Q61	Q17	Q39	R93	R70	R26	R48	NC	C21	C43	CR20	NC	NC
L.S.8	CEN2	Q82	Q60	Q16	Q38	R92	R69	R25	NC	R47	C20	C42	CR19	CR 108	N
L.S.9	R/W2	Q81	Q59	Q15	Q37	R91	R68	R24	R46	NC	C19	C41	CR18	NC	NC
L.S.10	PCH3	Q86	Q64	Q20	Q42	R96	R73	R29	R51	NC	C24	C46	CR24	NC	NC
L.S.11	CEN3	Q85	Q63	Q19	Q41	R95	R72	R28	NC	R50	C23	C45	CR23	CR 108	S
L.S.12	R/W3	Q84	Q62	Q18	Q40	R94	R71	R27	R49	NC	C22	C44	CR22	NC	NC

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM MEMORY LEVEL SHIFTER CIRCUITS	CODE IDENT C	DWG NO 89615532	REV A
			SHEET 5	

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



⚠5 THE TYPICAL LEVEL SHIFTER CIRCUIT IS ON SHEET 5

OUTPUT SIGNAL	REFERENCE DESIGNATIONS IN LEVEL SHIFTER CIRCUITS										
	QA	QB	QC	QD	RA	RB	RC	RD	CA	CB	CRA
A0	Q80	Q58	Q14	Q36	R90	R67	R23	R45	CI8	C40	CRI7
A1	Q76	Q54	Q10	Q32	R86	R63	RI9	R4I	CI4	C36	CRI3
A2	Q79	Q57	Q13	Q35	R89	R66	R22	R44	CI7	C39	CRI6
A3	Q78	Q56	Q12	Q34	R88	R65	R2I	R43	CI6	C38	CRI5
A4	Q77	Q55	Q11	Q33	R87	R64	R20	R42	CI5	C37	CRI4
A5	Q90	Q68	Q24	Q46	R100	R77	R33	R55	C28	C50	CR29
A6	Q89	Q67	Q23	Q45	R99	R76	R32	R54	C27	C49	CR28
A7	Q91	Q69	Q25	Q47	R101	R78	R 4	R56	C29	C5I	CR30
A8	Q88	Q66	Q22	Q44	R98	R75	R3I	R53	C26	C48	CR27
A9	Q87	Q65	Q21	Q43	R97	R74	R30	R52	C25	C47	CR26

ELBIT COMPUTERS LTD
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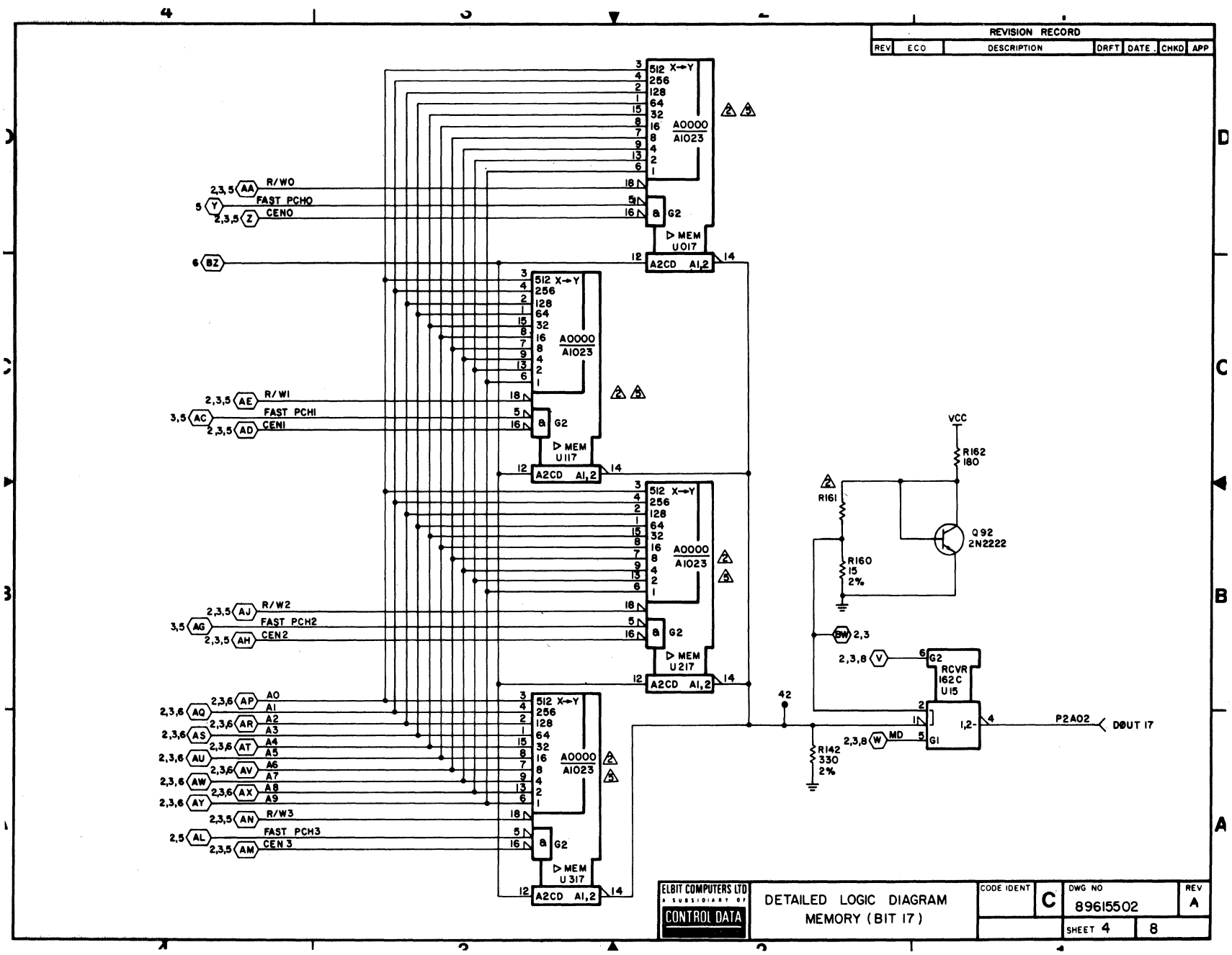
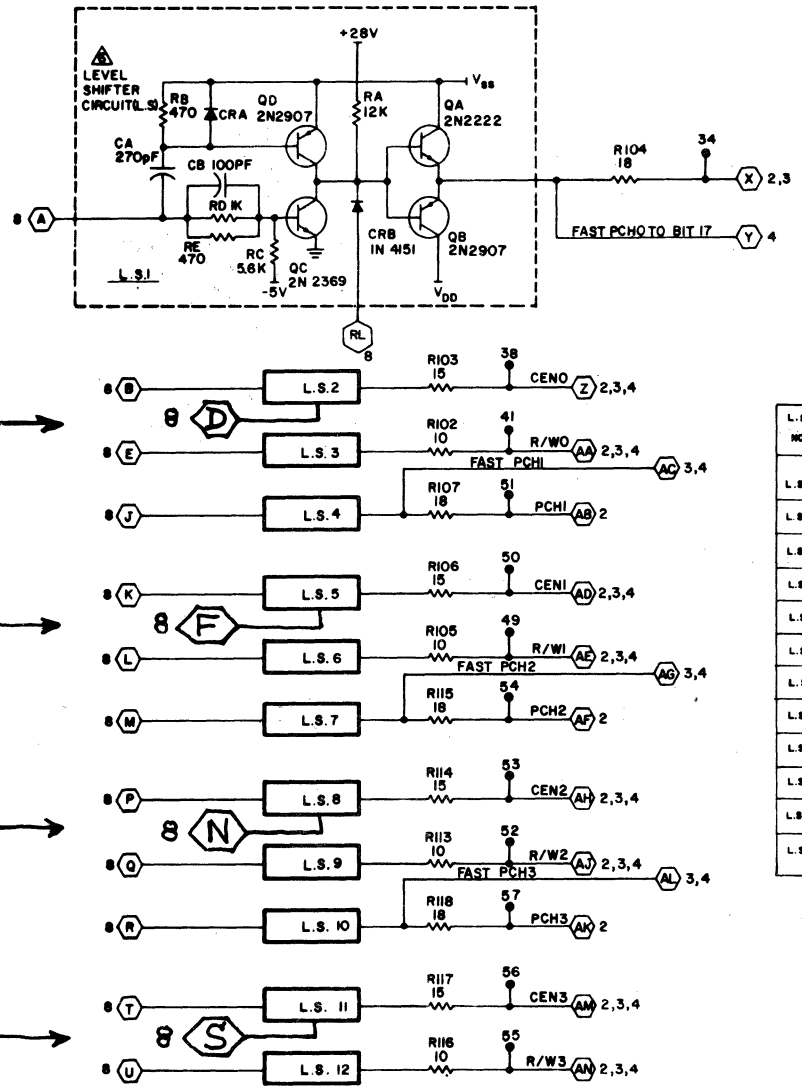
CONTROL DATA

DETAILED LOGIC DIAGRAM
MEMORY
LEVEL SHIFTER CIRCUITS

CODE IDENT: C
DWG NO: 89615502
REV: A
SHEET 6


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
512 X→Y
A0000
A1023
MEM U017
MEM U117
MEM U217
MEM U317
A2CD A1,2
R/W0
FAST PCH0
CEN0
R/W1
FAST PCH1
CEN1
R/W2
FAST PCH2
CEN2
R/W3
FAST PCH3
CEN3
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
VCC
R162 180
R161
R160 15 2%
R142 330 2%
Q92 2N2222
RCVR 162C U15
P2A02
DOUT 17
MD
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
MEMORY (BIT 17)
CODE IDENT C
DWG NO 89615502
REV A
SHEET 4 8

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



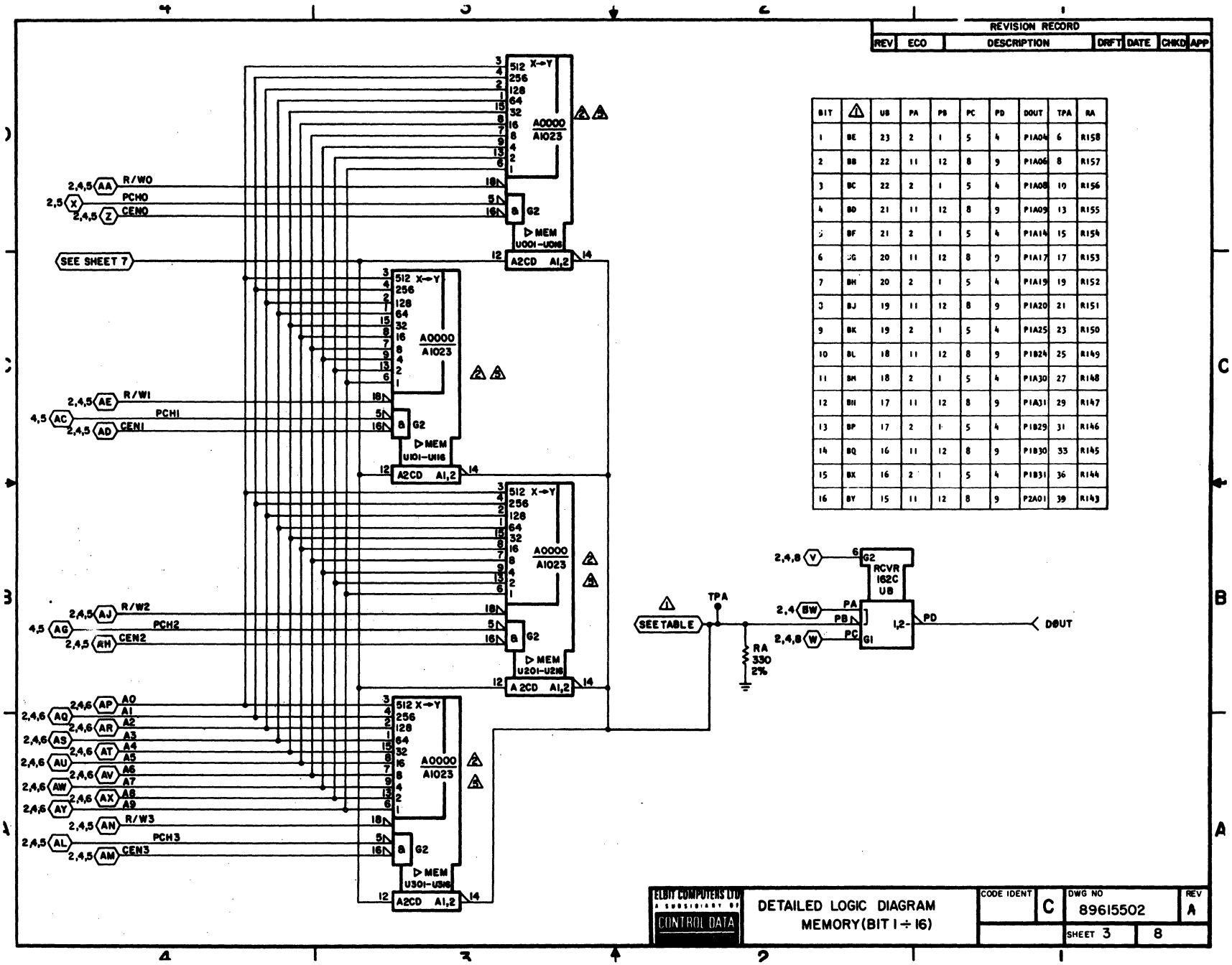
⑥ THE COMPONENTS ENCLOSED IN DASHED LINES FORM A LEVEL SHIFTER(L.S.) THE REF. DESIG. OF IT COMPONENTS FOR THE DIFFERENT LEVEL SHIFTER CIRCUITS SHOWN ON THIS SHEET ARE GIVEN IN THE TABLE. DESIG "NC" IN TABLE MEANS: COMPONENT AND LINE NOT CONNECTED IN THE SPECIFIED L.S

L.S. NO	OUTPUT SIGNAL	REFERENCE DESIGNATIONS IN LEVEL SHIFTER CIRCUITS													
		QA	QB	QC	QD	RA	RB	RC	RD	RE	CA	CB	CRA	CRB	RL
L.S.1	PCHO	Q72	Q50	Q6	Q28	R82	R59	R15	R17	NC	C10	C32	CR7	NC	NC
L.S.2	CENO	Q71	Q49	Q5	Q27	R81	R58	R14	R16	R34	C9	C31	CR6	CR 105	D
L.S.3	R/WO	Q70	Q48	Q4	Q26	R80	R57	R13	R35	NC	C8	C30	CR5	NC	NC
L.S.4	PCHI	Q75	Q53	Q9	Q31	R85	R62	R18	R40	NC	C13	C35	CR11	NC	NC
L.S.5	CENI	Q74	Q52	Q8	Q30	R84	R61	R17	R39	R38	C12	C34	CR10	CR 104	F
L.S.6	R/WI	Q73	Q51	Q7	Q29	R83	R60	R16	R38	NC	C11	C33	CR9	NC	NC
L.S.7	PCH2	Q83	Q61	Q17	Q39	R93	R70	R26	R48	NC	C21	C43	CR20	NC	NC
L.S.8	CEN2	Q82	Q60	Q16	Q38	R92	R69	R25	NC	R47	C20	C42	CR19	CR 106	N
L.S.9	R/W2	Q81	Q59	Q15	Q37	R91	R68	R24	R46	NC	C19	C41	CR18	NC	NC
L.S.10	PCH3	Q86	Q64	Q20	Q42	R96	R73	R29	R51	NC	C24	C46	CR24	NC	NC
L.S.11	CEN3	Q85	Q63	Q19	Q41	R95	R72	R28	NC	R50	C23	C45	CR23	CR 108	S
L.S.12	R/W3	Q84	Q62	Q18	Q40	R94	R71	R27	R49	NC	C22	C44	CR22	NC	NC

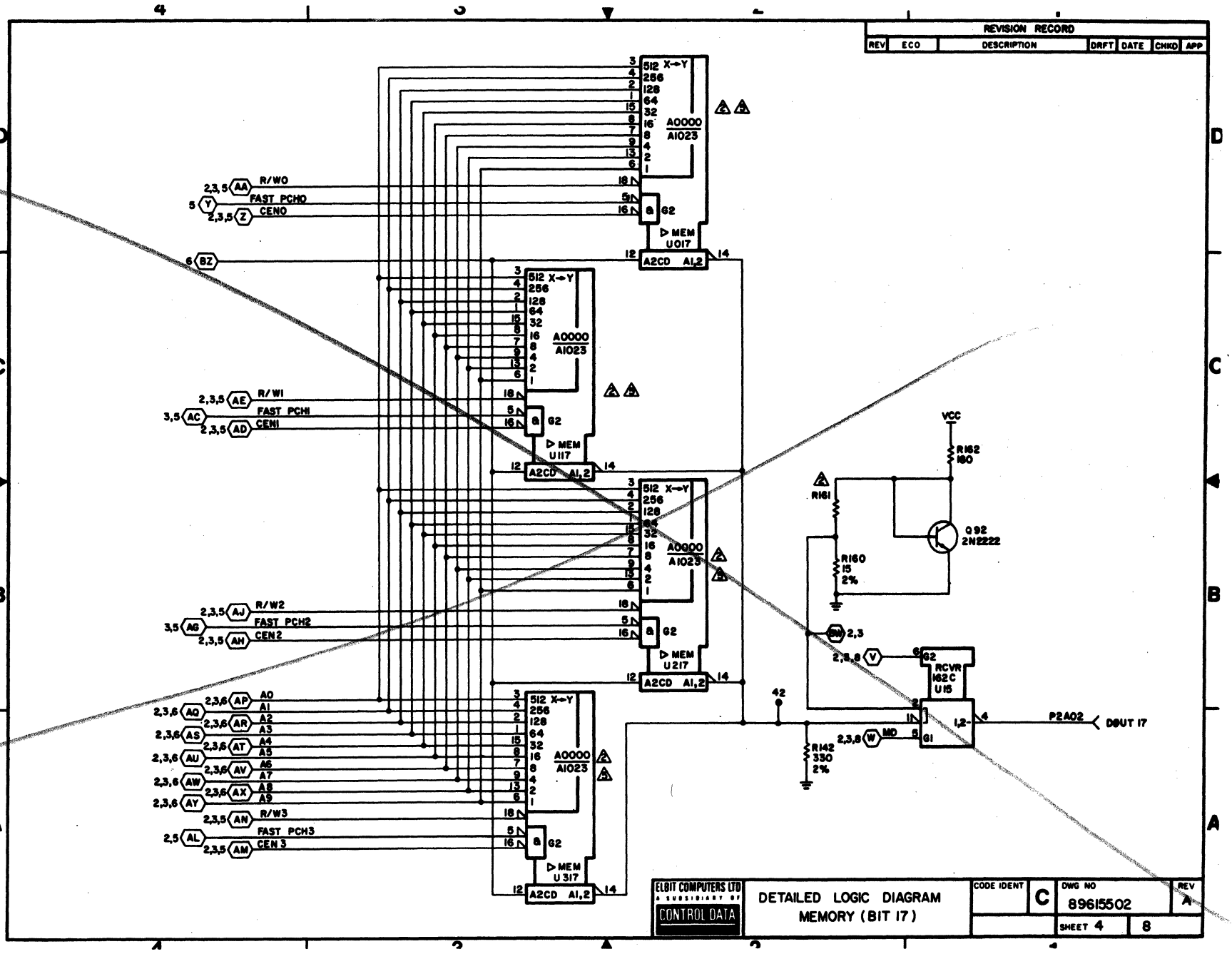
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

DETAILED LOGIC DIAGRAM
MEMORY
LEVEL SHIFTER CIRCUITS

CODE IDENT C | DWG NO 89615502 | REV D | SHEET 5



BIT	⚠	UB	PA	PB	PC	PD	DOUT	TPA	RA
1	BE	23	2	1	5	4	P1A04	6	R158
2	BB	22	11	12	8	9	P1A06	8	R157
3	BC	22	2	1	5	4	P1A08	10	R156
4	BD	21	11	12	8	9	P1A09	13	R155
5	BF	21	2	1	5	4	P1A14	15	R154
6	BG	20	11	12	8	9	P1A17	17	R153
7	BH	20	2	1	5	4	P1A19	19	R152
8	BJ	19	11	12	8	9	P1A20	21	R151
9	BK	19	2	1	5	4	P1A25	23	R150
10	BL	18	11	12	8	9	P1B24	25	R149
11	BM	18	2	1	5	4	P1A30	27	R148
12	BN	17	11	12	8	9	P1A31	29	R147
13	BP	17	2	1	5	4	P1B29	31	R146
14	BQ	16	11	12	8	9	P1B30	33	R145
15	BX	16	2	1	5	4	P1B31	36	R144
16	BY	15	11	12	8	9	P2A01	39	R143


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
512 X→Y
A0000
A1023
G2
MEM U017
A2CD A1,2
MEM U117
MEM U217
MEM U317
R/W0
FAST PCH0
CEN0
R/W1
FAST PCH1
CEN1
R/W2
FAST PCH2
CEN2
R/W3
FAST PCH3
CEN 3
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
VCC
R162 180
R161
Q 92 2N2222
R160 15 2%
R142 330 2%
RCVR 162 C U15
P2A02
DOUT 17
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
MEMORY (BIT 17)
CODE IDENT C
DWG NO 89615502
REV A
SHEET 4 8

ØFF SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4	5	6	7	8
A				D-4			D-1
B				C-4			D-1
D				C-4			D-2
E				C-4			D-1
F				C-4			C-2
J				C-4			C-1
K				B-4			C-1
L				B-4			C-1
M				B-4			C-1
N				B-4			C-2
P				B-4			B-1
Q				B-4			B-1
R				A-4			B-1
S				A-4			B-2
T				A-4			B-1
U				A-4			B-1
V	B-2	B-2	B-2				A-2
W	B-2	B-2	A-2				A-3
X	D-4	D-4		D-3			
Y			D-4	D-3			
Z	D-4	D-4	D-4	D-3			
AA	D-4	D-4	D-4	D-3			
AB	C-4			C-3			
AC		C-4	C-4	C-3			
AD	C-4	C-4	C-4	B-3			
AE	C-4	C-4	C-4	B-3			
AF	B-4			B-3			
AG		B-4	B-4	B-3			
AH	B-4	B-4	B-4	A-3			
AJ	B-4	B-4	B-4	B-3			
AK	A-4			A-3			
AL		A-4	A-4	B-3			
AM	A-4	A-4	A-4	A-3			
AN	A-4	A-4	A-4	A-3			
AP	B-4	B-4	A-4		D-3		
AQ	C-4	A-4	A-4		C-3		
AR	B-4	A-4	A-4		C-3		
AS	B-4	A-4	A-4		C-3		
AT	A-4	A-4	A-4		C-3		
AU	A-4	A-4	A-4		B-3		
AV	A-4	A-4	A-4		B-3		
AW	A-4	A-4	A-4		B-3		
AX	A-4	A-4	A-4		B-3		
AY	A-4	A-4	A-4		A-3		
BA	D-3		⚠1			C-1	
BB			⚠1			D-3	
BC			⚠1			D-2	

ØFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4	5	6	7	8
BD		⚠1				D-2	
BE		⚠1				D-3	
BF		⚠1				C-1	
BG		⚠1				C-3	
BH		⚠1				C-3	
AJ		⚠1				C-2	
BK		⚠1				C-2	
BL		⚠1				B-1	
BM		⚠1				B-3	
BN		⚠1				B-3	
BP		⚠1				B-2	
BQ		⚠1				B-2	
BW	B-2	B-2	B-2				
BX		⚠1			B-1		
BY		⚠1			A-3		
BZ			C-3		A-3		

SHEET REVISION STATUS

1	2	3	4	5	6	7	8
02	02	02	02	02	02	02	02
03	02	02	02	02	02	02	03
04	02	02	02	02	02	02	04
A	A	A	A	A	A	A	A
B	A	A	A	A	A	A	B

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
02	CK 364	REDRAWN PER CDC STD.	IONA	DEC 10		
03	CK 498	C 105 WAS 10μF, 35V	Aubrey Kagan	Feb, 74		E.H.
04	CK 621	R3 WAS 330 OHMS.	Aubrey Kagan	March, 14, 74		G.H.
05	CK 679	C68 DELETED				
06	CK 770	DETACHED LIST AW WAS 89616502 AY WAS 89633402				
07	CK 930	REVOL INSTR. INCORRECT AW WAS CORRECT AY WAS 89615302				
08	CK 978	R36, R39, R47, R60 WERE 1K, PIN 10 CAR B WAS CONNECTED TO L.S. OUTPUT	Aubrey Kagan	MAY 10 74	KH	Aubrey Kagan
A	CK 1126	RELEASED CLASS A PG.4 R160 WAS 15.4 OHMS PG.8 ADDED C93 BETWEEN VSS TO VDD.	M.L.	6/3/75	Mark	
B	CK 1209	SH.8 CAPACITORS BETWEEN VSS & VDD WERE 470PF (ZONE D-3).	M.L.	7.5.75	Mark	

NØTES:

1. ⚠1 REFER TØ TABLE ØN SHEET 3
2. ⚠2 THE FØLLØWING CØMPØNENTS HAVE DIFFERENT VALUES IN THE 900Nsec (EQUIPMENT BA 201-B) AND 600Nsec (EQUIPMENT BA-201A)

SHEET	CØMPØNENT	ASSY 89876300 (900NS)	89876600 (600 NS)	ELEMENT IDENTIFIER
8	C52, C53, C54, C55	270PF	39PF	
4	R161	56.2 OHMS ±2%	27.4 OHMS ±2%	
2	U000-U017 U100-U117 U200-U217 U300-U317	1103	1103-1	ARE PENDING

3. ⚠3 ALL UNMARKED DIØDES ARE IN4151
4. ⚠4 ALL UNMARKED RESISTØRS ARE 0.25 WATT 5%.
5. ⚠5

INTEGRATED CIRCUITS	VOLTAGE APPLIED	PIN NO.
U1-U10	Vccs	10
U11-U23	Vcci	10
U000-U017 U100-U117	Vss	17
U200-U217 U300-U317	Vdd	11
	Vbb	10

AW 89615402 | AY 89876300 | AY 89876600 | DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± | 2 PLACE ± | ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

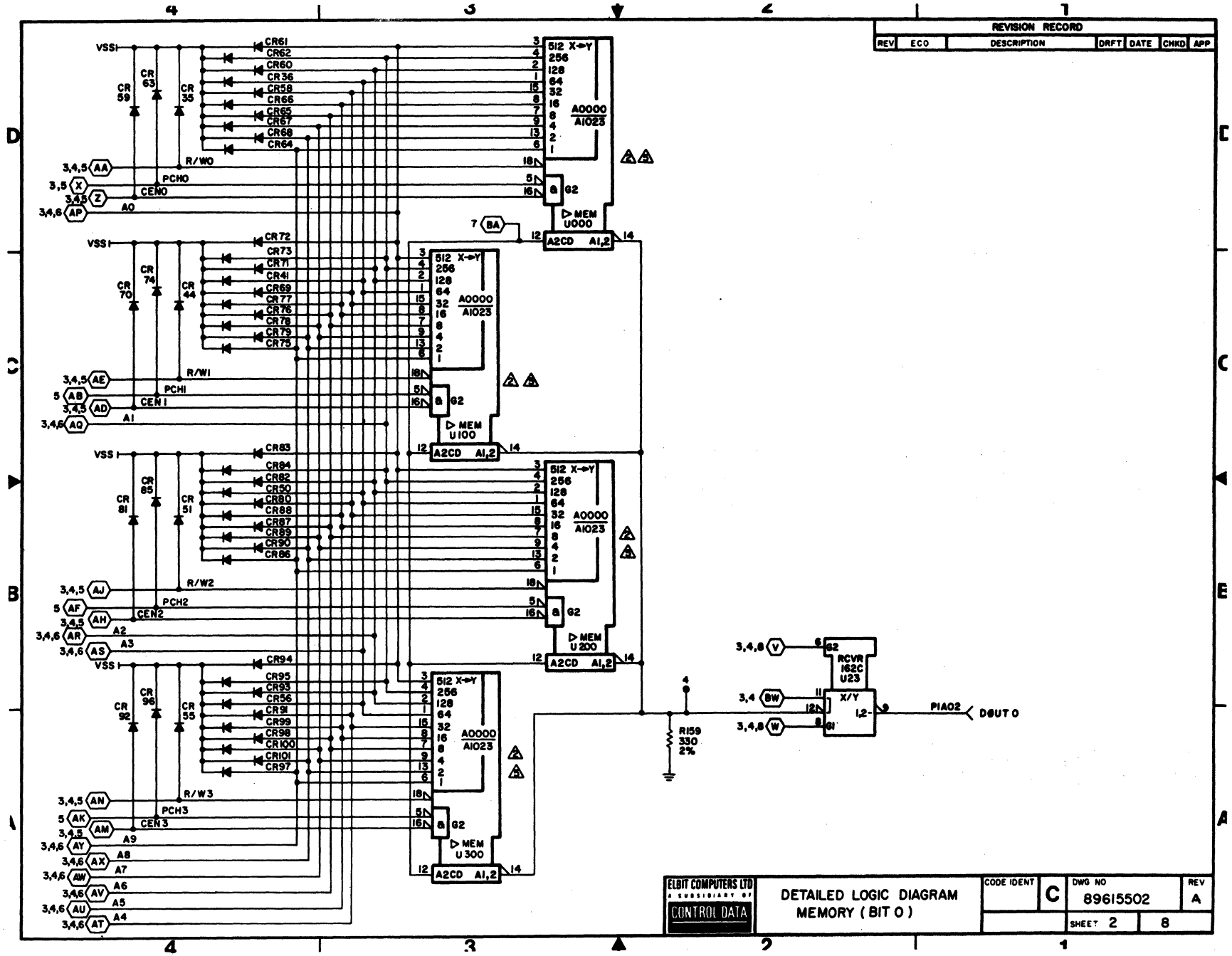
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

FIRST USED ON: BA 201-A, BA 201-B

DWN	IONA	DEC.
CHKD	Aubrey Kagan	DEC. 12 73
ENGR	SHMIT BZI	
MFG		
APPR	HAIM J. DEP	5.1.75
QA		

TITLE
DETAILED LOGIC DIAGRAM
MEMORY

CODE IDENT: C
DRAWING NO: 89615502
SCALE
SHEET 1 OF 8


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
VSS
CR61 CR62 CR60 CR36 CR58 CR66 CR65 CR67 CR68 CR64
CR 59 CR 63 CR 35
R/W0 PCH0 CEN0 A0
3,4,5 AA
3,5 X
3,4,5 Z
3,4,6 AP
512 X→Y 256 128 64 32 16 8 4 2 1
A0000 A1023
G2
MEM U000
7 BA
A2CD A1,2
CR72 CR73 CR71 CR41 CR69 CR77 CR76 CR78 CR79 CR75
CR 70 CR 74 CR 44
R/W1 PCH1 CEN1 A1
3,4,5 AE
5 AB
3,4,5 AD
3,4,6 AQ
MEM U100
CR83 CR84 CR82 CR50 CR80 CR88 CR87 CR89 CR90 CR86
CR 81 CR 85 CR 51
R/W2 PCH2 CEN2 A2 A3
3,4,5 AJ
5 AF
3,4,5 AH
3,4,6 AR
3,4,6 AS
MEM U200
CR94 CR95 CR93 CR56 CR91 CR99 CR98 CR100 CR101 CR97
CR 92 CR 96 CR 55
R/W3 PCH3 CEN3 A9 A8 A7 A6 A5 A4
3,4,5 AN
5 AK
3,4,5 AM
3,4,6 AY
3,4,6 AX
3,4,6 AW
3,4,6 AV
3,4,6 AU
3,4,6 AT
MEM U300
R159 330 2%
3,4,6 V
3,4 BW
3,4,6 W
RCVR I62C U23
X/Y
PIA02
DBUT 0
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
MEMORY (BIT 0)
CODE IDENT C
DWG NO 89615502
REV A
SHEET 2 8

MEMORY MODULE (drawing 89615502)

Power supply considerations

Between V_{SS} and V_{BB} the memory unit presents the equivalent of a silicon junction diode, which is reverse biased under normal operating conditions. During power supply turn on, V_{BB} should rise at least as fast as V_{SS} and during operation V_{BB} should not fall below V_{SS}. To insure proper V_{BB} regulation and to guarantee these turn-on characteristics, V_{BB} is generated by regulating V_{SS} at 3-4V below V_{BB}. Because the memory unit draws very little current from V_{BB} protective series resistance used; V_{BB} is adequately bypassed to V_{SS} at the unit, and level shifters connected to V_{BB} are connected to the power supply side of the series resistance.

ØFF SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4	5	6	7	8
A				D-4			D-1
B				C-4			D-1
D				C-4			D-2
E				C-4			D-1
F				C-4			C-2
J				C-4			C-1
K				B-4			C-1
L				B-4			C-1
M				B-4			C-1
N				B-4			C-2
P				B-4			B-1
Q				B-4			B-1
R				A-4			B-1
S				A-4			B-2
T				A-4			B-1
U				A-4			B-1
V	B-2	B-2	B-2				A-2
W	B-2	B-2	A-2				A-3
X	D-4	D-4		D-3			
Y			D-4	D-3			
Z	D-4	D-4	D-4	D-3			
AA	D-4	D-4	D-4	D-3			
AB	C-4			C-3			
AC		C-4	C-4	C-3			
AD	C-4	C-4	C-4	B-3			
AE	C-4	C-4	C-4	B-3			
AF	B-4			B-3			
AG		B-4	B-4	B-3			
AH	B-4	B-4	B-4	A-3			
AJ	B-4	B-4	B-4	B-3			
AK	A-4			A-3			
AL		A-4	A-4	B-3			
AM	A-4	A-4	A-4	A-3			
AN	A-4	A-4	A-4	A-3			
AP	D-4	B-4	A-4		D-3		
AQ	C-4	A-4	A-4		C-3		
AR	B-4	A-4	A-4		C-3		
AS	B-4	A-4	A-4		C-3		
AT	A-4	A-4	A-4		C-3		
AU	A-4	A-4	A-4		B-3		
AV	A-4	A-4	A-4		B-3		
AW	A-4	A-4	A-4		B-3		
AX	A-4	A-4	A-4		B-3		
AY	A-4	A-4	A-4		A-3		
BA	D-3		⚠1			C-1	
BB			⚠1			D-3	
BC			⚠1			D-2	

ØFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4	5	6	7	8
BD		⚠1				D-2	
BE		⚠1				D-3	
BF		⚠1				C-1	
BG		⚠1				C-3	
BH		⚠1				C-3	
AJ		⚠1				C-2	
BK		⚠1				C-2	
BL		⚠1				B-1	
BM		⚠1				B-3	
BN		⚠1				B-3	
BP		⚠1				B-2	
BQ		⚠1				B-2	
BW	B-2	B-2	B-2				
BX		⚠1			B-1		
BY		⚠1			A-3		
BZ			C-3		A-3		

SHEET REVISION STATUS

1	2	3	4	5	6	7	8
D				D			
E							
04	02	02	02	02	02	02	04
A	A	A	A	A	A	A	A
B	A	A	A	A	A	A	B

CAAAAAA

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
02	CK 364	REDRAWN PER CDC STD.	IONA	DEC 10		
03	CK 498	C 105 WAS 10μF, 35V				
04	CK 621	R3 WAS 330 ØHMS.				G.H.
05	CK 673	C68 DELETED				
06	CK 770	DETACHED LIST AW WAS 89615502 AY WAS 89639402				
07	CK 930	REV 06 INSTR. INCORRECT AW WAS CORRECT AY WAS 89615302				
08	CK 978	R38, R39, R47, R50 WERE 1K, P/N 19. CR8 WAS CONNECTED TO L.S. OUTPUT		NOV. 10 74		
A	CK 1126	RELEASED CLASS A PG. 4 R160 WAS 15.4 ØHMS PG. 8 ADDED C93 BETWEEN VSS TO VDD.	M.L.	6/3/75		
B	CK 1209	SH. 8 CAPACITORS BETWEEN VSS & VDD WERE 470 PF (ZONE D-3).	M.L.	7.8.75		
C	CK 1306	SH8: VALUE OF C93 CORRECTED.				
D	CK 1436	R.C.O. SH5.				
E	CK 1830	TO MATCH MFD. PWA'S: SH 1, NOTE 2: 900NS: 89876600 RE-PLACES 89876300 600NS: 89876300 RE-PLACES 89876600				

NØTES:

1. ⚠1 REFER TØ TABLE ØN SHEET 3
2. ⚠2 THE FØLLØWING CØMPØNENTS HAVE DIFFERENT VALUES IN THE 900Nsec (EQUIPMENT BA 201-B) AND 600Nsec (EQUIPMENT BA-201A)

SHEET	CØMPØNENT	900NS PWA 89876600	600NS PWA 89876300	ELEMENT IDENTIFIER
8	C52, C53, C54, C55	270PF	39PF	
4	R161	56.2 OHMS ±2%	27.4 OHMS ±2%	
2	U000-U017 U100-U117 U200-U217 U300-U317	1103	1103-1	ARE PENDING

3. ⚠3 ALL UNMARKED DIØDES ARE IN4151
4. ⚠4 ALL UNMARKED RESISTØRS ARE 0.25 WATT 5%.
5. ⚠5

INTEGRATED CIRCUITS	VOLTAGE APPLIED	PIN NO.
U1-U10	Vcc5	14
U11-U23	Vcc1	14
U000-U017 U100-U117 U200-U217 U300-U317	Vss	17
	Vdd	11
	Vbb	10

AW 89615402 (600NS)
AY 89876300 (600NS)
AY 89876600 (900NS)
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES
TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

FIRST USED ON BA201-A (600NS) BA201-B (900NS)

DWN	IONA	DEC.
CHKD	Aubrey Kagan	DEC. 12 75
ENGR	SNYIT RLI	
MFG		
APPR	HAIM T.	
Q.A		

TITLE
DETAILED LOGIC DIAGRAM
MEMORY

CODE IDENT: C
DRAWING NO: 89615502
SCALE
SHEET 1 OF 8

MEMORY MODULE (drawing 89615502)

PROTECTION AGAINST CATASTROPHIC FAILURE

Capacitive coupling circuit

The MOS-level signal, after the level shifter, is fed to the precharge line on all memory modules. This line includes a capacitive coupling circuit, which protects the memory chips from catastrophic damage. Power dissipation in the chip is a function of precharge duty cycle. If a precharge driver fails or remains active (low output) for too long, the memory units may overheat and be destroyed. However, with the capacitive coupling circuit, the precharge is pulled up even if the level shifter output continues to remain low. The capacitive coupling circuit does not slow down the precharge signal in operation.

A series termination resistor (22 ohm) connects the MOS-level signals to the memory chips, after the capacitive coupling circuit. The signals run down the 18-bit kiloword bus, connecting to each memory chip. The address lines branch into 4 groups, each running down a separate 18-bit kiloword line. A clamping diode is connected at the end of each line to V_{SS} to prevent the signal from exceeding V_{SS}. There is one diode for each kiloword line, that is, a total of 4 diodes are located on the address lines.

For bit 17 (protect bit), the one physically closest to the level shifters, the precharge signal is connected directly after the capacitive coupling device without series termination. This decreases precharge overlap time due to line reflections, and thereby decreases data output time for bit 17.

MEMORY MODULE (drawing 89615502)

Power supply considerations

Between V_{SS} and V_{BB} the memory unit presents the equivalent of a silicon junction diode, which is reverse biased under normal operating conditions. During power supply turn on, V_{BB} should rise at least as fast as V_{SS} and during operation V_{BB} should not fall below V_{SS}. To insure proper V_{BB} regulation and to guarantee these turn-on characteristics, V_{BB} is generated by regulating V_{SS} at 3-4V below V_{BB}. Because the memory unit draws very little current from V_{BB} protective series resistance used; V_{BB} is adequately bypassed to V_{SS} at the unit, and level shifters connected to V_{BB} are connected to the power supply side of the series resistance.

MEMORY MODULE (drawing 89615502, sheets 3,4)

Sense Amplifiers

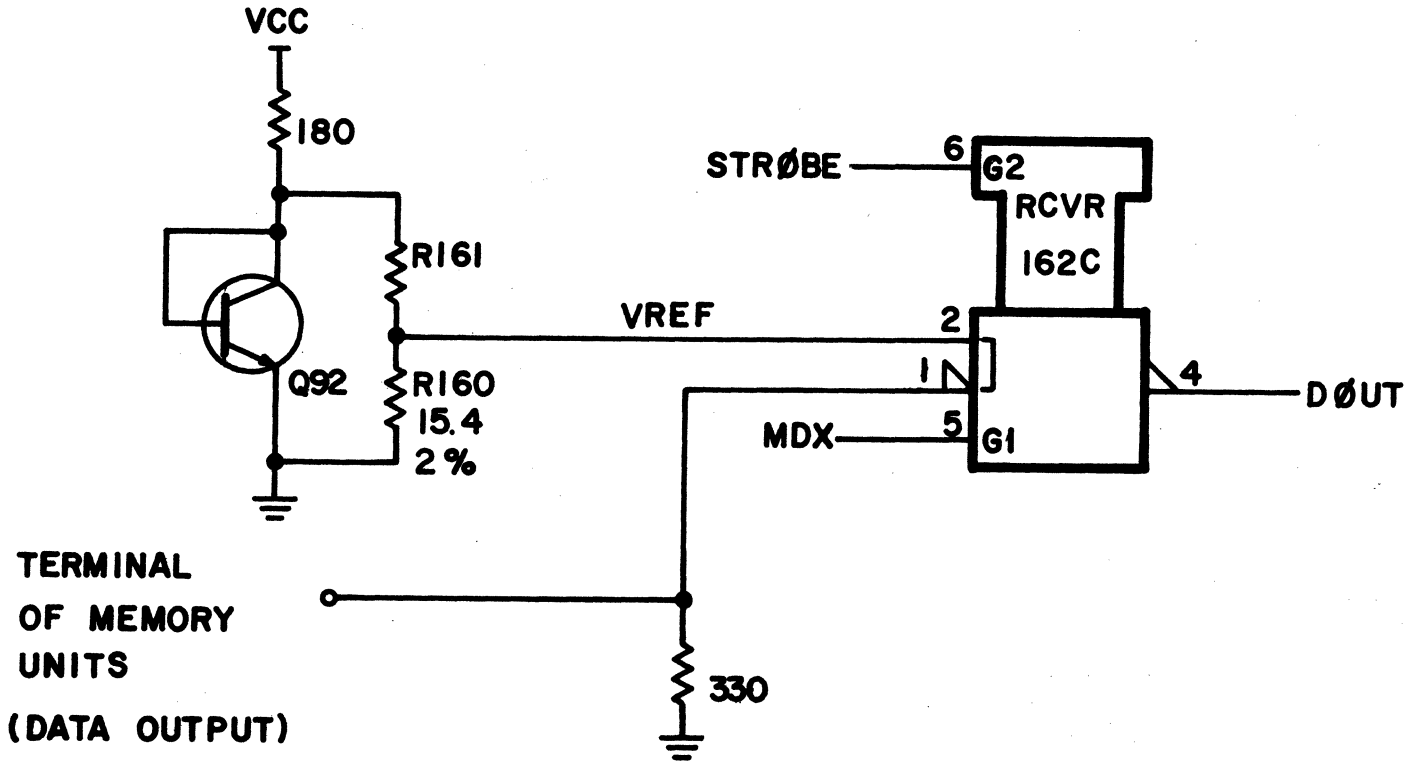
The data output (terminal 14) of the memory units appears on an open collector. The output pins of corresponding bits of the four kilowords on the module are wire-ORed to form the 18 output lines of the Memory Module. Each wired-OR is taken through a 330 ohm resistor to ground which converts the current source output of the memory unit to a voltage level. This voltage level is fed to a differential sense amplifier (receiver unit 162C) whose output is the DØUT line. The other input of the receiver is connected to a reference voltage. This reference voltage is determined by the two resistors acting as a divider on V_{cc} using Q92. The value of the reference voltage (VREF) differs in the high speed and low speed units:

- BA201-A: VREF = 110 mV
- BA201-B: VREF = 50 mV

The data output is activated by the cell enable (Cenable) signal to the memory unit.

The output of the sense amplifier is not enabled unless the $\overline{\text{STROBE}}$ is low (during clocks 5 - 10) and the module was selected ($\overline{\text{MDX}}$ low). When the sense amplifier is not enabled, its output is high. Pull-up resistors located on the Memory Control assembly pull the DØUT lines to V_{cc}.

MEMORY MODULE (drawing 89615502, sheets 3,4)



Note:

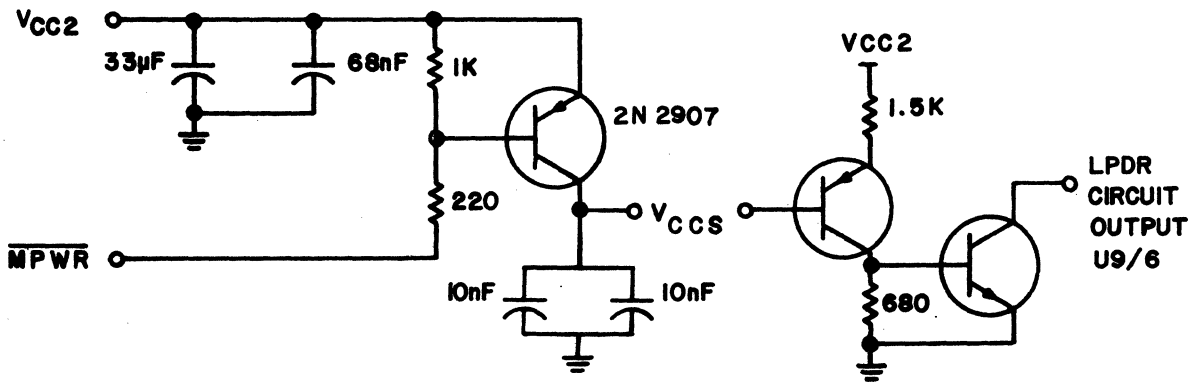
	Equipment	
	BA201-B	BA201-A
R161	56.2 ohms ± 2%	27.4 ohms ± 2%
VREF	50 mV	110 mV

Data-Out Sense Amplifier Circuit Diagram

MEMORY MODULE (Drawing 89615502, sheet 8)

Low Power Data Retention

Between refresh cycle bursts in the Low Power Data Retention (LPDR) made during a power failure, none of the TTL logic circuits receive power. This circuit ensures that the Precharge and Cenable signals do not activate as the V_{cc} is switched "on". It achieves this by keeping the enabling inputs of the Precharge output gates low (at U9/6).



Switched Supply (V_{CCS}) and LPDR Circuit

The circuit senses that the switched logic supply (V_{CCS}) dropped, and, with a short delay, holds U9/6 low; when V_{CCS} rises, the circuit releases U9/6, after a short delay. The attack time of the circuit (the time allowed between V_{CCS} dropping and U9/6 being held low) is 10 milliseconds. The release time is determined by the Disable signal: Disable will not go active (low) for 1.6 milliseconds after $\overline{MPWF}$ is active (that is V_{CCS} is active, thus the circuit has 1.6 milliseconds before it must release U9/6.

MEMORY MODULE (drawing 89615502, sheet 8, cont'd)

The main logic supply (V_{CC}) may fail during normal operation. This will not affect memory operation if the optional back-up source, battery equipment GD611 is installed. In this case the computer switches to Low-Power Data Retention (LPDR) mode and to conserve power the following TTL circuits are connected to the switched logic supply (V_{CCS}):

- Column address (A5 - A9)
- Data-in level shifters
- Data-out sense amplifiers

During intercycle refresh bursts, all circuits not directly involved are switched off by V_{CCS}. The outputs level of the shifters to precharge, Cenable and R/W continue, however, to remain high.

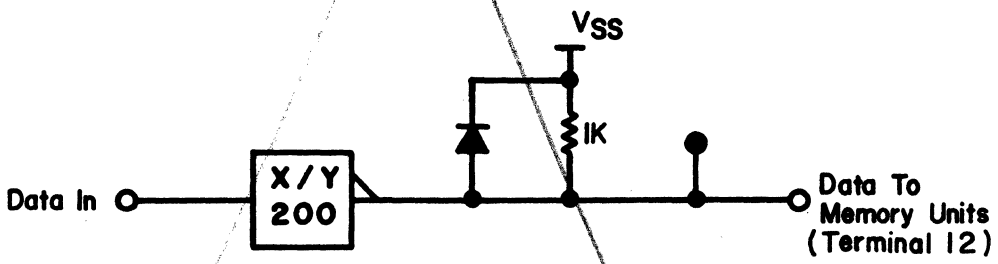
Address Level Shifters

To avoid long transmission paths on the memory module assembly five of the addresses, located far from the connector, have two TTL inverters instead of the usual one.

MEMORY MODULE (drawing 89615502, sheet 7)

Data-In Level Shifters

The level shifters for the data input to each memory unit is an open collector inverter with a 1 Kilohm pull-up resistor to V_{SS}. The DATA IN (DIN) lines are normally low. When a DATA-IN line becomes active (high) during a write cycle, the information on it is immediately valid. The outputs of the data-in level shifters have a fast fall time, but a comparatively slow rise time, making them suitable for this signal polarity.



Data-in Level Shifter and Clamp

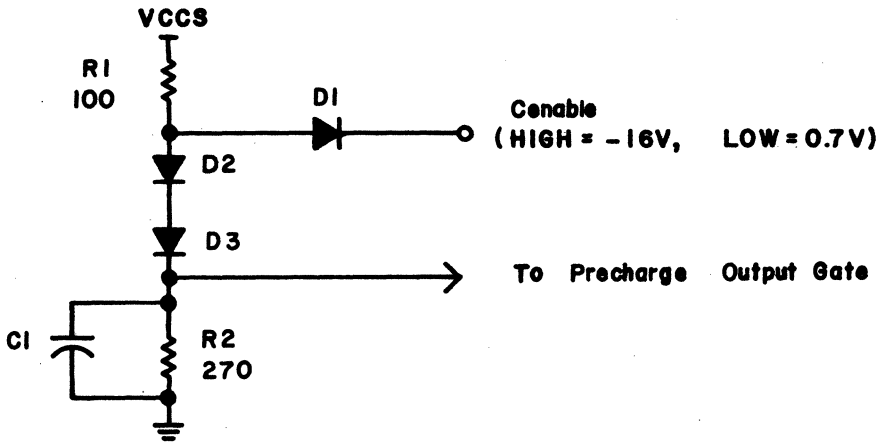
MEMORY MODULE (drawing 89615502, sheets 5,8)

The Overlap Circuit (Cenable - Precharge Delay)

One overlap delay circuit is in the precharge line of each kiloword unit on the Memory Module. It regulates the overlap timing t_{OVL} and t_{OVH} in the memory units (see Table 4-2 and the Detailed Operation of the Memory Unit), and consists of a diode switching network controlling an RC delay circuit.

The circuit is shown below. In normal operation Cenable at the output of a level shifter is high, blocking diode D1 and so allowing a voltage of about 2 volts to develop on the delay network (C1, R2). This voltage enables the precharge output gate.

When the Cenable line is activated (gone low), diode D1 conducts and blocking diodes D2, D3 isolate the delay circuit. The voltage to the precharge unit decays with the time constant of the delay circuit so ending the precharge signal.



Overlap (Cenable-Precharge Delay) Circuit: Circuit Diagram

MEMORY MODULE (drawing 89615502, sheet 5)

Level Shifters: TTL to MOS

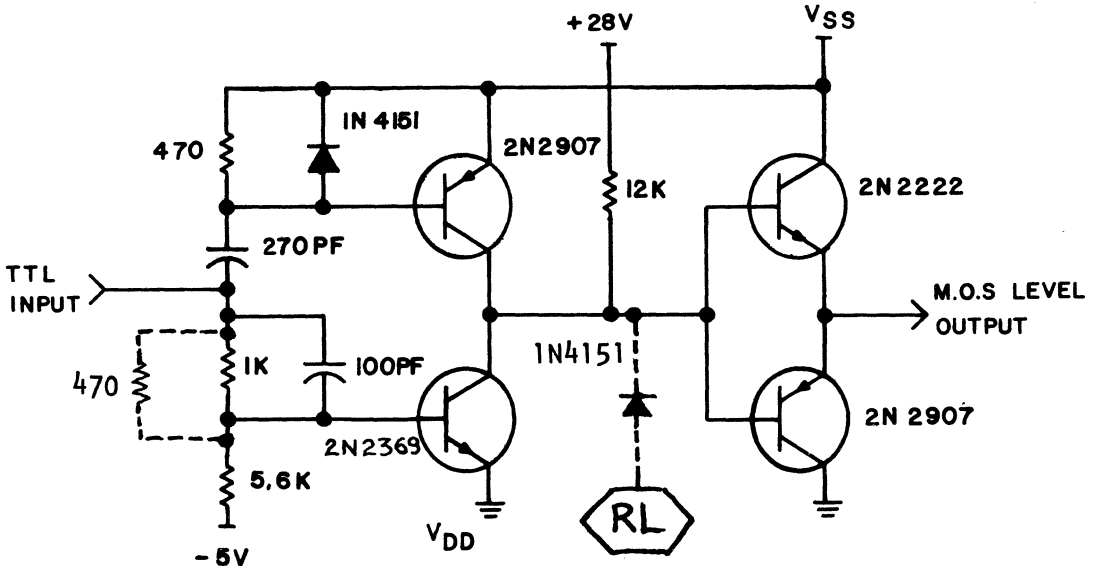
TTL logic levels are 0.7 volts (low) and 2.0 volts (high). MOS levels are approximately zero volts to V_{SS} (16 volts). A level shifter is needed to match the two kinds of logic circuits. The following signals use identical level shifters:

Precharge, Read/Write (R/W) and Address

These level shifters are common emitter push-pull inverting amplifiers, using four transistors. They accept TTL input and provide an output to drive MOS circuitry, that is, they drive a 300 pf load in 45 nanoseconds. Two capacitors are used to speed up the operation. The use of -5V and +28V power supplies improves delay and rise-fall times. See page 4-34.

The Cenable 0, 1, 2, 3 signals use the above type of level shifter, but with two components added: a 470-ohm resistor and a type 1N4151 diode. The resistor and diode are connected for the Cenable level shifters only. To indicate this, they are drawn in dashed lines in the circuit diagram below.

In logic drawing 89615502 sheet 5, the 470-ohm resistor is marked RE and the type 1N4151 diode is marked CRB.

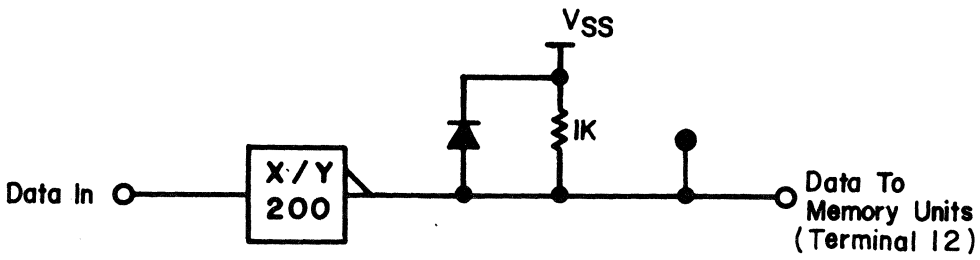


TTL to MOS Logic Level Shifter Circuit Diagram

MEMORY MODULE (drawing 89615502, sheet 7)

Data-In Level Shifters

The level shifters for the data input to each memory unit is an open collector inverter with a 1 Kilohm pull-up resistor to V_{SS}. The DATA IN (DIN) lines are normally low. When a DATA-IN line becomes active (high) during a write cycle, the information on it is immediately valid. The outputs of the data-in level shifters have a fast fall time, but a comparatively slow rise time, making them suitable for this signal polarity.



Data-In Level Shifter and Clamp

MEMORY MODULE

The Memory Module circuits are accommodated on a single 50-PAK printed wiring board. The logic circuit diagrams are given in drawing number 89615502, sheets 1-8.

The equipments, BA201-A and BA201-B are both designated Memory Modules. The difference in function between the two equipments is their speed of operation expressed in terms of the memory read/write cycle time, as follows:

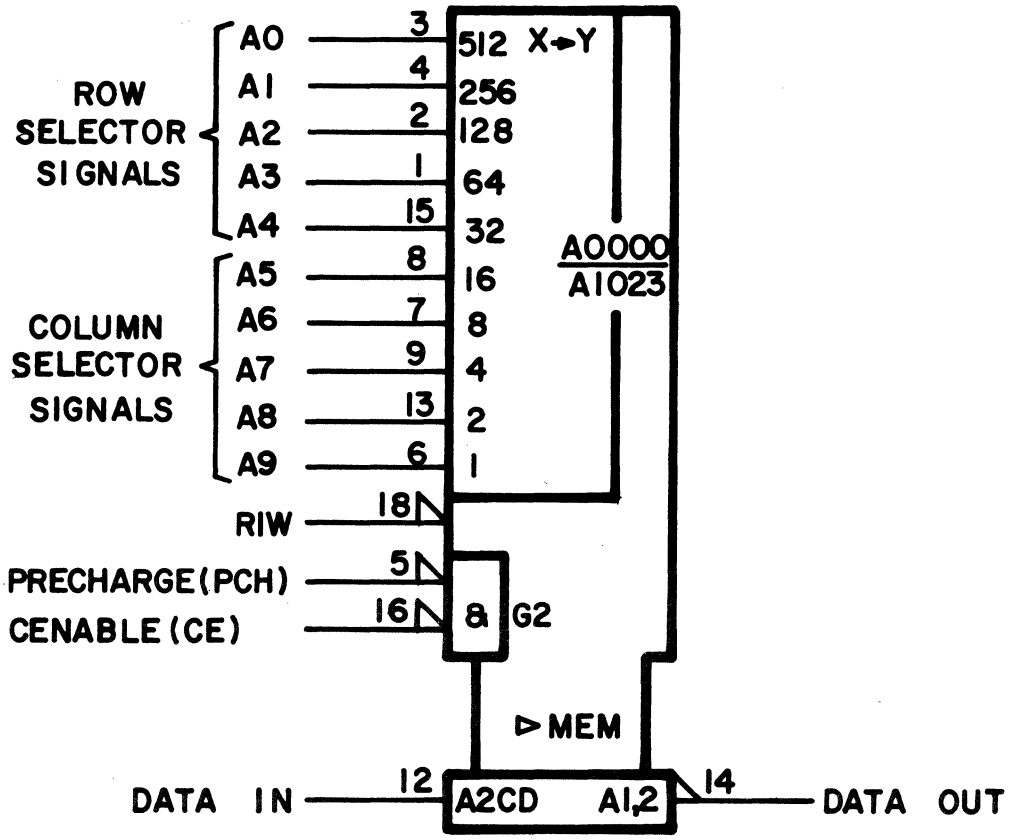
Memory Module Equipment	Cycle Time	Accommodated in Equipment
BA201-A	600 nsec	AB108, BT148
BA201-B	900 nsec	AB107, BT148

The memory module, as part of the memory system is described in Section 4 of this manual.

The principles of operation and circuit configuration of the two equipments are identical. The component memory units they utilize are similar and differ only in their speed of operation (refer to Section 4 of this manual for detailed operation and timing). Changes in the values of other components between the two equipments are noted on sheet 1 of drawing 89615502.

The memory module block diagram is described in Section 4 of this manual. Detailed circuit diagrams are given here. The circuits are repetitive and for bits 1 through 16 they are identical. Only one circuit diagram is given therefore and it is supplemented by tables defining each component.

The level shifters and other circuits which make up the memory module are described in the following. The memory unit is described in detail in Section 4. Its terminal functions are summarized in the following diagram.



SUPPLIES

SUPPLY	VOLTAGE	TERMINAL
VSS	+19.7V(BA201-A)	17
	+16.7V(BA201-B)	17
VBB	VSS +3V	10
VDD	GROUND	11

Memory Unit External Connectors

MEMORY SYSTEM

The memory system consists of the printed wiring assemblies (PWA's) listed in the following table:

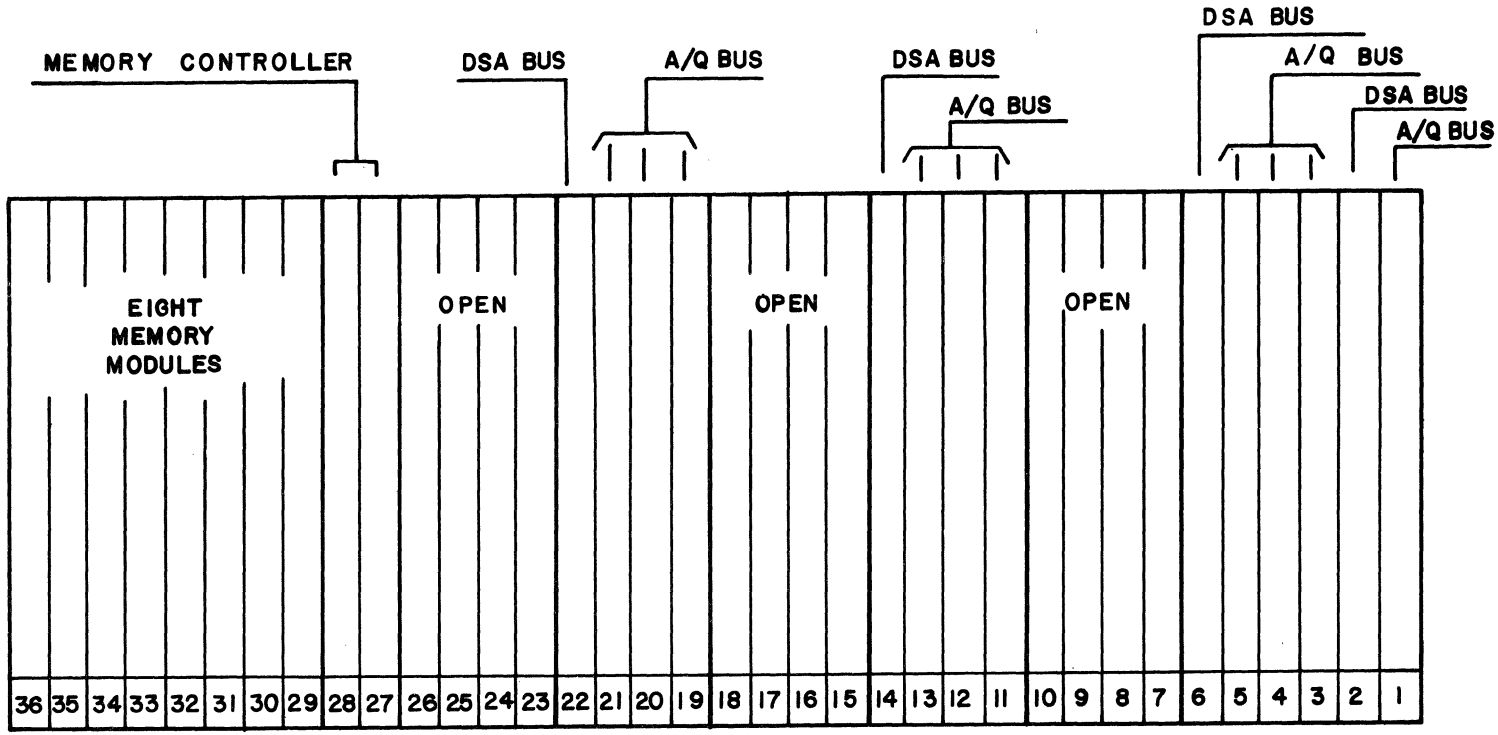
Designation	Slot Location	Remarks
Memory Module	29 through 36	Equipment BA201-A or BA201-B
Memory Address	28	)
Memory Control	27	) Memory Controller System PWA's

Notes:

1. The slot allocation is identical in equipments AB107/AB108, BT148.
2. The Memory Controller system in the expansion enclosure is equipment BU120-A. It is similar to the Memory Controller used in equipments AB107/AB108.

The memory timing is shown in figure 4-6 and in the timing diagram associated with sheet of the Memory Control assembly.

"Pages 5-9 to 5-18 are unassigned."



NOTES 1. The Memory Control assembly and the Memory Address assembly together form the Memory Controller, equipment number BU120-A.

2. See section 1 for definition of equipments.

3. Slot 25 is provided with an additional connection to logic ground at 25P1A03. Slot 26 is provided with an additional connection to logic ground at 26P2B06.

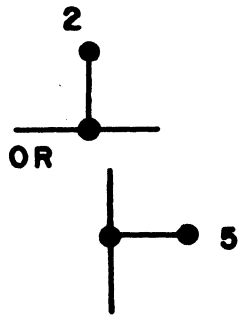
Card Placement Slot Assignment - Expansion Enclosure

DIAGRAM REVISION CORRELATION SHEET

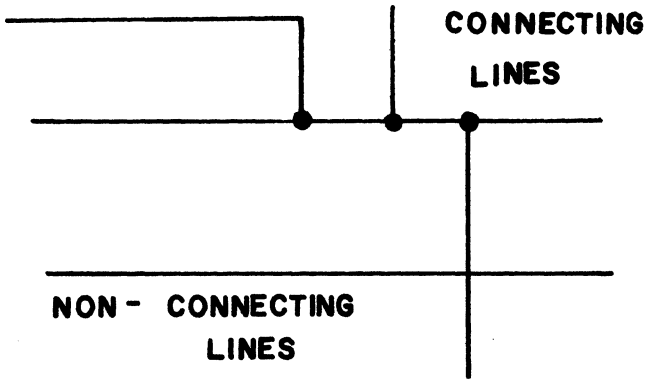
The following is a numerical list of the logic diagrams (prefix LD) and the wiring diagrams (prefix WD) included in section 5, with the revision status for revision F of this manual. See the table of contents.

NUMBER-REVISION	NAME
WD 89601601 - A	Power Supply Wiring
LD 89614300 - A	Arithmetic Logic Unit (ALU)
LD 89614900 - A	Decoder
LD 89615200 - A	Memory Address
LD 89615502 - E	Memory
LD 89616400 - J	TTY Controller
LD 89616400 - H	TTY Controller
LD 89616400 - G	TTY Controller
LD 89616400 - F	TTY Controller
LD 89617000 - A	Timing
LD 89618800 - B	Console Interface
LD 89619100 - C	Memory Control
LD 89619700 - A	Input/Output (I/O) Interface
LD 89640500 - B	Programmer's Console
LD 89640501 - A	Programmer's Console
LD 89640502 - A	Programmer's Console
LD 89640800 - D	LP Card - Power Supply
LD 89657700 - B	HP Control Unit
WD 89762200 - 05	Power Supply Input-Output Wiring
WD 89911800 - B	Power Supply Wiring
WD 89942600 - A	Power Supply Input-Output Wiring
LD 89982800 - A	Anti-Bounce Circuit

Test Points



The test point symbol on the logic diagram shows the connections of a test point on the printed wiring board (PWB). The number adjacent to the symbol refers to the test point position on the PWB at the edge opposite the connectors. Only test point number one is labeled on the edge of the PWB, the other test point are numbered sequentially.



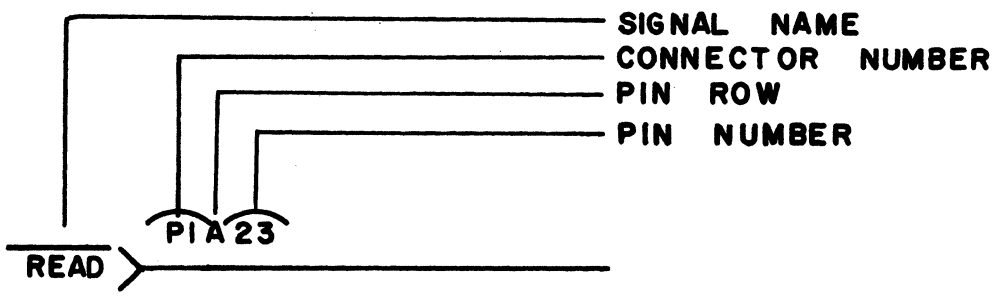
Connecting and Non-Connecting Lines

Lines connected to a common point or at a junction point are shown in the upper part of this illustration. No more than three lines are normally connected to a common point in the diagrams.

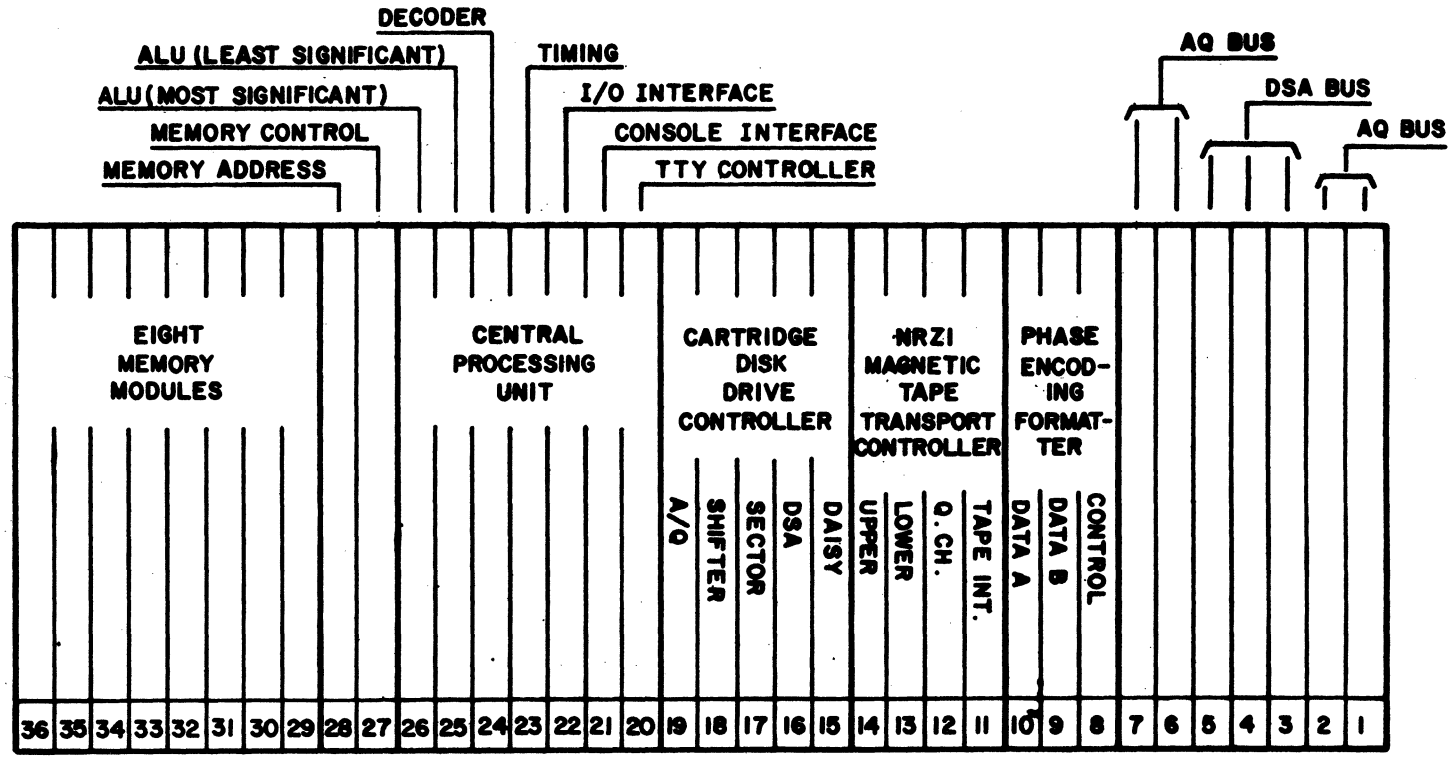
Lines crossing but not connected are shown in the lower part of this illustration.

Connectors

All PWB connectors are sockets (female) and are shown as such. The name of the signal is placed in the open end of the connector symbol (shown below), using the full name of the signal or the common abbreviation applicable to logic diagrams. The connector number, pin row and pin numbers are located above the line extending from the connector symbol. Refer to Input/Output specification manual publication number 89673100 for an explanation of the mechanical location of connector pins.



Card Placement Slot Assignment
Main Computer Enclosure



NOTES

1. The Memory Control assembly and the Memory Address assembly together form the Memory Controller. This is similar to equipment BU120-A in the Expansion Enclosure.
2. See Section 1 for definition of equipments.

KEY TO LOGIC SYMBOLS

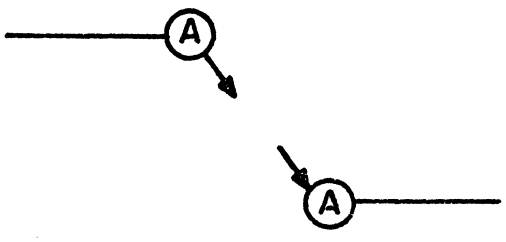
Publication 89723700 (Key to Logic Symbols) or equivalent, lists the symbols used in the logic diagrams in this manual and gives a short description of the functions they represent. The symbols conform generally to Control Data usage (Microcircuit Handbook, publication number 15006100), using the polarity logic convention.

The following paragraphs describe the signal flow conventions used.

SIGNAL FLOW

Input signals are drawn coming from the left or above; output signals are drawn going to the right or down.

The signal lines are sometimes interrupted to allow logical grouping of components and to avoid long lines. At each such interruption one of the following indicators is used:



On-Sheet Continuation Reference Symbols

These symbols when used with the logic symbols in the following diagrams indicate that a connection exists between two points on a sheet. The arrows attached to each circle point from signal origin to signal destination. The letters, C, H, I, O and P are not used inside the circles, since they bear special significance on logic diagrams.

(ON SHEET 2)

(ON SHEET 6)

Off-Sheet Continuation Reference Symbols

These symbols when used with the logic symbols in the following diagrams indicate two sheets in a series of related drawings. These symbols point from output to direction of input as shown in the illustration. The number(s) next to each hexagon indicate the sheet(s) that the signal is continued from or on. For instance, the numbers 3.6 refer to sheets 3 and 6, while 2.3 refers to sheets 2 and 3. It should be noted that the referenced sheet number(s) is always placed opposite the line extending from the hexagon.

OFF-SHEET REFERENCE LETTER	SIGNAL	SHEET			
		2	3	4	5
A	BIT3	D-1▼			
B	BIT2	C-1▼			
C	BIT1	B-1▼			
D	BIT0	A-1▼			
E	PTADD	D-2	D-2		
F	QTADD	D-2	D-1		
G	KTADD	D-2	D-2		
	MTADD	A-2	D-2		

The interconnections are listed in an Off-Sheet Reference table in the logic diagrams. This table gives the location of the off-sheet reference on each sheet and generally indicates the signal on which the signal originates (▼). The signal name at the interconnection is also generally given in the table when available.

SECTION 5

INTRODUCTION

This section carries the explanation of the detailed logic and circuit diagrams relating to equipments AB107/AB108 and BT148. These equipments are described in Section 1 of this manual; their theory of operation is given in Section 4.

The explanation is grouped in functional units, as follows:

Notes:

1. All units, except the Power Supply assembly and Programmer's Console, are mounted in slots in the main body of the enclosure (refer to card placement slot assignment, pages 5-6, 5-7). The order of the explanation follows the reverse order of slot assignments.

2. The Memory Controller, (consisting of the Memory Address and Memory Control boards) as equipment BU120-A is installed in the BT148 enclosure.

3. The calibration of the Power Supply unit is different in the AB107 and the AB108 equipments. The following table gives a summary:

EQUIPMENT	CALIBRATION
AB107 and BT148 connected to it	V_{SS} = +16.7 V
AB108 and BT148 connected to it	V_{SS} = +19.7 V

This information is given in other parts of the manual as required. See the Diagnostics and Margin Tests on page 6-7.

The diagrams, together with their latest revision status, are listed in the Revision Correlation Sheet. The diagrams themselves are not bound in this manual, but are packaged separately.

An explanation of symbols used in the diagrams is given in the Key to Logic Symbols and Signal Flow.

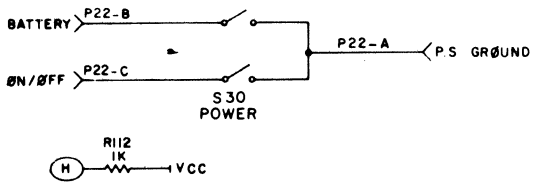
SECTION 5

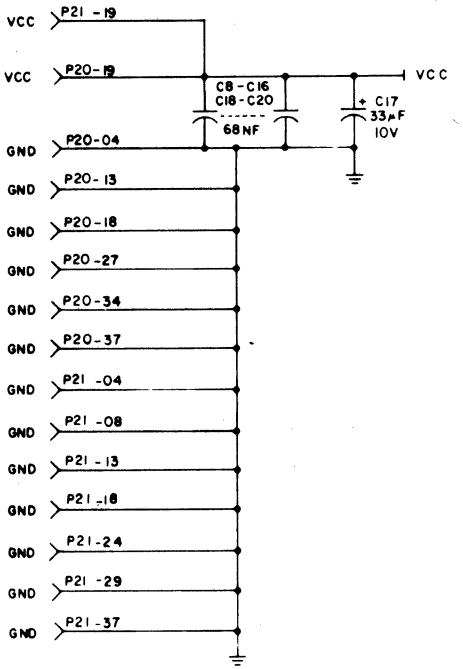
DIAGRAMS

89633300 G

ØFF - SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4
A	A-1	A-3	
B	B-1	A-2	
D	D-2		C-4





SHEET REVISION STATUS				REVISION RECORD						
1	2	3	4	REV	ECO	DESCRIPTN	DRFT	DATE	CHKD	APP
08	08	08	08	00	CK 1109	REVISED AND REDRAWN ALL OUTPUTS REVISED FITS PWA 89884000 REV 01. PG 4 (U16) ADDED TO RESOLVE GO SWITCH AND MANUAL INTERRUPT PROBLEM. OUTPUT EXT PNUT ADDED TO N2116	Lief	Jan 75		
				B	CK 1431	PG 3 ZONE 4 "NOT" SIGNAL ADDED TO S15, S16, S20-S24. FUNCTION NAMES ON S12 & S13, S20 & S21 REVERSED. SH 4. ADD'L CHANGE TO RESOLVE GO SWITCH & MI PROBLEM, R78, R80 WERE 1K OHM. C23, C24 WERE 10 NF R113, R114 ADDED	Hoy	29 Jan 75	SK	

BBBB

NØTES

1. C1-C7 ARE 1nF
2. ALL RESISTØRS ARE 0.25 WATT 5%.
3. R1-R17, R34-R50 AND R97-R103 ARE 180 ØHMS.
4. R18-R33, R114, R113 ARE 330 ØHMS.
5. R51-R74, R76, R77, R79, R81-R96, R112 ARE 1K ØHMS.
6. R104-R110 ARE 560 ØHMS.
7. R75 AND R111 ARE 33K ØHMS.
8. C23, C24 ARE 100 nF.
9. C21, C22 ARE 0.47 MF.
10. R78, R80 ARE 5.6 K ØHMS.

AY 89602068

A W 8988:900 DETACHED LISTS

DIMENSIONS ARE IN INCHES TOLERANCES 3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL

FINISH

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA

FIRST USED ON AB107-A /B

DWN		Jan 75
CHKD		
ENGR		JAN 75
MFG		
APPR		

TITLE

DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE

CODE IDENT C

DRAWING NO 89640500

SCALE

SHEET 1 OF 4

5-145/5-146

Logic Diagram 89640500, Sheet 1, For Programmer's Console PWA P/N 89985400 and PWA P/N 89602069

PROGRAMMER'S CONSOLE (Sheet 2)

REGISTER SELECTORS

Function

The seven pushbutton switches (S1 through S7) allow the selection of one of the six internal registers or the Breakpoint (B) register. When a register has been selected, the corresponding front panel indicator lamp lights. The circuits are actuated on pressing the pushbutton.

Pushbutton Switches

PANEL DESIGNATION	CIRCUIT DESIGNATION	FUNCTION
M	S1	Selects register M
P	S2	Selects register P
Y	S3	Selects register Y
X	S4	Selects register X
A	S5	Selects register A
Q	S6	Selects register Q
B	S7	Selects register B

Inputs

SIGNAL	ACTIVE	FUNCTION	LOCATION SHEET	SQUARE
SEN	H	Active when computer stopped (from TTY Controller)	2	D-2
P4M	H	Clock from Memory Address	2	B-2
CLREG	H		3	A-4

PROGRAMMER'S CONSOLE (sheet 2, cont'd)

Output

SIGNAL	ACTIVE	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{CSM}$	L		2	B-1
$\overline{CSP}$	L		2	B-1
$\overline{CSY}$	L		2	B-1
$\overline{CSX}$	L	Register control signals	2	B-1
$\overline{CSA}$	L		2	C-1
$\overline{CSQ}$	L		2	C-1
CSB	H		2	D-1
$\overline{CLRB}$	L	Clears B Register	2	A-1
BCK	H	B Register clock	2	A-1
CSCK	H		2	B-1
$\overline{CLREG}$	L	Clears selected register	2	C-1
$\overline{PCL}$	L	Clears all CPU timing flip-flops when P Register is cleared	2	C-1

PROGRAMMER'S CONSOLE (sheet 2, cont'd)

Circuit Description

The switches are connected to the corresponding register control lines through input network and gating circuits. The input network also ensures that only one register at a time may be selected.

The input network consists of a set-reset flip-flop in each selector line; the set input of the flip-flop is taken from the switch through a pull-up resistor and delay capacitor, the reset input from the inverted output of an 8-input NAND gate whose inputs are also taken directly from the switches. When any one switch is pressed, its line is grounded and all the register select flip-flops are held reset, including the one selected. When the pushbutton switch is released, all flip-flops remain reset except the one selected; this is set by the signal (ground) conserved on the delay capacitor at its set input.

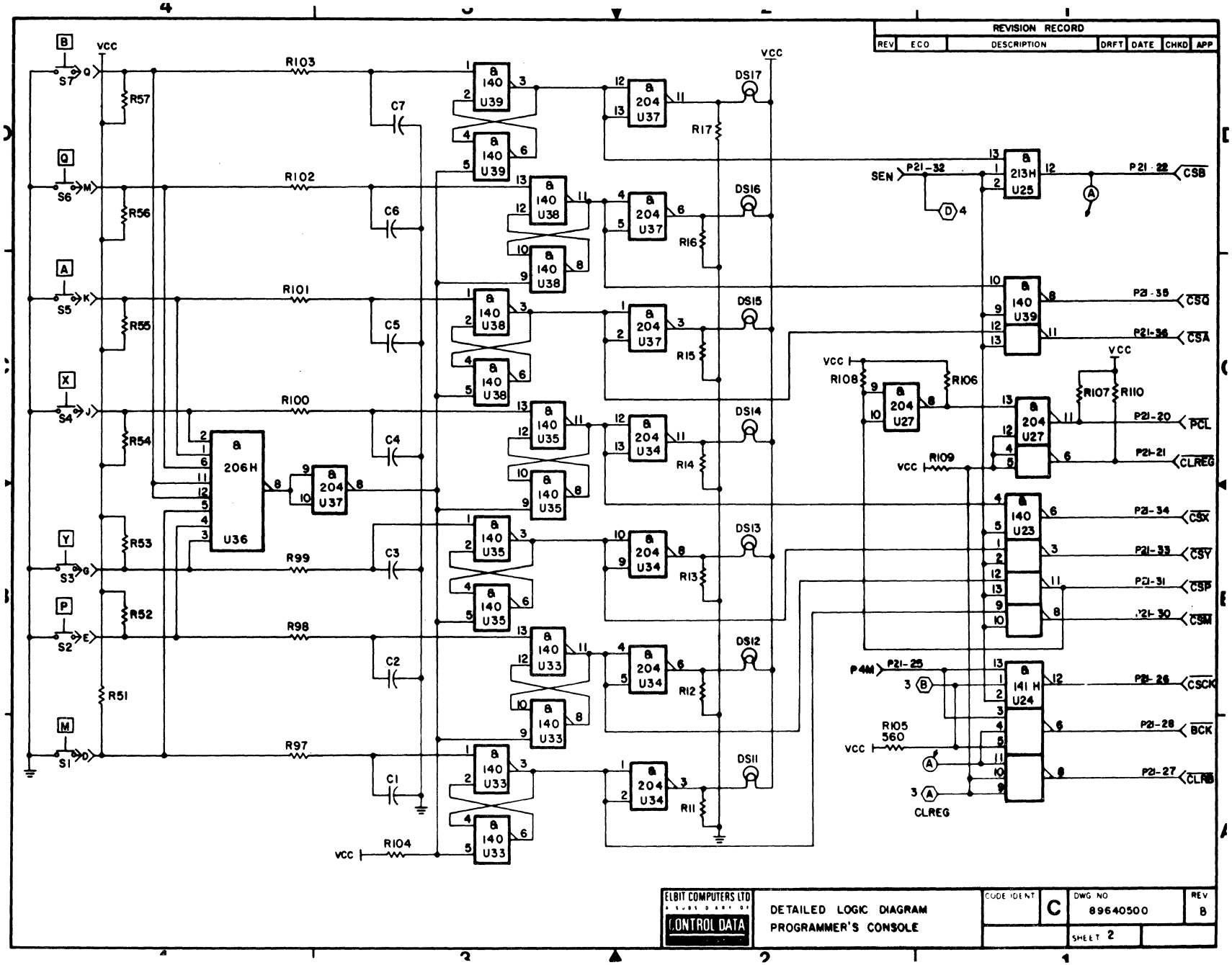
The indicator lamp drivers are actuated from the selector flip-flop output and cause the indicator to light when the flip-flop corresponding to it is set.

The register control signals are obtained by ANDing the output of the corresponding selector flip-flop with the signal SEN in AND and NAND gates. This prevents manual operation of the computer while it is running under program control.

PROGRAMMER'S CONSOLE (sheet 2, cont'd)

The other output signals are as follows:

Signal	Equation	Function/Remarks
$\overline{\text{CLRB}}$	CSB•CLREG	Clears the B register
$\overline{\text{CLREG}}$		Clears selected internal register
$\overline{\text{PCL}}$	CSP•CLREG	Resets all CPU timing flip-flops when P register is cleared
CSCK	SEN•P4M•C	Clocks data into one of the six internal registers. It is produced when any one of the data bit or clear pushbutton switches is pressed [condition C (U26,10)] and is active only when the computer is stopped (condition SEN). The frequency of the clock is that of P4M. P4M - clock signal from Memory Control; repetition rate approximately 0.44μsec for AB108, 0.65μsec for AB107.
BCK	P4M•CSB•C	Clocks the B register. It is produced when any one of the data bit or the clear pushbutton switches is pressed (condition C) and has the frequency of P4M.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
VCC
R103
R102
R101
R100
R99
R98
R97
R104
R57
R56
R55
R54
R53
R52
R51
C7
C6
C5
C4
C3
C2
C1
S7
S6
S5
S4
S3
S2
S1
B
Q
A
X
Y
P
M
U39
U38
U35
U33
U37
U34
206H U36
DSI7
DSI6
DSI5
DSI4
DSI3
DSI2
DSI1
R17
R16
R15
R14
R13
R12
R11
SEN
P21-32
213H U25
P21-22 CSB
P21-35 CSQ
P21-36 CSA
R108
R106
R107
R110
U27
P21-20 PCL
R109
P21-21 CLREG
U23
P21-34 CSX
P21-33 CSY
P21-31 CSP
P21-30 CSM
P4M
P21-25
141 H U24
P21-26 CSCK
R105 560
P21-28 BCK
P21-27 CLRB
CLREG
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
CODE IDENT C
DWG NO 89640500
REV B
SHEET 2

PROGRAMMER'S CONSOLE (sheet 3)

DATA BIT SELECTORS

Function

The circuit allows data input to each of 16 bits of the computer from the programmer's console when the computer is stopped. The indicators associated with each bit allow monitoring the contents of each bit location, both on manual operation and when the computer is running under program control. The clear pushbutton and its circuitry are included here.

Pushbutton Switches

PANEL DESIGNATION	CIRCUIT DESIGNATION	FUNCTION	ASSOCIATED SIGNAL
0	S23	Sets data bit in selected register; corresponding indicator lights	$\overline{\text{SET 00}}$
1	S22		$\overline{\text{SET 01}}$
2	S20		$\overline{\text{SET 02}}$
3	S21		$\overline{\text{SET 03}}$
4	S19		$\overline{\text{SET 04}}$
5	S18		$\overline{\text{SET 05}}$
6	S17		$\overline{\text{SET 06}}$
7	S16		$\overline{\text{SET 07}}$
8	S15		$\overline{\text{SET 08}}$
9	S14		$\overline{\text{SET 09}}$
10	S12		$\overline{\text{SET 10}}$
11	S13		$\overline{\text{SET 11}}$
12	S11		$\overline{\text{SET 12}}$
13	S10		$\overline{\text{SET 13}}$
14	S9		$\overline{\text{SET 14}}$
15	S8		$\overline{\text{SET 15}}$
CLEAR	S24	Clears selected registers (sheet 2)	$\overline{\text{CLREG}}$

PROGRAMMER'S CONSOLE

Input See switches and notes on output signals.

Outputs

SIGNAL	ACTIVE	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{\text{CNS 0L}}$ thru $\overline{\text{CNS 7L}}$	L	Main data path	3	A-2 to B-2
$\overline{\text{CNS 0M}}$ thru $\overline{\text{CNS 7M}}$	L	Main data path	3	C-2 to D-2

Notes: a. these signals are bidirectional when computer is operated from the front panel.

b. these signals are inputs when computer runs under program control.

Circuit Description

Each pushbutton switch is connected through a pull-up resistor and an inverter to an open collector NAND gate used as an inverter. The open collector outputs drive the CNS lines corresponding to the switch pressed.

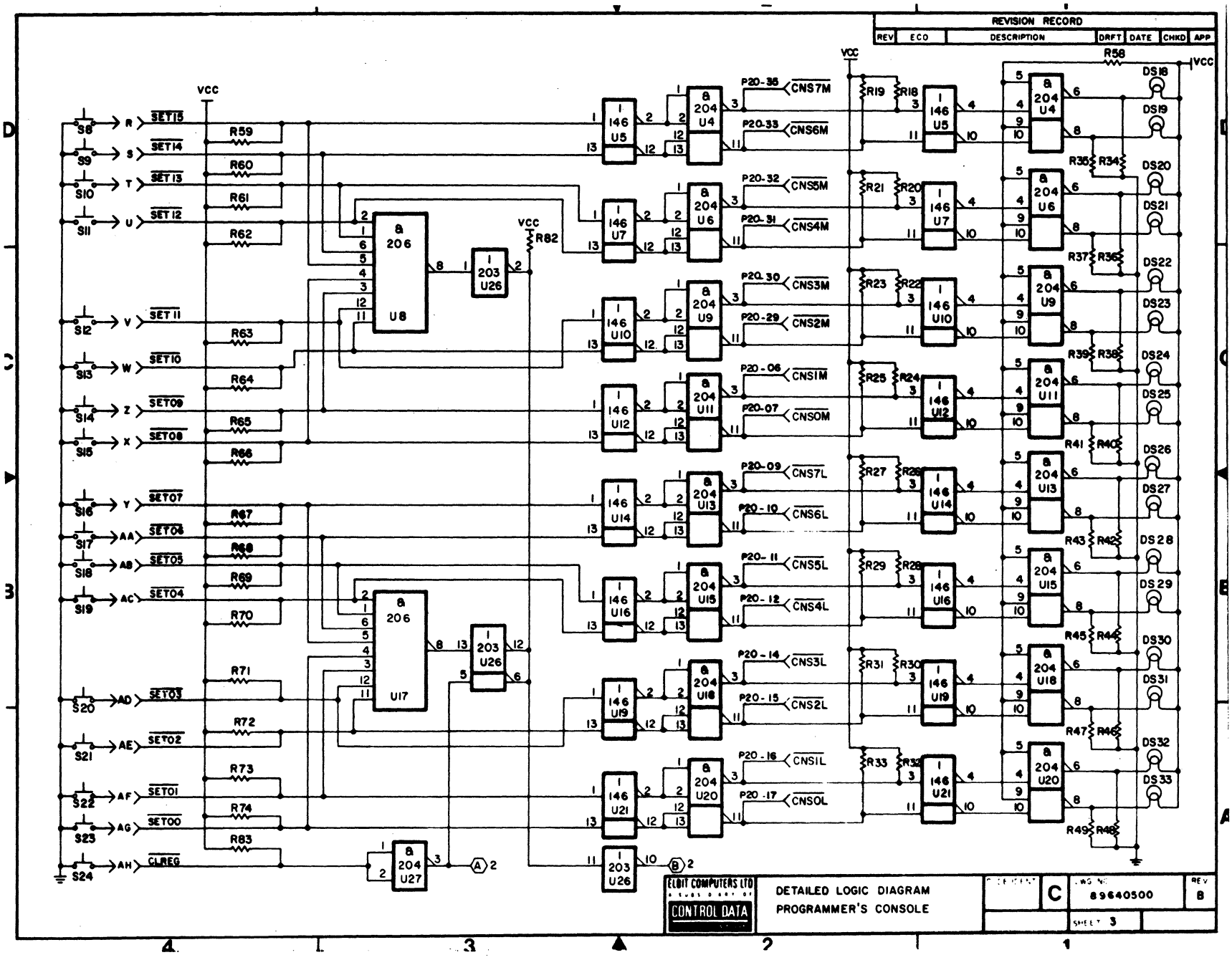
When the computer runs under program control the main data path signals appear at the pins carrying the CNS signals.

The indicator lights corresponding to the bit locations are lit according to the signal on the appropriate CNS line.

Two auxiliary signals are produced as follows (these are used on sheet 2):

Condition C: active high when any one of the pushbuttons in this circuit is pressed.

CLREG: Clear Register


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
VCC
S8 R SET15
S9 S SET14
S10 T SET13
S11 U SET12
S12 V SET11
S13 W SET10
S14 Z SET09
S15 X SET08
S16 Y SET07
S17 AA SET06
S18 AB SET05
S19 AC SET04
S20 AD SET03
S21 AE SET02
S22 AF SET01
S23 AG SET00
S24 AH CLREG
R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 R71 R72 R73 R74 R83 R82 R58
U8 U17 U26 U27
U4 U5 U6 U7 U9 U10 U11 U12 U13 U14 U15 U16 U18 U19 U20 U21
P20-35 CNS7M
P20-33 CNS6M
P20-32 CNS5M
P20-31 CNS4M
P20-30 CNS3M
P20-29 CNS2M
P20-06 CNS1M
P20-07 CNSOM
P20-09 CNS7L
P20-10 CNS6L
P20-11 CNS5L
P20-12 CNS4L
P20-14 CNS3L
P20-15 CNS2L
P20-16 CNS1L
P20-17 CNSOL
R19 R18 R21 R20 R23 R22 R25 R24 R27 R28 R29 R28 R31 R30 R33 R32
R35 R34 R37 R36 R39 R38 R41 R40 R43 R42 R45 R44 R47 R46 R49 R48
DS18 DS19 DS20 DS21 DS22 DS23 DS24 DS25 DS26 DS27 DS28 DS29 DS30 DS31 DS32 DS33
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
SIZE C
DWG NO 89640500
REV B
SHEET 3

PROGRAMMER'S CONSOLE

CONTROL SWITCHES AND INDICATORS

SWITCHES AND OUTPUT SIGNALS

PANEL DESIGNATION	CIRCUIT	SWITCH TYPE Pushbutton (P) Toggle (T)	SIGNAL OUTPUT
AUTOLOAD	S25	P	AUTOLOAD
MANUAL INTRPT.	S26	P	$\overline{\text{M.I.}}$
STOP	S27	P	$\overline{\text{STØP CS}}$
MASTER CLEAR	S28	P	$\overline{\text{MCCS}}$
GO	S29	P	$\overline{\text{GØCSW}}$
POWER	S30	T	PWR. SW
BREADPOINT STORE			
BREAKPOINT	S31	T	
PARITY FAULT STOP			
AUTORESTART	S32	T	$\overline{\text{AUTØRSW}}$
PROGRAM PROTECTS			PRTSW
TEST MODE	S33	T	$\overline{\text{TMSW}}$
32K			32KW
65K	S34	T	$\overline{\text{(32KW)}}$
ENTER			$\overline{\text{ENTER}}$
SWEEP	S35	T	$\overline{\text{SWEEP}}$
SELECTIVE SKIP	S36	T	$\overline{\text{SLK}}$
SELECTIVE STOP	S37	T	
INSTRUCTION			$\overline{\text{INSTEP}}$
CYCLE	S38	T	$\overline{\text{STØPCS}}$

NOTE:
The signal PRGST is transmitted to the console interface board. It is used to stop the computer under certain conditions.

1. When the cyclic parity error signals CCPE is active and the PE stop switch is set.
2. When the BEAC signal is active and the Breakpoint stop switch is set. BEAC is active when the contents of the Breakpoint register equals the CPU memory address.

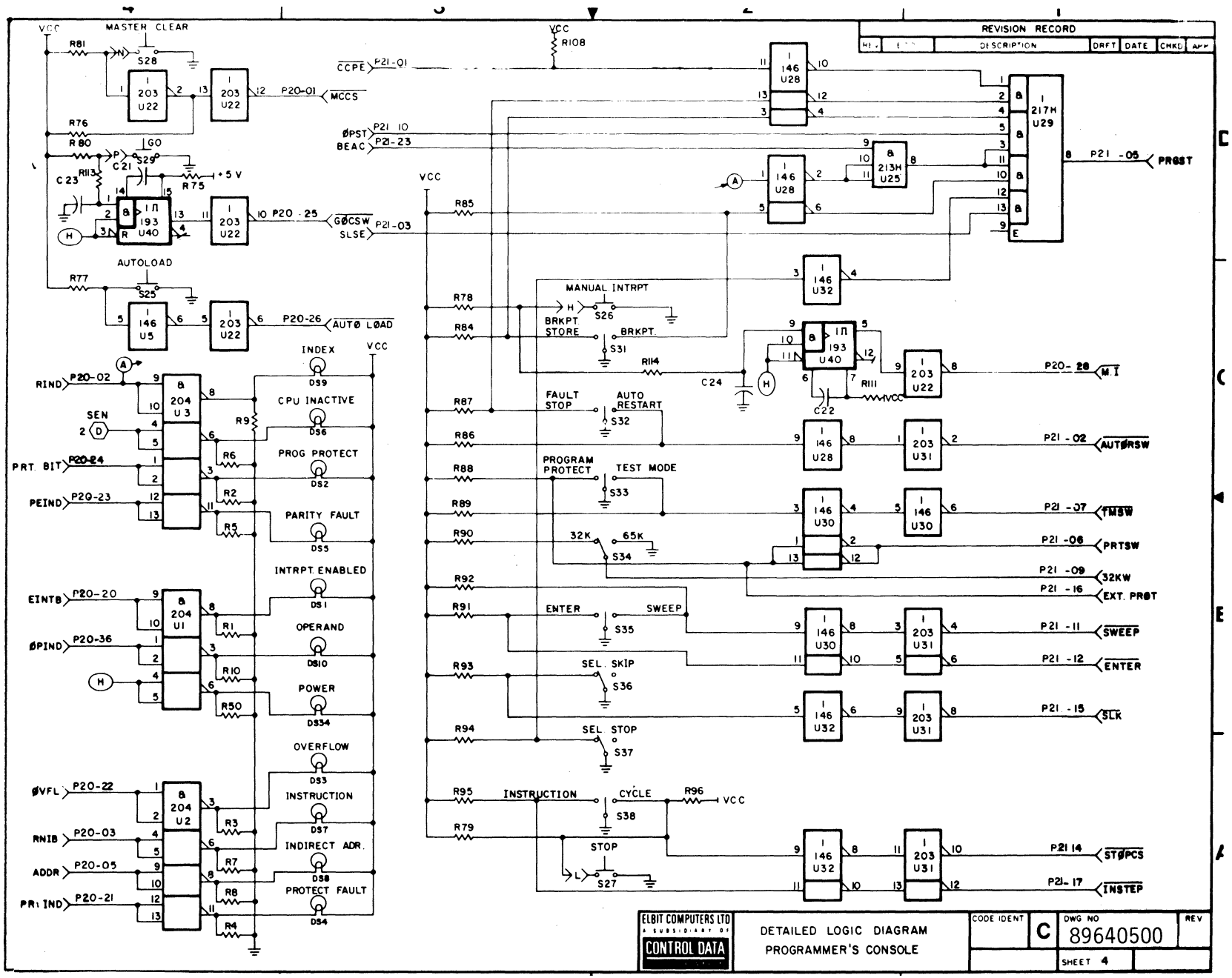
PROGRAMMER'S CONSOLE (Cont'd)

3. When the BEAC and ØPST signals are active and the Breakpoint store switch is set.
4. When the SLSE signal is active and the selective stop switch is set.

INDICATOR LIGHTS AND INPUT SIGNALS

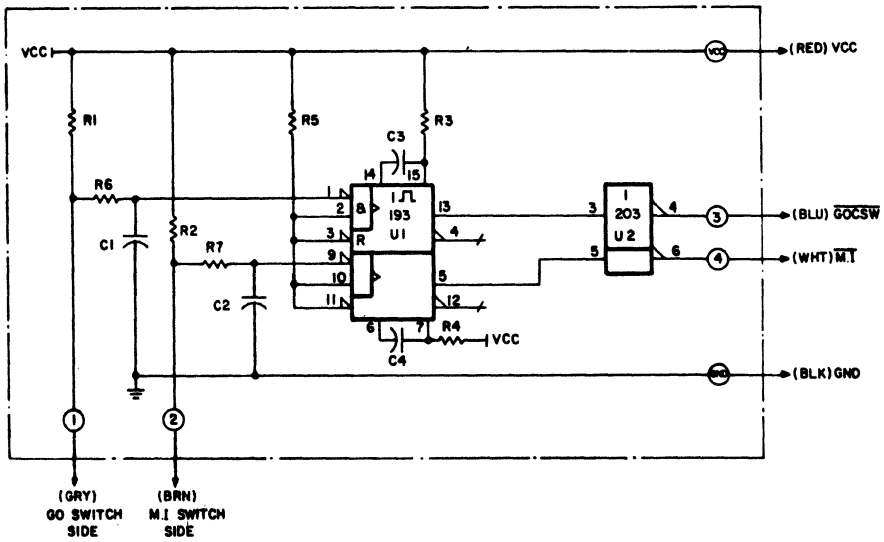
PANEL DESIGNATION	CIRCUIT	INPUT SIGNAL
INTERPT ENABLED	DS1	EINTB
PROG. PROTECT	DS2	PRT BIT
OVERFLOW	DS3	ØVFL
PROTECT FAULT	DS4	PRFIND
PARITY FAULT	DS5	PEIND
CPU INACTIVE	DS6	SEN
INSTRUCTION	DS7	RNIB
INDIRECT ADR.	DS8	ADDR
INDEX	DS9	RIND
OPERAND	DS10	ØPIND
POWER	DS34*	PWRIND
-	-	$\overline{\text{CCPE}}$
-	-	ØPST
-	-	BEAC
-	-	SLSE
-	-	PWRSW

* Indicates dc power switch on.



Logic Diagram 89640500, Sheet 4, For Programmer's Console PWA P/N 89985400 and PWA P/N 89602069

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	CK 1461	RELEASED TO CLASS A	S.D	DEC 75		



USED WITH PWA P/N 89987600

AND PWA P/N 89987700

AW 89982700	UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES	ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	FIRST USED ON ABIO7/8-A	TITLE DETAILED LOGIC DIAGRAM ANTI-BOUNCE CIRCUIT		
AY/PL 89982600	3 PLACE ± 2 PLACE ± ANGLES ±					
DETACHED LISTS	DO NOT SCALE DRAWING	DWN S.D DEC 75		CODE IDENT	C	DRAWING NO 89982800
	MATERIAL	CHKD				
	FINISH	ENGR		SCALE		SHEET 1 OF 1
		MFG DEC 75				
		APPR				

OFF - SHEET REFERENCE

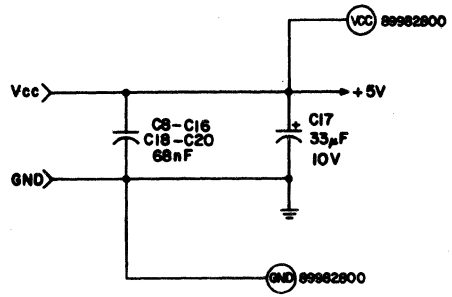
OFF SHEET REFERENCE LETTER	SHEET LOCATION 2	3	4
A	A-1	A-3	
B	B-1	A-2	
D	D-2		C-4

SHEET REVISION STATUS 1	2	3	4
A	A	A	A

REVISION RECORD REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	CK 1559	RELEASED CLASS A	mda	[illegible]	[illegible]	[illegible]

NOTES:

1. C1 – C7 ARE 1nF.
2. ALL RESISTORS ARE 0.25 WATT 5%.
3. R1 – R17, R34 ÷ R50 AND R97 ÷ R103 ARE 180 ØHMS
4. R18 – R33 ARE 330 ØHMS.
5. R51 – R96 ARE 1000 ØHMS.
6. R104 – R110 ARE 560 ØHMS.
7. LD 89982800 REFERENCED ON S.H.4 IS LOGIC DIAGRAM FOR ANTI – BOUNCE CIRCUIT SUB-ASSEMBLY
8. LOGIC FITS P/N 89640300 REWORKED TO P/N 89987600 BY FCO CK1431



FOR PWA P/N 89987600

AW 89640400

DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL

FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

FIRST USED ON AB107-A

DWN	IONA Z.	NOV.7.73
CHKD	HAIM IOSEF	NOV.7.73
ENGR	DAVID WEISS	DEC.9.73
MFG		
APPR		

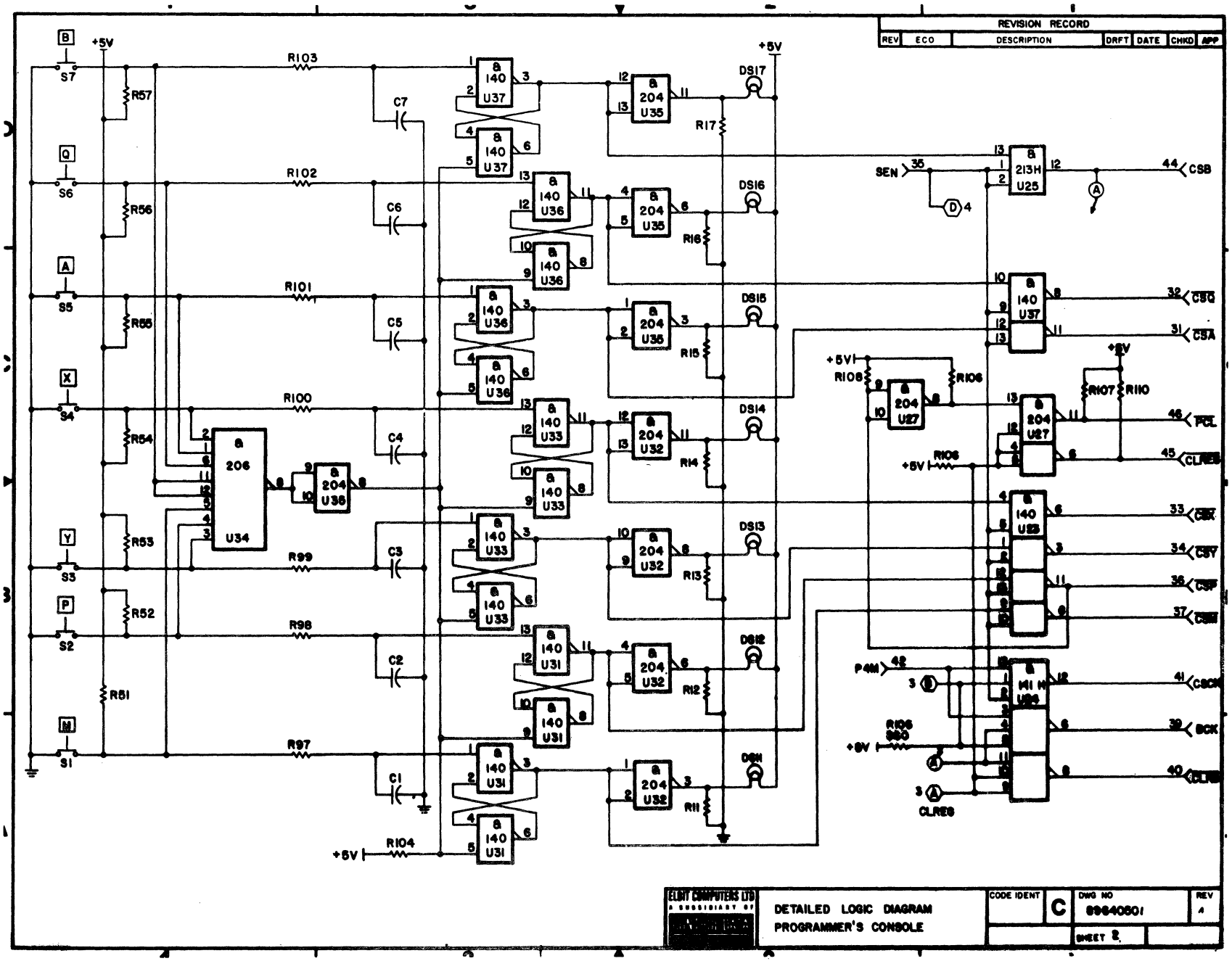
TITLE
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
FOR P/N 89987600

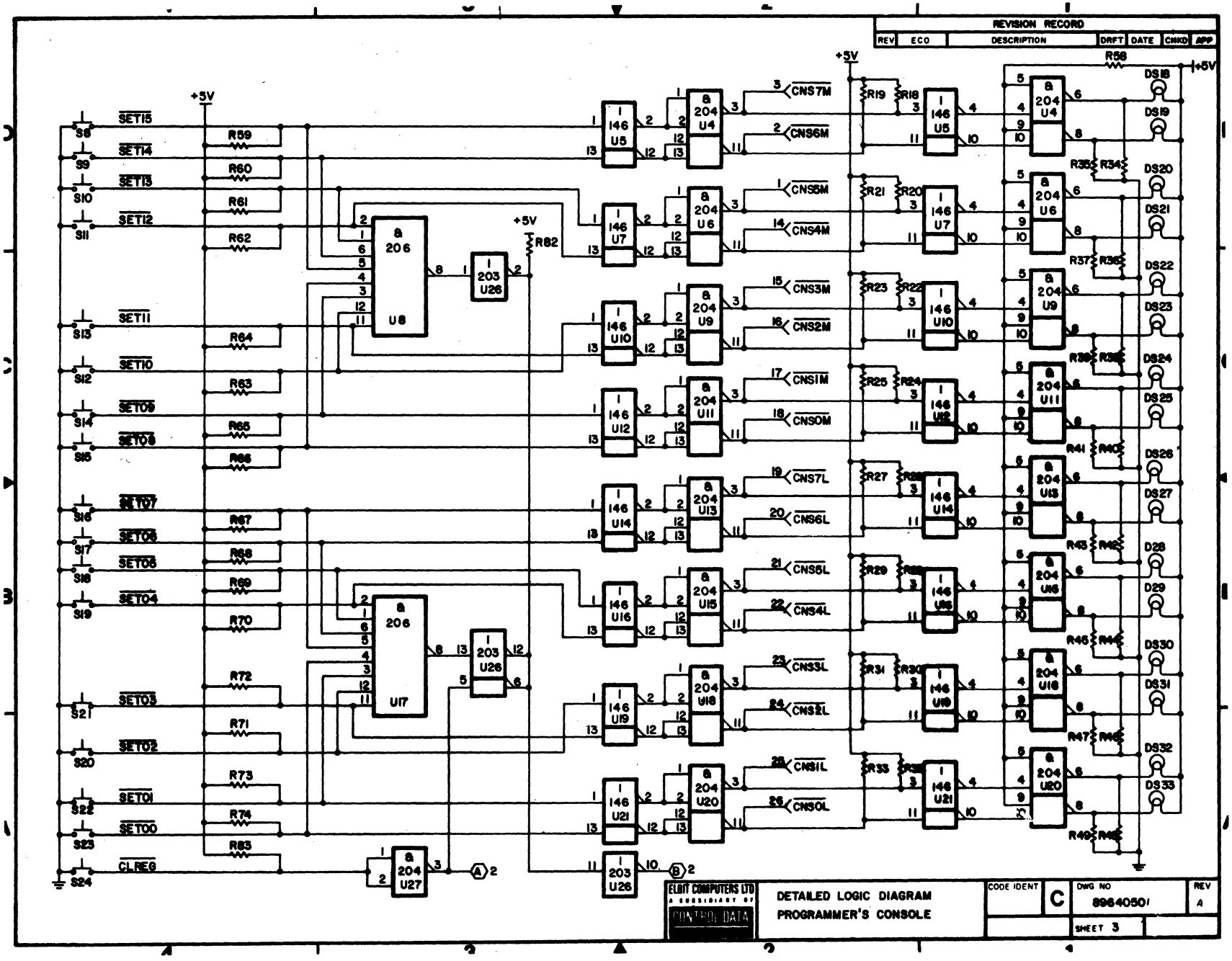
CODE IDENT C

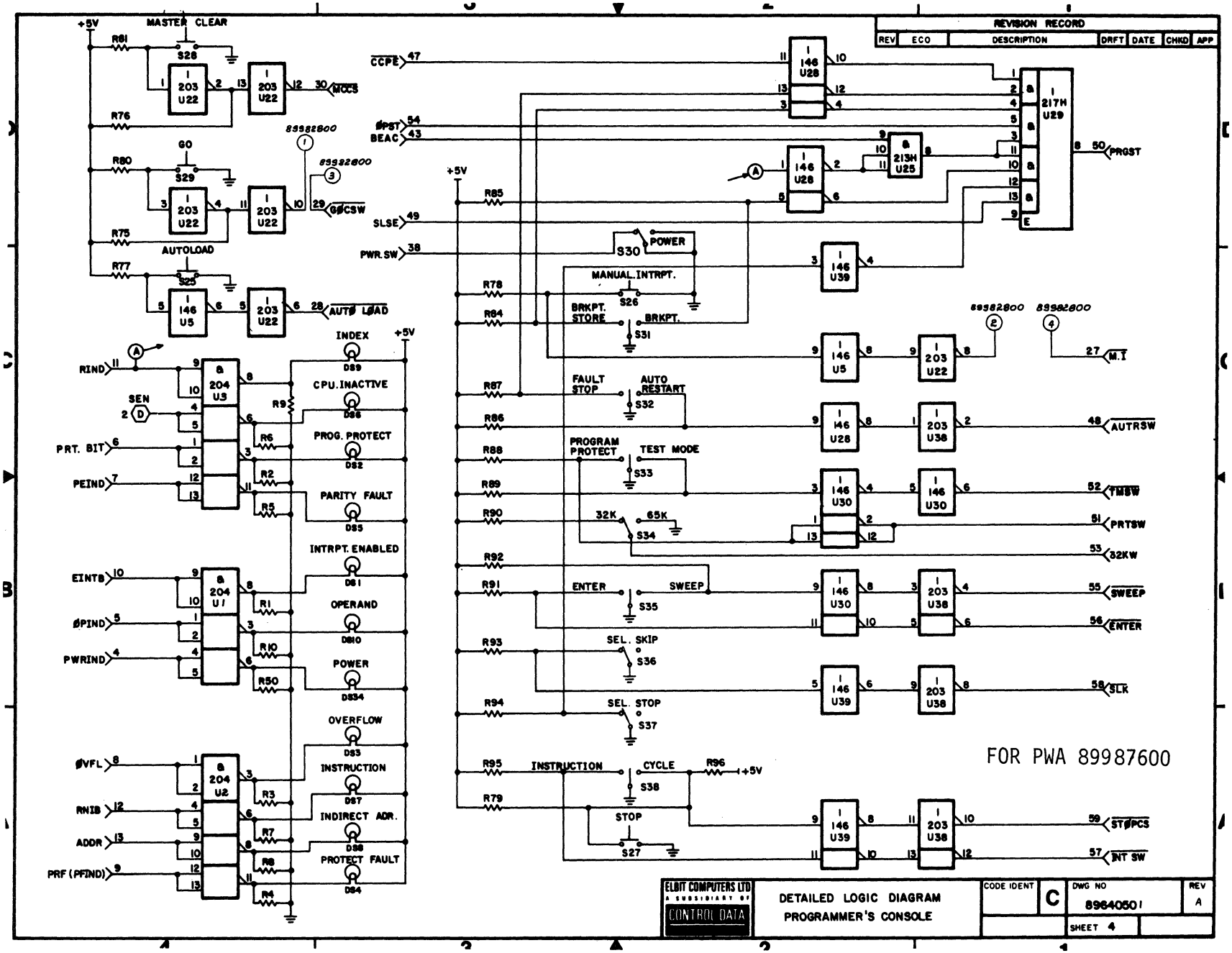
DRAWING NO 89640501

SCALE

SHEET 1 OF 4

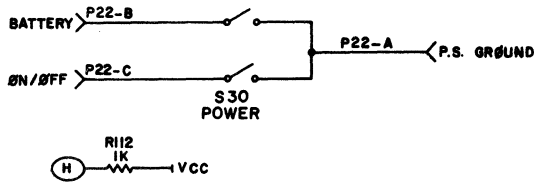

REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
B Q A X Y P M
S7 S6 S5 S4 S3 S2 S1
+5V
R103 R102 R101 R100 R99 R98 R97
R57 R56 R55 R54 R53 R52 R51
C7 C6 C5 C4 C3 C2 C1
R104
U37 U36 U33 U31
U35 U32
DS17 DS16 DS15 DS14 DS13 DS12 DS11
R17 R16 R15 R14 R13 R12 R11
U34 U36
SEN 35
D 4
U25
44 CSB
32 CSC
31 CSA
R108 R106 R107 R110
U27
46 PCL
45 CLRES
33 CSX
34 CSY
36 CSP
37 CSM
P4M 42
41 CSCK
39 SCK
40 CLRK
CLRES
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
CODE IDENT C
DWG NO 8964060/
REV A
SHEET 8

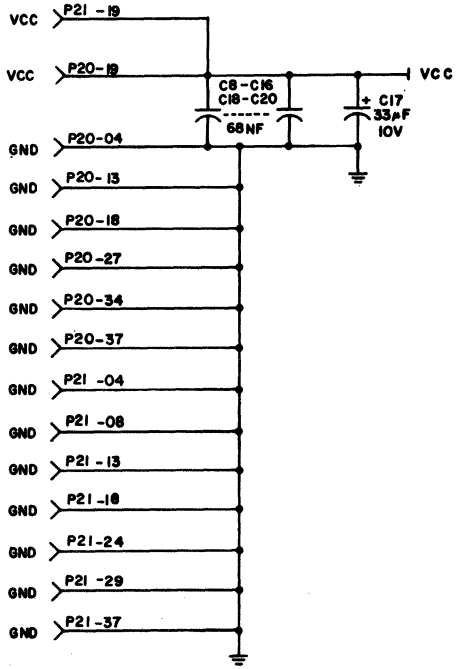

REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
+5V
SET15 SET14 SET13 SET12 SET11 SET10 SET09 SET08 SET07 SET06 SET05 SET04 SET03 SET02 SET01 SET00 CLREG
S8 S9 S10 S11 S13 S12 S14 S15 S16 S17 S18 S19 S21 S20 S22 S23 S24
R59 R60 R61 R62 R64 R63 R65 R66 R67 R68 R69 R70 R72 R71 R73 R74 R83 R82 R58
U8 U17 U27 U26 U5 U7 U10 U12 U14 U16 U19 U21 U4 U6 U9 U11 U13 U15 U18 U20
CNS7M CNS6M CNS5M CNS4M CNS3M CNS2M CNS1M CNS0M CNS7L CNS6L CNS5L CNS4L CNS3L CNS2L CNS1L CNS0L
DS18 DS19 DS20 DS21 DS22 DS23 DS24 DS25 DS26 DS27 D28 D29 DS30 DS31 DS32 DS33
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
CODE IDENT C
DWG NO 8964050/
REV A
SHEET 3


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
+5V
MASTER CLEAR
S28
GO
S29
AUTOLOAD
S25
R81
R76
R80
R75
R77
R78
R84
R85
R87
R86
R88
R89
R90
R92
R91
R93
R94
R95
R79
R9
R6
R2
R5
R1
R10
R50
R3
R7
R8
R4
R96
U22
U5
U1
U2
U3
U25
U26
U28
U29
U30
U38
U39
U146
U203
U204
U213H
U217H
MCCS
GØCSW
AUTØ LOAD
CCPE
ØPST
BEAC
SLSE
PWR.SW
PRGST
POWER
S30
MANUAL.INTRPT.
S26
BRKPT. STORE
BRKPT.
S31
FAULT STOP
AUTO RESTART
S32
PROGRAM PROTECT
TEST MODE
S33
32K
65K
S34
ENTER
SWEEP
S35
SEL. SKIP
S36
SEL. STOP
S37
INSTRUCTION
CYCLE
S38
STOP
S27
M.I
AUTRSW
TMSW
PRTSW
32KW
SWEEP
ENTER
SLK
STØPCS
INT SW
INDEX
CPU.INACTIVE
PROG. PROTECT
PARITY FAULT
INTRPT. ENABLED
OPERAND
POWER
OVERFLOW
INSTRUCTION
INDIRECT ADR.
PROTECT FAULT
DS9
DS8
DS2
DS5
DS1
DS10
DS34
DS3
DS7
DS6
DS4
RIND
SEN
PRT. BIT
PEIND
EINTB
ØPIND
PWRIND
ØVFL
RNIB
ADDR
PRF (PFIND)
FOR PWA 89987600
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
CODE IDENT
C
DWG NO
8964050 I
REV
A
SHEET 4

ØFF – SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4
A	A-1	A-3	
B	B-1	A-2	
D	D-2		C-4





SHEET REVISION STATUS 1	2	3	4
A	A	A	A

REVISION RECORD REV	ECO	DESCRIPTN	DRFT	DATE	CHKD	APP
A	CK 1559	RELEASED TO CLASS A	H.P	19.2.75		

NØTES:

1. C1 – C7 ARE 1nF.
2. ALL RESISTØRS ARE 0.25 WATT 5%.
3. R1 – R17, R34 ÷ R50 AND R97 ÷ R103 ARE 180 ØHMS.
4. R18 – R33 ARE 330 ØHMS.
5. R51 – R74, R76 - 96 AND R112 ARE 1K ØHMS
6. R104 – R110 ARE 560 ØHMS.
7. R75 AND R111 ARE 33K ØHMS.

FOR PWA P/N 89987700

AW 89881900 DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

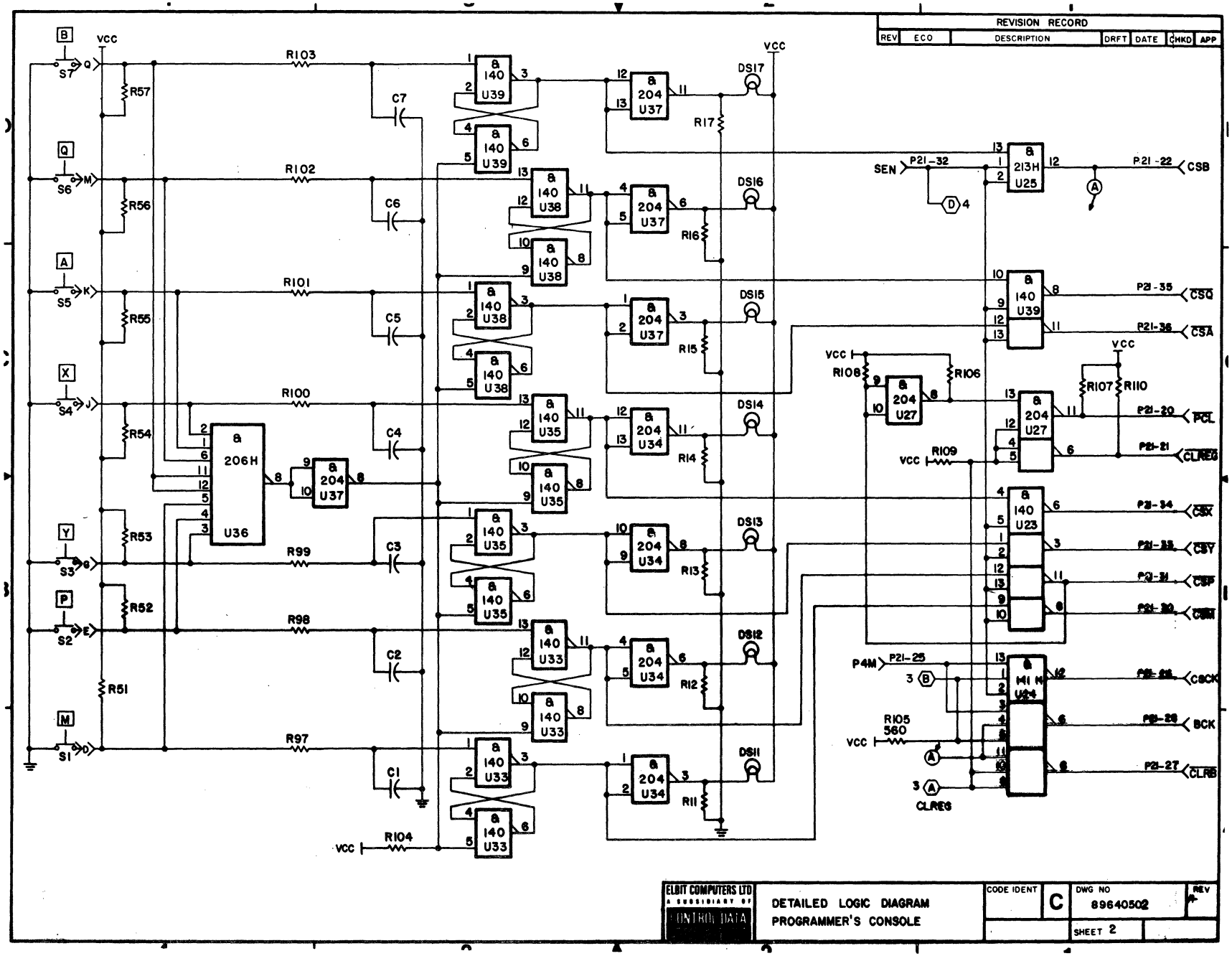
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

FIRST USED ON AB107-A/B

DWN	[illegible]	Jan. 75
CHKD		
ENGR	NISGAV S.	JAN. 75
MFG	[illegible]	
APPR	[illegible]	

TITLE
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
FOR P/N 89987700

CODE IDENT C
DRAWING NO 89640502
SCALE
SHEET 1 OF 4


REVISION RECORD
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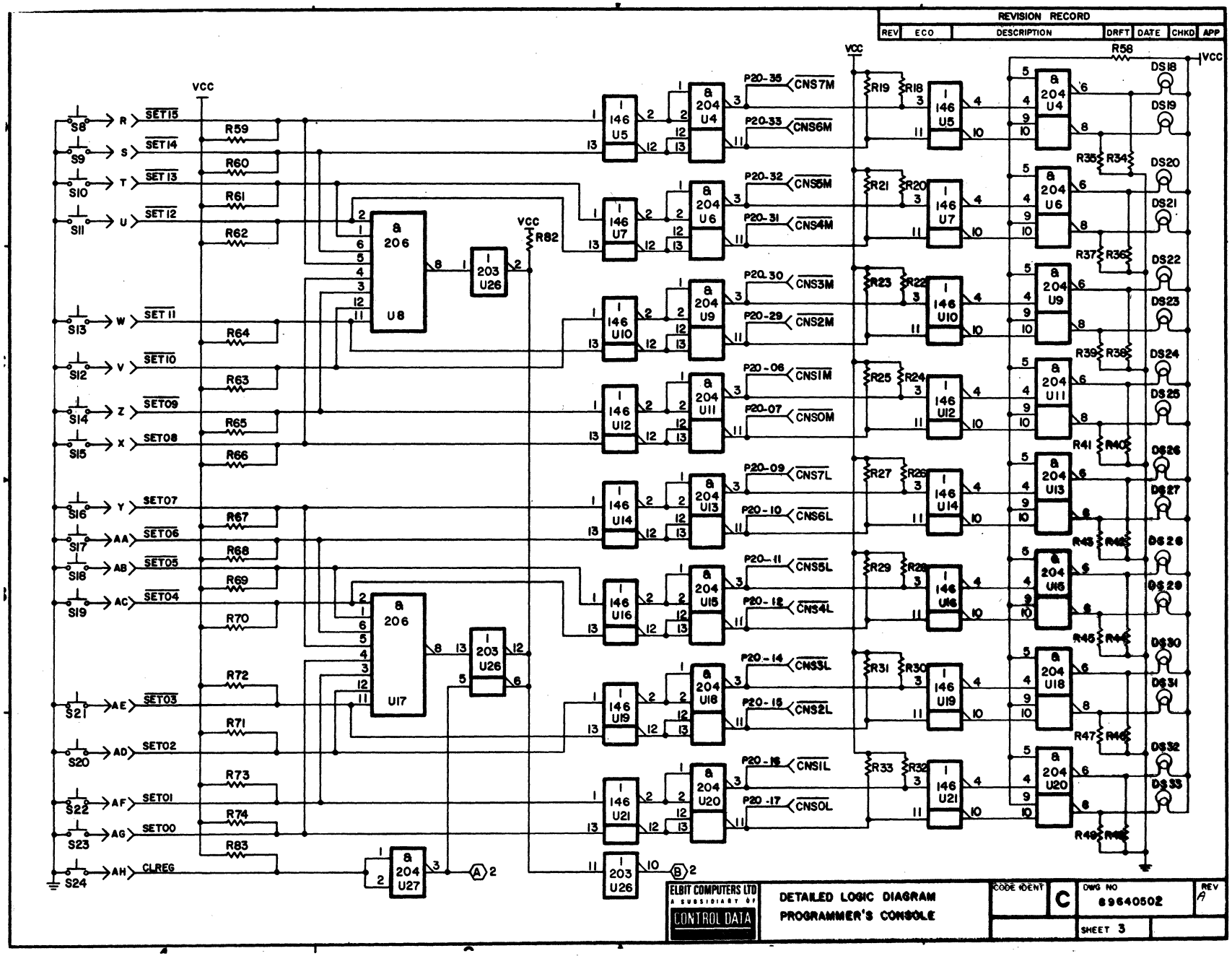
VCC
R103
R102
R101
R100
R99
R98
R97
R104
R57
R56
R55
R54
R53
R52
R51
C7
C6
C5
C4
C3
C2
C1
S7
S6
S5
S4
S3
S2
S1
U39
U38
U35
U33
U37
U34
U36
206H
DSI7
DSI6
DSI5
DSI4
DSI3
DSI2
DSI1
R17
R16
R15
R14
R13
R12
R11
SEN
P21-32
D4
U25
213H
P21-22
CSB
P21-35
CSQ
P21-36
CSA
R108
R106
R107
R110
R109
U27
P21-20
PCL
P21-21
CLREG
U23
P21-34
CSX
P21-33
CSY
P21-31
CSF
P21-30
CSM
P4M
P21-25
R105
560
U24
P21-26
CSCK
P21-28
BCK
P21-27
CLRS
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
CODE IDENT
C
DWG NO
89640502
REV
SHEET 2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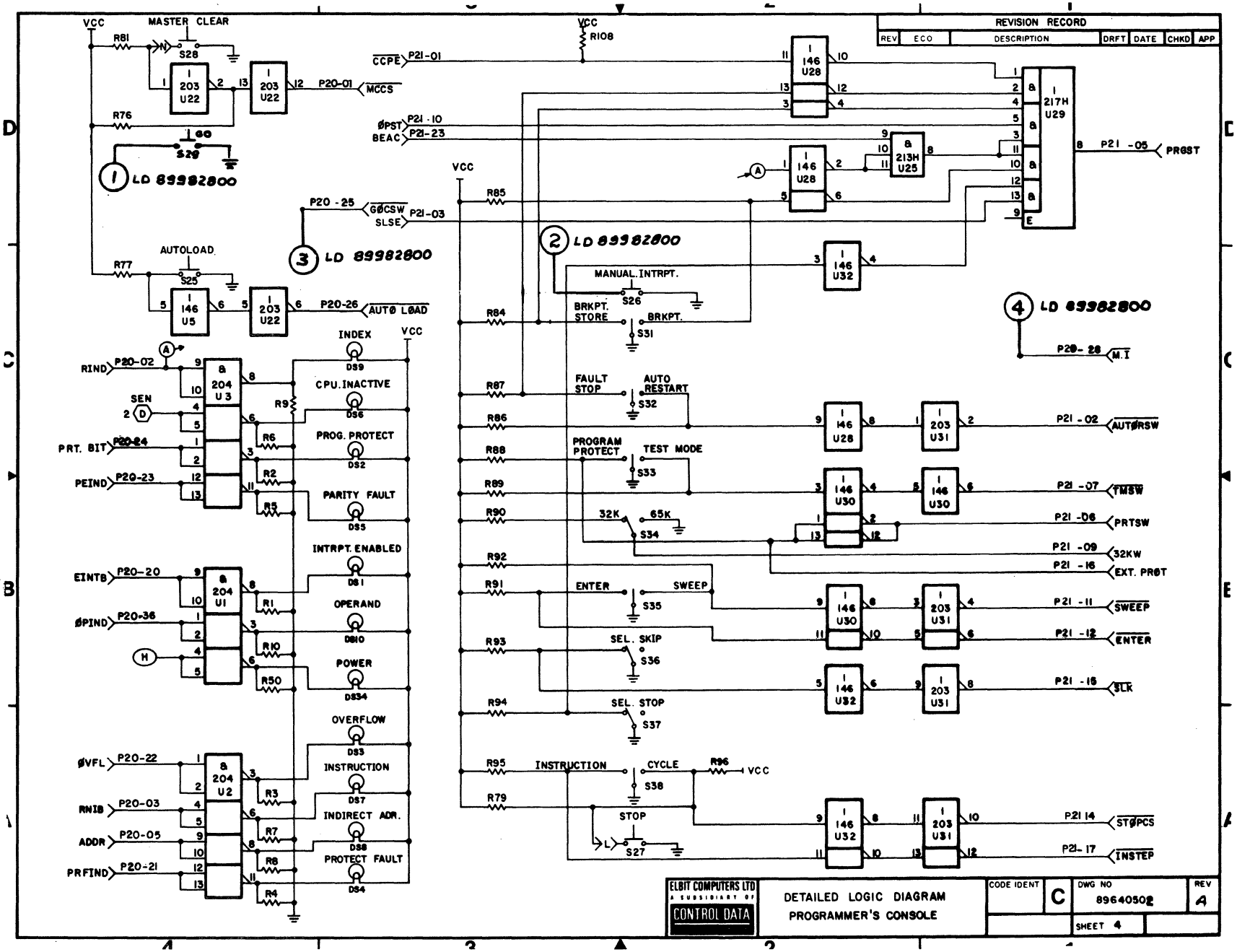
VCC
R58
S8 R SET15
S9 S SET14
S10 T SET13
S11 U SET12
S13 W SET11
S12 V SET10
S14 Z SET09
S15 X SET08
S16 Y SET07
S17 AA SET06
S18 AB SET05
S19 AC SET04
S21 AE SET03
S20 AD SET02
S22 AF SET01
S23 AG SET00
S24 AH CLREG
R59 R60 R61 R62 R64 R63 R65 R66 R67 R68 R69 R70 R72 R71 R73 R74 R83
R82
U8 U17 U26 U27
U4 U5 U6 U7 U9 U10 U11 U12 U13 U14 U15 U16 U18 U19 U20 U21
P20-35 CNS7M
P20-33 CNS6M
P20-32 CNS5M
P20-31 CNS4M
P20-30 CNS3M
P20-29 CNS2M
P20-06 CNS1M
P20-07 CNS0M
P20-09 CNS7L
P20-10 CNS6L
P20-11 CNS5L
P20-12 CNS4L
P20-14 CNS3L
P20-15 CNS2L
P20-16 CNS1L
P20-17 CNS0L
R19 R18 R21 R20 R23 R22 R25 R24 R27 R26 R29 R28 R31 R30 R33 R32
R35 R34 R37 R36 R39 R38 R41 R40 R43 R42 R45 R44 R47 R46 R49 R48
DS18 DS19 DS20 DS21 DS22 DS23 DS24 DS25 DS26 DS27 DS28 DS29 DS30 DS31 DS32 DS33
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
CODE IDENT C
DWG NO 89640502
REV A
SHEET 3


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
VCC
MASTER CLEAR
R81
S28
R76
S29
AUTOLOAD
R77
S25
R85
R84
R87
R86
R88
R89
R90
R92
R91
R93
R94
R95
R79
R96
R10
CCPE P21-01
ØPST P21-10
BEAC P21-23
P20-25 GØCSW
SLSE P21-03
P20-26 AUTØ LØAD
MANUAL. INTRPT.
S26
BRKPT. STORE
BRKPT.
S31
FAULT STOP
AUTO RESTART
S32
PROGRAM PROTECT
TEST MODE
S33
32K
65K
S34
ENTER
SWEEP
S35
SEL. SKIP
S36
SEL. STOP
S37
INSTRUCTION
CYCLE
S38
STOP
S27
P21-05 PRØST
P20-28 M.I
P21-02 AUTØRSW
P21-07 TMSW
P21-06 PRTSW
P21-09 32KW
P21-16 EXT. PRØT
P21-11 SWEEP
P21-12 ENTER
P21-15 SLK
P21 14 STØPCS
P21-17 INSTEP
INDEX DS9
CPU. INACTIVE DS6
PROG. PROTECT DS2
PARITY FAULT DS5
INTRPT. ENABLED DS1
OPERAND DS10
POWER DS34
OVERFLOW DS3
INSTRUCTION DS7
INDIRECT ADR. DS8
PROTECT FAULT DS4
RIND P20-02
SEN
PRT. BIT P20-24
PEIND P20-23
EINTB P20-20
ØPIND P20-36
ØVFL P20-22
RNIB P20-03
ADDR P20-05
PRFIND P20-21
LD 89982800
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
PROGRAMMER'S CONSOLE
CODE IDENT C
DWG NO 89640502
REV A
SHEET 4

ARITHMETIC AND LOGIC UNIT (ALU) (drawing 89614300)

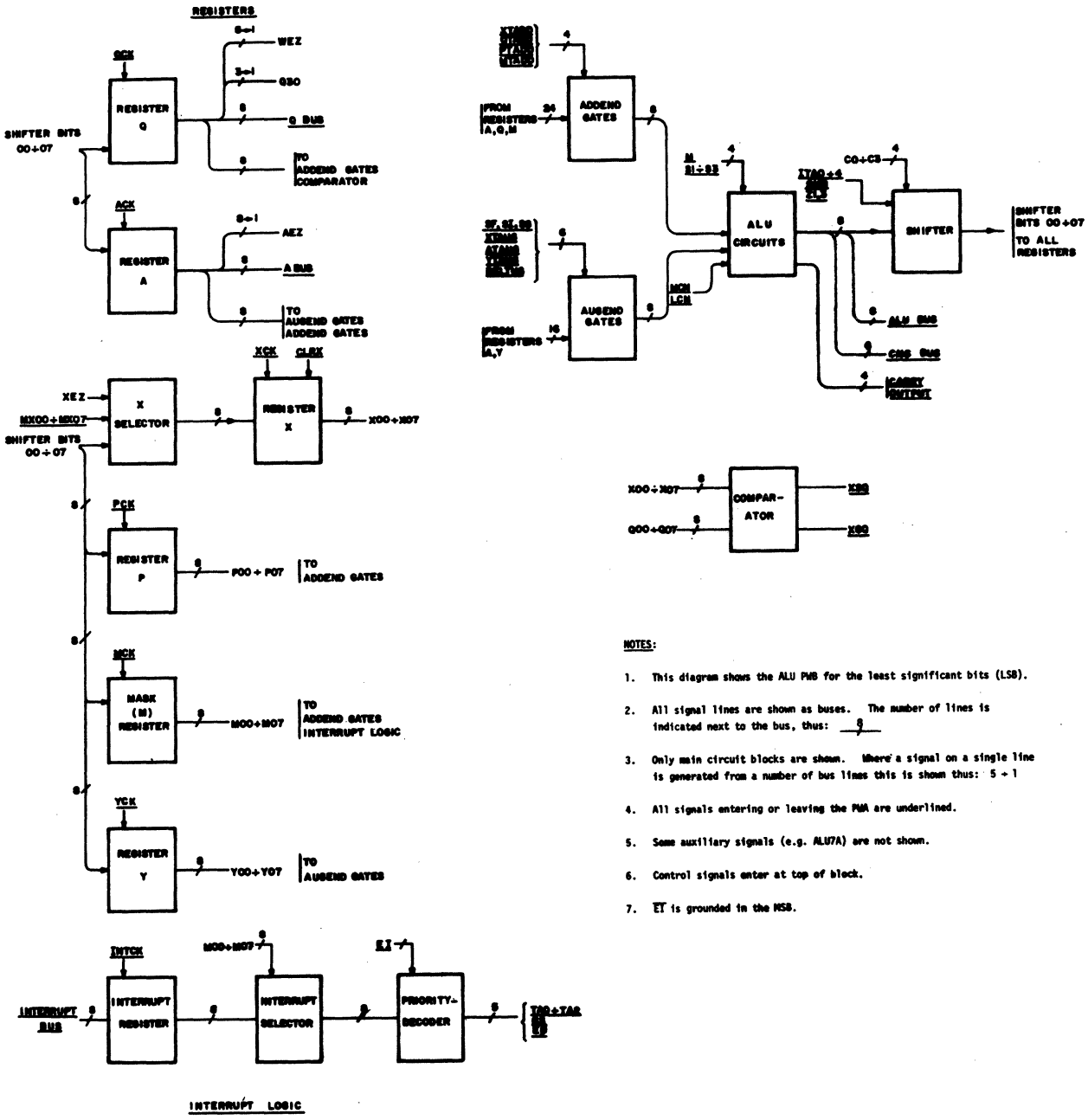
The ALU circuits are accommodated on two identical 50-PAK printed wiring boards. The logic circuit diagram for the board is given in drawing number 89614300 (sheets 1-10).

Two ALU assemblies are used to accommodate the 16 bits of the computer word (without parity or protect bits), the circuitry of one board being sufficient for eight bits only. One board, designated LSB, operates on the least significant bits (bits 00 through 07), the other board (MSB) operates on the most significant bits (bits 08 through 15). Circuitry common to both boards is accommodated on the Console Interface board, timing signals are generated on the Timing board.

This page lists the principal blocks making up one ALU board and gives the input and output signals. Both the circuits and the signals are described in detail on pages facing the corresponding sheet of the circuit diagram.

MAIN FUNCTIONAL BLOCKS

Designation/Description	Shown on sheet
Addend Registers and Gates	2,3
Augend Registers and Gates	4,5
Arithmetic and Logic Operations	6,7
Shifter	6,7
Interrupt logic	8



NOTES:

1. This diagram shows the ALU PWB for the least significant bits (LSB).
2. All signal lines are shown as buses. The number of lines is indicated next to the bus, thus: ___/ 8
3. Only main circuit blocks are shown. Where a signal on a single line is generated from a number of bus lines this is shown thus: 5 ÷ 1
4. All signals entering or leaving the PWA are underlined.
5. Some auxiliary signals (e.g. ALU7A) are not shown.
6. Control signals enter at top of block.
7. $\overline{EI}$ is grounded in the MSB.

INTERRUPT LOGIC

ALU SIMPLIFIED BLOCK DIAGRAM

ALU (drawing 89614300)

Inputs

Signal	Active	Signal Source/ Connector Pin	Function	Location Sheet	Square
MCK	H	P2A13	M register clock	2	D4
QCK	H	P1A14	Q register clock	2	C4
PCK	H	P1B13	P register clock	2	B4
$\overline{\text{CLRQ}}$	H	P1A13	Clear Q register	2	C4
PTADD	H	P1A12	Controls for transferring addend register content to ALU	2	D2
QTADD	H	P2A26		2	D2
XTADD	H	P1A09		2	D2
MTADD	H	P1B14		2	C2
32KW	H	P2A29	Memory mode selector	3	D4
$\overline{\text{ØVFW}}$	L	P2B27		3	D4
XEZ	H	P1A18	X register content zero	4	D4
MX03	H	P1A16	Data from Memory Control	4	D4
MX02	H	P1B15		4	D4
MX01	H	P1A19		4	D4
MX00	H	P1B18		4	C4
YCK	H	P1A20	Y register clock	4	C4
ACK	H	P1B19	A register clock	4	B4
XCK	H	P1A15	X register clock	4	D3
$\overline{\text{CLRX}}$	H	P1B20	Clear X register	4	D3
XTAUG	H	P2A25	Controls for transferring augend register content to ALU	4	D2
ATAUG	H	P2A21		5	D2
YTAUG	H	P1B17		5	D2
$\overline{\text{DELTAUG}}$	H	P2B16		5	C2
SF	H	P1B22	Augend gate controls	4	B2
SG	H	P1A22		5	D2
SI	H	P1A17		5	D2
MX07	H	P2B19	Date from Memory Control	5	D4
MX06	H	P2A18		5	D4
MX05	H	P2B20		5	D4
MX04	H	P2A20		5	D4

ALU (drawing 89614300)

Inputs (cont'd.)

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
MC	H	P2B30	Master Clear	5	C4
$\overline{AQC}$	L	P2A30	A/Q channel control signal	5	A4
ZO1	H	P2A09		7	A4
ZO3	H	P2A04		6	A4
ZO5	H	P2A06		6	B4
MCN	H	P1A07	Carry signals	7	B4
LCN	H	P1B26		6	B4
SHB	H	P2B05		6	A4
$\overline{ITA00}$	L	P2B06	Trap address bits	6	A4
$\overline{ITA02}$	L	P1A25		6	C2
$\overline{ITA03}$	L	P1A24		6	D2
$\overline{ITA04}$	L	P2B10		7	D4
$\overline{ITA05}$	L	P2A12		7	C4
CO0	H	P1B23	Selector lines	7	A4
CO1	H	P2A10		7	D4
CO2	H	P1A01		7	D4
CO3	H	P2B31		7	D4
M	H	P2B07	ALU mode control input	7	C4
SO3	H	P1B25	ALU function select inputs	7	C4
SO2	H	P1A26		7	C4
SO1	H	P2B09		7	B4
SO0	H	P2A08		7	B4
AUG07	H	P2B08		7	
ADD07	H	P2A14		7	B4
$\overline{CLREG}$	L	P1A28	Clear Register	7	A4
SH0	H	P2B11		7	A4
INTCK	H	P1B03	Interrupt clock	8	D4

ALU (drawing 89614300)

Inputs (cont'd.)

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
$\overline{INT00}$	L	P1A10	Interrupt Lines	8	B4
$\overline{INT01}$	L	P1B10		8	B4
$\overline{INT02}$	L	P1A07		8	B4
$\overline{INT03}$	L	P1B07		8	B4
$\overline{INT04}$	L	P1A05		8	C4
$\overline{INT05}$	L	P1A06		8	C4
$\overline{INT06}$	L	P1B06		8	C4
$\overline{INT07}$	L	P1B05		8	C4
$\overline{EI}$	L	P1A03		8	B3
+5V		P2A31	V_{cc}	8	B2
GND		P1B11	Logic Ground	8	A2
GND		P1A29		8	A2
GND		P2A03		8	A2
GND		P2B21		8	A2

ALU (drawing 89614300)

Outputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
Q30	H	P1B08	$\overline{Q00} \cdot \overline{Q01} \cdot \overline{Q02}$	2	C2
Q00	H	P1B12	Q register bits	2	B2
Q01	H	P1A11		2	B2
Q02	H	P1A08		2	B2
Q03	H	P1B09		2	B2
Q04	H	P2A24		3	B2
Q05	H	P2B28		3	B2
Q06	H	P2B25		3	B2
Q07	H	P2A28		3	B2
$\overline{WEZ}$	L	P2B29	Q03+Q04+Q05+Q06+Q07	3	C2
XGQ	H	P2A17	{X} > {Q}	3	D2
XSQ	H	P2B18	{X} < {Q}	3	D2
ØA00	H	P2A05	Gated A register outputs	4	B2
ØA01	H	P1B02		4	B2
ØA02	H	P1A30		4	B2
ØA03	H	P2B04		4	A2
ØA04	H	P2A23		5	B2
ØA05	H	P2B24		5	B2
ØA06	H	P2A22		5	B2
ØA07	H	P2B22		5	B2

ALU (drawing 89614300)

Outputs (cont'd.)

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
$\overline{A00}$	L	P2A27	Least significant bit of A register	5	A3
AUG07	H	P2B08		5	D1
AEZ	H	P1B16	$\overline{A00} \cdot \overline{A01} \cdot \overline{A02} \cdot \overline{A03} \cdot \overline{A04} \cdot \overline{A05} \cdot \overline{A06} \cdot \overline{A07}$	4	A3
XSEL07	H	P2A19	X selector output bit 7	5	D2
SHA	H	P2B26		6	C3
A07	H	P2B23		6	C3
Q7A	H	P2B01		6	A4
$\overline{CNS00}$	L	P1B31		6	B2
$\overline{CNS01}$	L	P1A31		6	B2
$\overline{CNS02}$	L	P1B29		6	B2
$\overline{CNS03}$	L	P1B28	CNS data bus bits	6	C2
$\overline{CNS04}$	L	P2B12		7	C2
$\overline{CNS05}$	L	P2A11		7	C2
$\overline{CNS06}$	L	P2B13		7	A2
$\overline{CNS07}$	L	P2B14		7	A2
GM	H	P2B03		7	B3
PM	H	P2A01	Carry generate and propagate	7	B3
GL	H	P1B21		6	B2
PL	H	P1A23		6	B2

ALU (drawing 89614300)

Outputs (cont'd.)

Signal	Active	Connector/ Pin	Function	Location Sheet	Location Square
$\overline{TA02}$	L	P1B04		8	C1
$\overline{TA01}$	L	P1A04		8	B1
$\overline{TA00}$	L	P1B02		8	B1
$\overline{GS}$	L	P1A02		8	B1
$\overline{E\emptyset}$	L	P1B01		8	B1
ALU00	H	P1B24	ALU signals to bus	7	
ALU01	H	P1B30		7	
ALU02	H	P1B27		7	
ALU03	H	P1A21		7	
ALU04	H	P2B17		7	D4
ALU05	H	P2A16		7	C4
ALU06	H	P2A15		7	C4
ALU07	H	P2B15		7	A4
ALU07A	H	P2B02		7	A4
ALU0A	H	P1A27			

ØFF – SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SHEET LOCATION						
	2	3	4	5	6	7	8
A	D-1				B-3		
B	C-1				B-3		
C	B-1				B-3		
D	A-1				B-3		
E	D-2	D-2					
F	D-2	D-1			D-4		
G	D-2	D-2					
K	D-2	D-2					
L	A-1		C-2				
M	B-1		B-2				
N	C-1		D-2				
P	D-1		D-2				
R	B-2						B-3
S	C-3						B-3
T	D-3						B-3
U	D-4	A-4					
V	B-3	C-3					
W	D-3		C-3				
X	D-3		C-3				
Y	D-3		D-3				
Z	D-3		D-3				
Q	A-3						B-3
AA	D-2	D-3					
AB	D-2	D-3					
AC	D-2	D-3					
AD	C-4	B-4			B-4		
AE	B-4	C-4					
AF	D-4	C-4	C-4	A-4	B-4		D-4
AG	B-4		B-4	A-4	A-1		
AK	A-4		B-4		C-1		
AL	A-4		B-4		D-1		
AM	A-4		B-4		B-1		
AN	C-4	B-4					
AP		D-1				B-4	
AQ		C-1				B-4	

SHEET REVISION STATUS

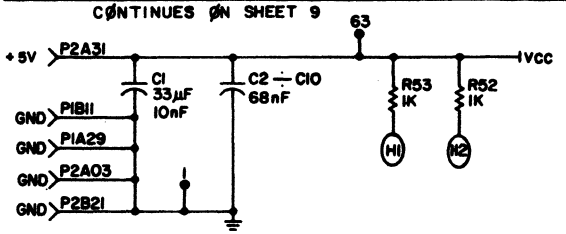
1	9	2	3	4	5	6	7	8
05	05	04	04	04	04	04	04	04
06	05	06	06	06	06	06	06	06
A	A	A	A	A	A	A	A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
04	CK327	REDRAWN PER CDC STD.	L.K.	29.11.73		
05	LK345	CHANGE SH. 1A TO SH. 9	[illegible]	9.12.73	[illegible]	[illegible]
04	CK 651	USE ECO'S 327 AND 651 TO DRAW LOGIC REV. 04 SH. 2 : TP5 SH 3 : TP44, U54-6 SH 4 : TP22 REF LTRS DA SH 5 : TP 58, TP59 REF LTRS DA SH 6 : REF LTRS DY SH 7 : REF LTRS DY, P2B15 SH 8 : U16-15, R33 ÷ R40 SH 9 : REF LTRS DA AND DY	[illegible]	25.7.74		
06	CK 785	CORRECTION OF DWG. ERRORS	[illegible]	26/Aug/74		
A	CK 1478	RELEASED CLASS A. R45 (SH2, C-2), R46 (SH2, C-2) AND R43 (SH3, C-2) CHANGED FROM 190 TO 1K TO MATCH PARTS LIST.	M.L	8.76	G.D	

	2	3	4	5	6	7	8
AR		B-1				B-4	
AS		A-1				B-4	
AT		A-1		A-2			
AU		B-1		B-2			
AV		C-1		D-2			
AW		D-1		D-2			
AX		A-2					C-3
AY		A-1					C-3
AZ		A-3					C-3
BA		A-1					D-3

CØNTINUES ØN SHEET 9



NØTE: ALL RESISTØRS ARE 0.25 WATT 5%

P.L. 89614100
A.W. 89614200
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES
TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL N/A

FINISH N/A

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

FIRST USED ON AB107-A AB108-A

DWN		
CHKD	[illegible]	2.12.74
ENGR	DAVID WEISS	3.12.74
MFG	A. ADECA	12.5.75
APPR	YOHAI J.	3.17.75
QA	Arnie Nagler	[illegible]

TITLE
DETAILED LOGIC DIAGRAM
ALU

CODE IDENT C

DRAWING NO 89614300

SCALE N/A

SHEET 1 OF 9

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

ØFF-SHEET REFERENCES (CØNTINUED FRØM SHEET 1)

	2	3	4	5	6	7	8
BB				D-1		B-4	
BC				C-1		B-4	
BD				B-1		B-4	
BE				A-1		B-4	
BF			D-2	D-2			
BG			D-2	D-2			
BK			D-2	D-2			
BL			D-2	D-2			
BM			D-2	D-2			
BN			A-3	A-3			
BP		D-3		D-3			
BR		D-3		D-3			
BS		D-3		C-3			
BT			D-3	D-3			
BZ		C-4		B-4		D-1	
BU			D-3	D-3			
BY		C-4		B-4		C-1	
BV			B-4	B-4			
BW		C-4		B-4		A-1	
BQ		D-3		D-3			
CA			C-4	C-4			
CB			D-4	D-4			
CC				B-2		A-1	
CD				B-2		B-1	
CE				B-2		C-1	
CF				B-2		D-1	
CG		B-3			B-4		
CK			A-1		B-3		
CL			B-1		B-3		
CM			C-1		B-3		
CN			D-1		B-3		
CP			B-2		D-1		
CR			B-2		B-1		
CS			B-2		A-1		
CT					C-3	C-4	
BX		C-4		B-4		B-1	

	2	3	4	5	6	7	8
CU					C-3	C-4	
CW					B-3	C-4	
CV					C-3	C-4	
CX					B-3	C-4	
CQ			B-2		C-1		
CY					C-2	C-3	
DA			B-3	A-3			
DB					D-2	D-2	
DC					A-1	A-3	
DD					D-2	D-2	
DE					D-2	D-3	
DF					D-2	D-2	
DX				A-3	C-4		
DY					D-1	D-3	

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM ALU	CODE IDENT C	DWG NO 89614300	REV A
			SHEET 9	

ALU (drawing 89614300, sheets 2,3)

ADDEND REGISTERS AND GATES

Function

This section contains the following circuits:

- the addend registers Q, P, M;
- the X register which is used both as an addend and augend register;
- the addend gates and the comparator for comparing the X and Q register contents.

Description

NOTE

As in the rest of the ALU, one board accommodates the circuitry sufficient for eight bits and therefore two boards are used. In the following the numbers refer to the lower eight bits 00 through 07 (ALU slot location 25): for the board dealing with the upper eight bits (08 through 15) increment the bit number by eight.

The Q, P and M registers store the information selected by the shifter (refer to sheets 6,7). Each one is timed by a separate clock signal (QCK, PCK, MCK) generated on the Timing board.

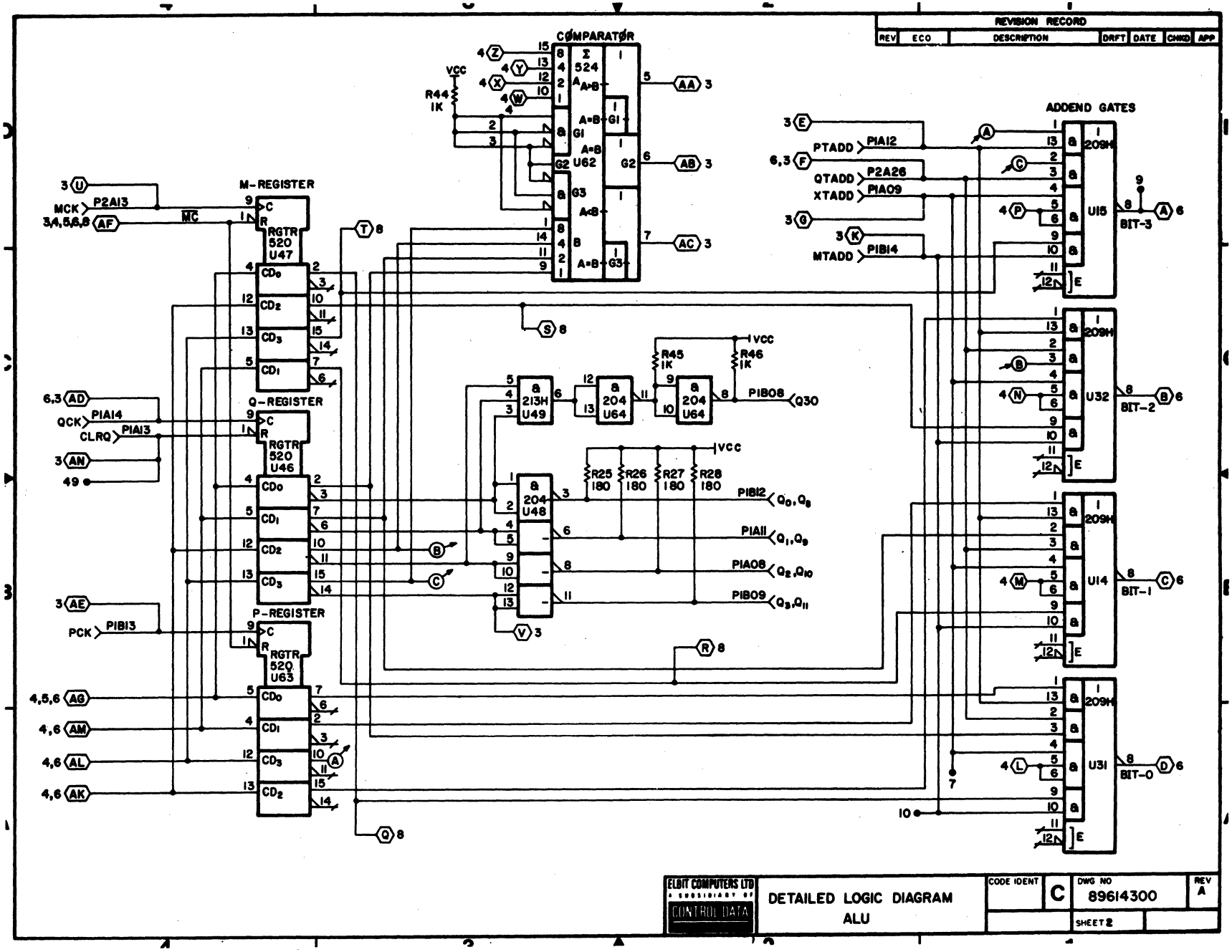
The P and M registers are reset by the Master Clear ($\overline{MC}$) signals, the Q register by its own clear signal (CLRQ). The Q register outputs supply the A/Q channel bus through open collector buffers U36, U48. The three least significant bits of the Q register are also sent, in complement form, to a three-input AND gate (U49/6) to produce the signal Q30 = $\overline{Q00} \cdot \overline{Q01} \cdot \overline{Q02}$. This signal leaves the board through an open-collector driver.

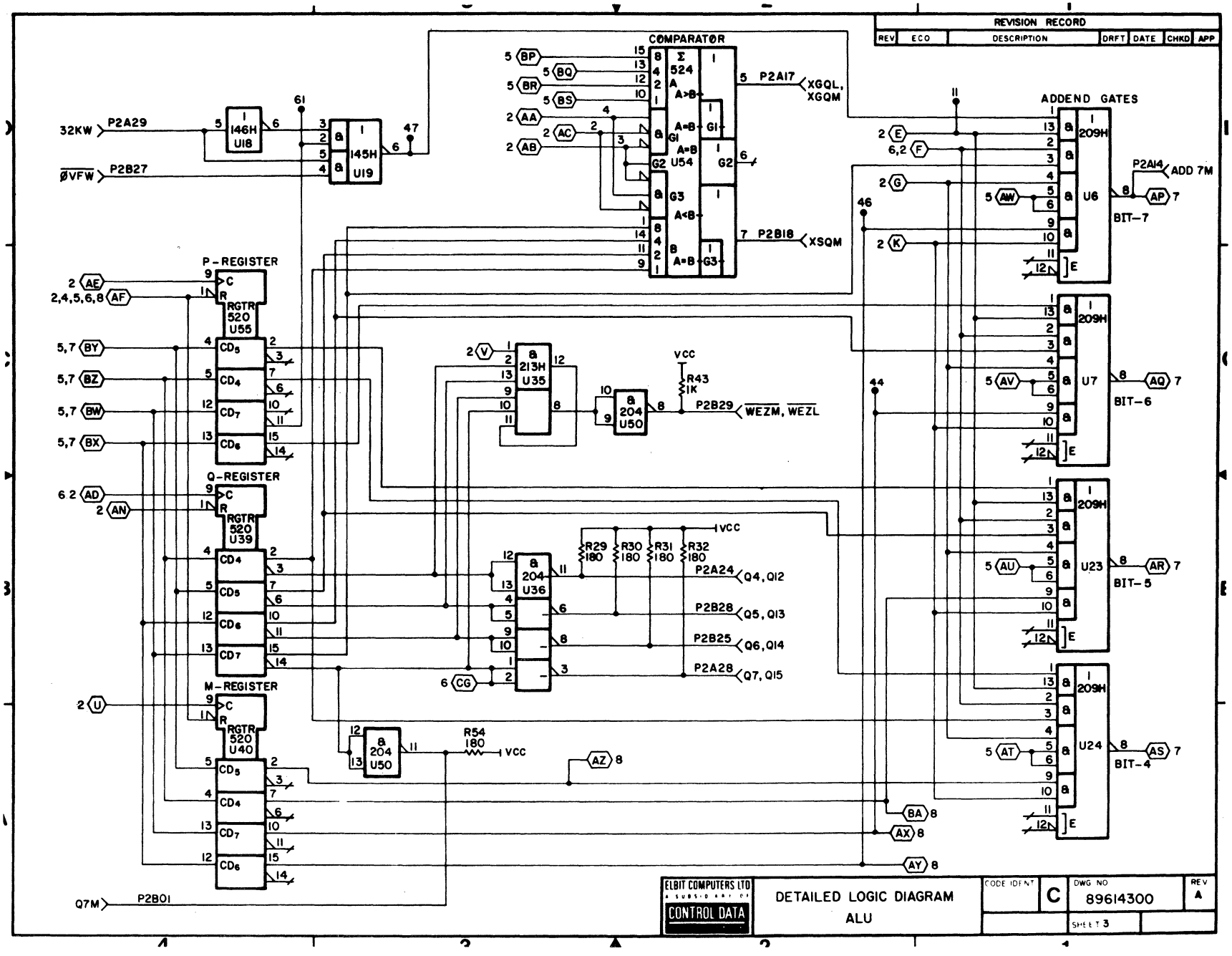
ALU (drawing 89614300) sheets 2, 3, cont'd.

The five higher bits of the Q register (the W field) are used to produce the function $\overline{WEZ} = \overline{\overline{Q03} \cdot \overline{Q04} \cdot \overline{Q05} \cdot \overline{Q06} \cdot \overline{Q07}}$ at U35/8. The signal, from the most significant ALU board, is sent to the A/Q channel through the console interface board. The $\overline{WEZ}$ and Q30 signals from both ALU boards are used to sense when the contents of the Q register is zero (see Console Interface sheet 6).

The X register and its associated selector are described on pages facing sheets 4, 5 of the ALU circuit. The comparator U54, U62 compares the outputs of the Q register with the complement of the X register. This comparator produces the signals XSQ and XGQ (X<Q, X>Q) which are sent to the console interface card. This comparator is used only during divide instruction. Because the absolute values of X and Q must be compared and the X register content is always negative during the divide instructions, the complement of the X register content is input to the comparator.

The addend selector gates select the outputs of one of the addend register for transfer to the ALU under control of the signals QTADD, PTADD, MTADD and STADD.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
COMPARATOR
ADDEND GATES
M-REGISTER
Q-REGISTER
P-REGISTER
RGTR 520 U47
RGTR 520 U46
RGTR 520 U63
MCK P2AI3
QCK PIAI4
CLRQ PIAI3
PCK PIBI3
PTADD PIAI2
QTADD P2A26
XTADD PIA09
MTADD PIBI4
R44 1K
R45 1K
R46 1K
R25 180
R26 180
R27 180
R28 180
U15 BIT-3
U32 BIT-2
U14 BIT-1
U31 BIT-0
PIBI2 Q0,Q8
PIAII Q1,Q9
PIA08 Q2,Q10
PIB09 Q3,Q11
PIB08 Q30
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
ALU
CODE IDENT C
DWG NO 89614300
REV A
SHEET 2


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
COMPARATOR
ADDEND GATES
P-REGISTER
Q-REGISTER
M-REGISTER
32KW P2A29
ØVFW P2B27
5 BP
5 BQ
5 BR
5 BS
2 AA
2 AC
2 AB
5 P2A17 XGQL, XGQM
7 P2B18 XSQM
2 E
6,2 F
2 G
5 AW
2 K
P2A14 ADD 7M
BIT-7
5 AV
BIT-6
5 AU
BIT-5
5 AT
BIT-4
2 AE
2,4,5,6,8 AF
5,7 BY
5,7 BZ
5,7 BW
5,7 BX
6 2 AD
2 AN
2 U
2 V
6 CG
R43 1K
VCC
P2B29 WEZM, WEZL
R29 180
R30 180
R31 180
R32 180
P2A24 Q4, Q12
P2B28 Q5, Q13
P2B25 Q6, Q14
P2A28 Q7, Q15
R54 180
AZ 8
BA 8
AX 8
AY 8
Q7M P2B01
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
ALU
CODE IDENT C
DWG NO 89614300
REV A
SHEET 3

ALU (drawing 89614300, sheets 4, 5).

AUGEND REGISTERS AND GATES

Function

This circuit contains the augend registers A, Y and the augend gates; as well as the X register, which is used both as an augend and addend register.

Description

NOTE

As in the rest of the ALU, one board accommodates the circuitry sufficient for eight bits and therefore two boards are used. In the following the numbers refer to the lower eight bits 00 through 07 (ALU slot location 25); for the board dealing with the upper eight bits 08 through 15) increment the bit number by eight.

The A and Y register store the information selected by the shifter (refer to sheets 6, 7). Each one is timed by a separate clock signal (ACK, YCK) generated on the Timing board. The X register stores either the shifter outputs or the MX outputs of the memory control board. The choice between the two inputs is made in the X selector (U53, U61) under control of the signal XEZ from the I/O interface circuit.

The MX data from the memory control board is the memory output during a read memory reference cycle: MX00 through MX07 for the ALU board dealing with the least significant bits, MX08 through MX15 for the ALU board dealing with the most significant bits.

The MX data lines are terminated in 330 ohm pull-up resistors on the ALU boards

The A and Y registers are reset by Master Clear ($\overline{MC}$) whereas the X register has its own clear signal (CLRX).

ALU (drawing number 89614300) sheets 4, 5, cont'd.

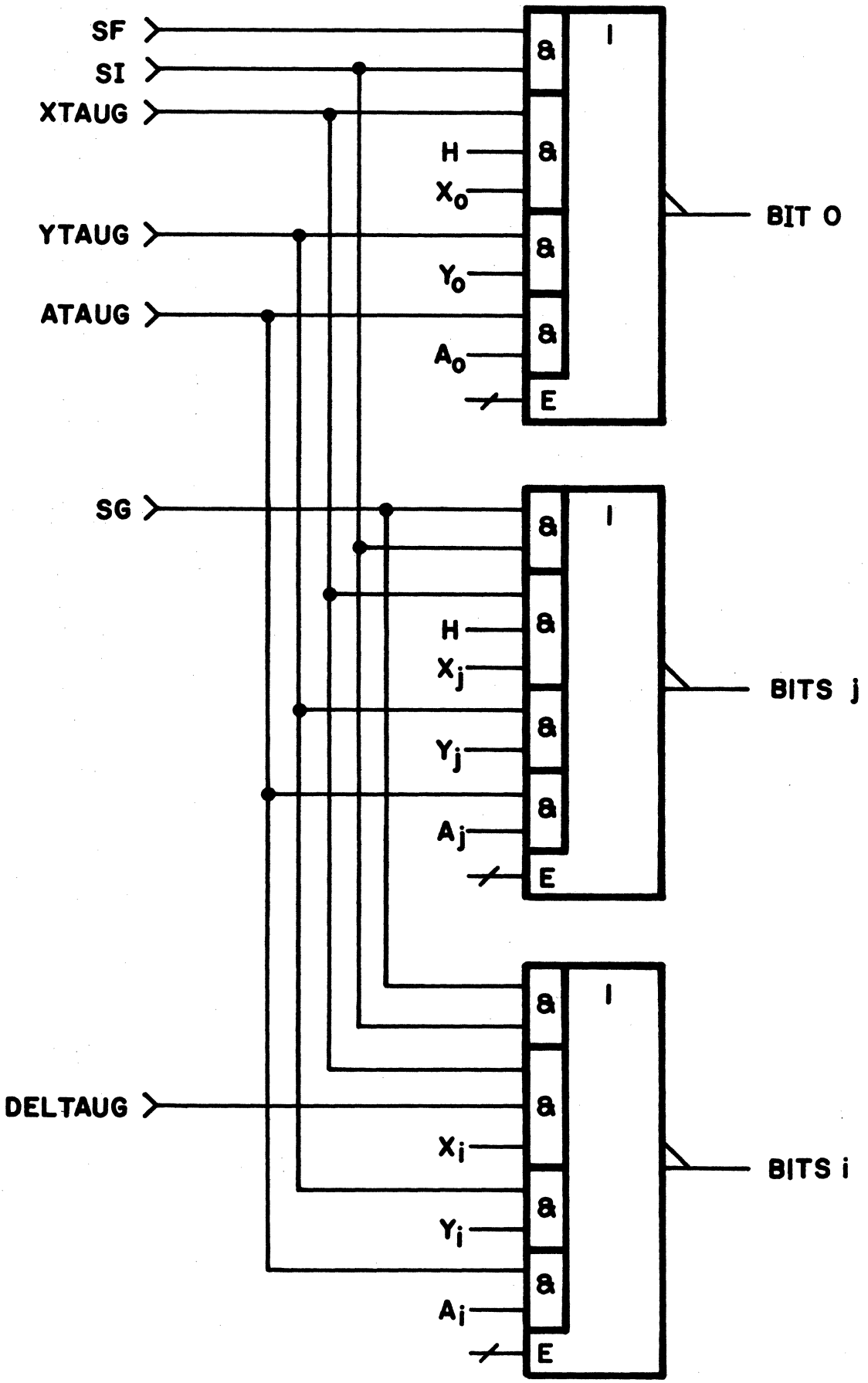
The outputs of the A, Y and X registers form some of the inputs of the augend selector gates. The outputs of any one register are transferred to the augend gates under control of the signals ATAUG, YTAUG, XTAUG.

The other control inputs to the augend selector gates are SG, SI, SF and DELTAUG.

The following figure shows the augend gate control signal connections.

Notes (to Augend Gate Control Signals):

1. j are bits 01 ÷ 03 on the LSB, bits 09 ÷ 11 on the MSB.
2. i are bits 04 ÷ 07 on the LSB, bits 12 ÷ 15 on the MSB.


SF
SI
XTAUG
YTAUG
ATAUG
SG
DELTAUG
H
X_0
Y_0
A_0
E
BIT 0
H
X_j
Y_j
A_j
E
BITS j
X_i
Y_i
A_i
E
BITS i

ALU (drawing 89614300) sheets 4, 5, cont'd.

The augend selector gates can, with the aid of the above signals, transfer the content of the A register, Y register, or X register to the ALU. These gates can also transfer part of the content of the X register with the upper bits zero, as follows:

Transfer Signal	X Register Bits transferred	Remarks Remaining X-Register bits:
DELTAUG	00 ÷ 03	12 bits recognized as zero
DELTAUG	00 ÷ 07	8 bits recognized as zero
	00 ÷ 07	8 bits sign-extended according to bit X07

The output of the augend gates is active low.

The following table summarizes the selection of the constants:

Control Signal	Constant Selected
SI•SF	+1
SI•SG	-1
SI•SF•SG	-0
$\overline{ATAUG}\cdot\overline{YTAUG}\cdot\overline{XTAUG}\cdot\overline{SI}$	+0

ALU (drawing 89614300) sheets 4, 5, cont'd.

The following truth tables show the augend gate control signal configurations for both ALU boards and the corresponding augend gate outputs.

AUGEND SELECTOR - MOST SIGNIFICANT BOARD (MSB)

Augend Gate Control and (Corresponding Signal)							Augend Gate Output (active low)
ATAUG (ATAUG)	YTAUG (YTAUG)	XTAUG (XTAUG)	DELTAUG (H)	SF (SE)	SG (SSE)	SI (IM)	
H	L	L	H	L	L	X07	A register
L	H	L	H	L	L	X07	Y register
L	L	H	H	L	L	X07	X register
L	L	L	H	H	H	X07	Extended sign bit of Δ
L	L	L	H	L	L	X07	00_{16}
L	L	L	H	H	H	H	FF_{16}

AUGEND SELECTOR - LEAST SIGNIFICANT BOARD (LSB)

Augend Gate Control and (Corresponding Signal)							Augend Gate Output (active low)
ATAUG (ATAUG)	YTAUG (YTAUG)	XTAUG (XTAUGL)	DELTAUG (DELTAUG)	SF (SFL)	SG (SGL)	SI (SIL)	
H	L	L	H	H	L	L	A register
L	H	L	H	H	L	L	Y register
L	L	H	H	H	L	L	X register
L	L	H	L	H	L	L	lower 4 bits of X, "0" extended
L	L	L	H	H	L	H	01_{16}
L	L	L	H	L	H	H	FE_{16}

The signals ATAUG, XTAUGL, XTAUGM, and SIL are produced on the decoder board. The signals YTAUG and SGL are produced on the timing board. The signals SFL, IM, SE, and DELTAUG are produced on the I/O interface board.

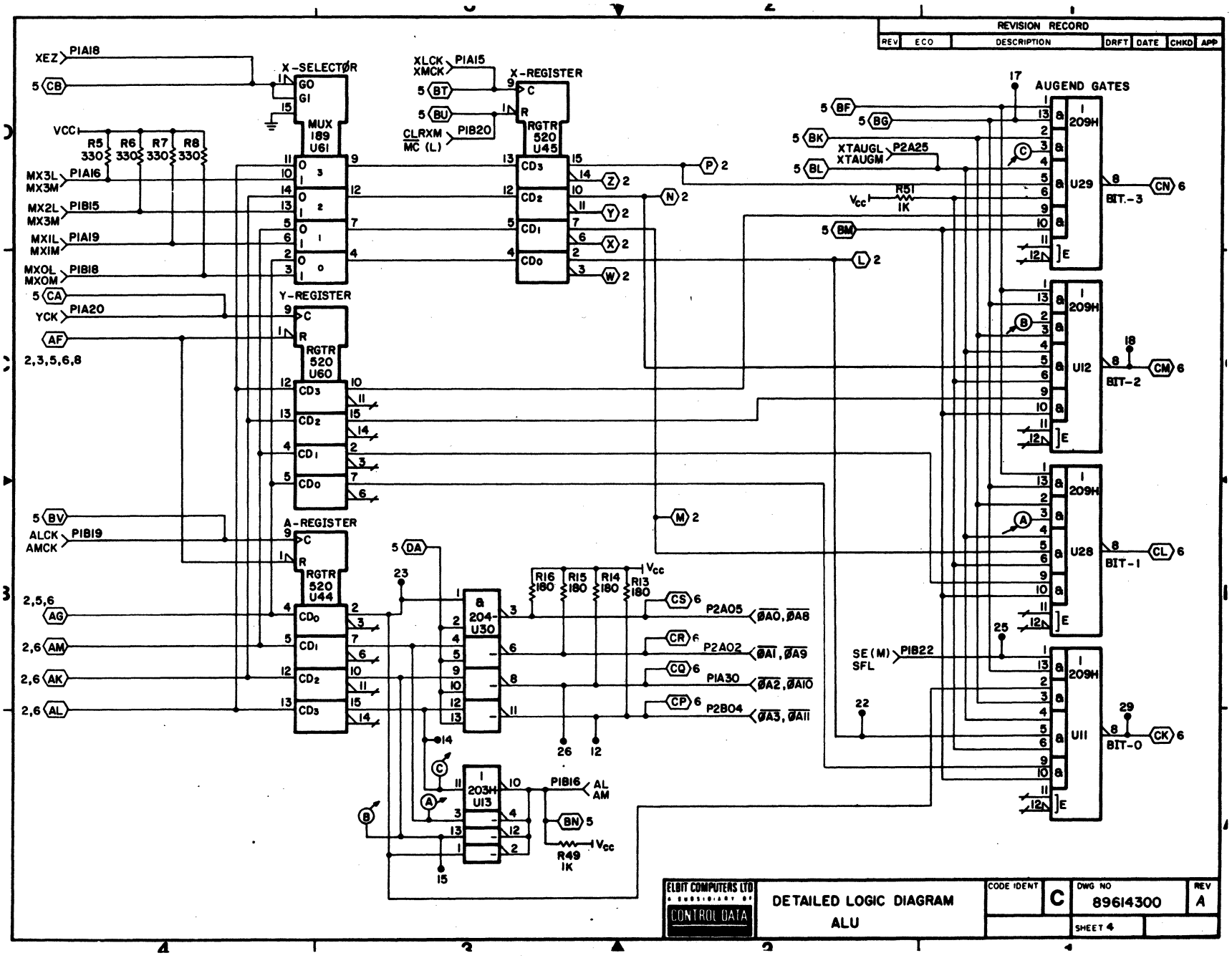
H = active high, L = active low

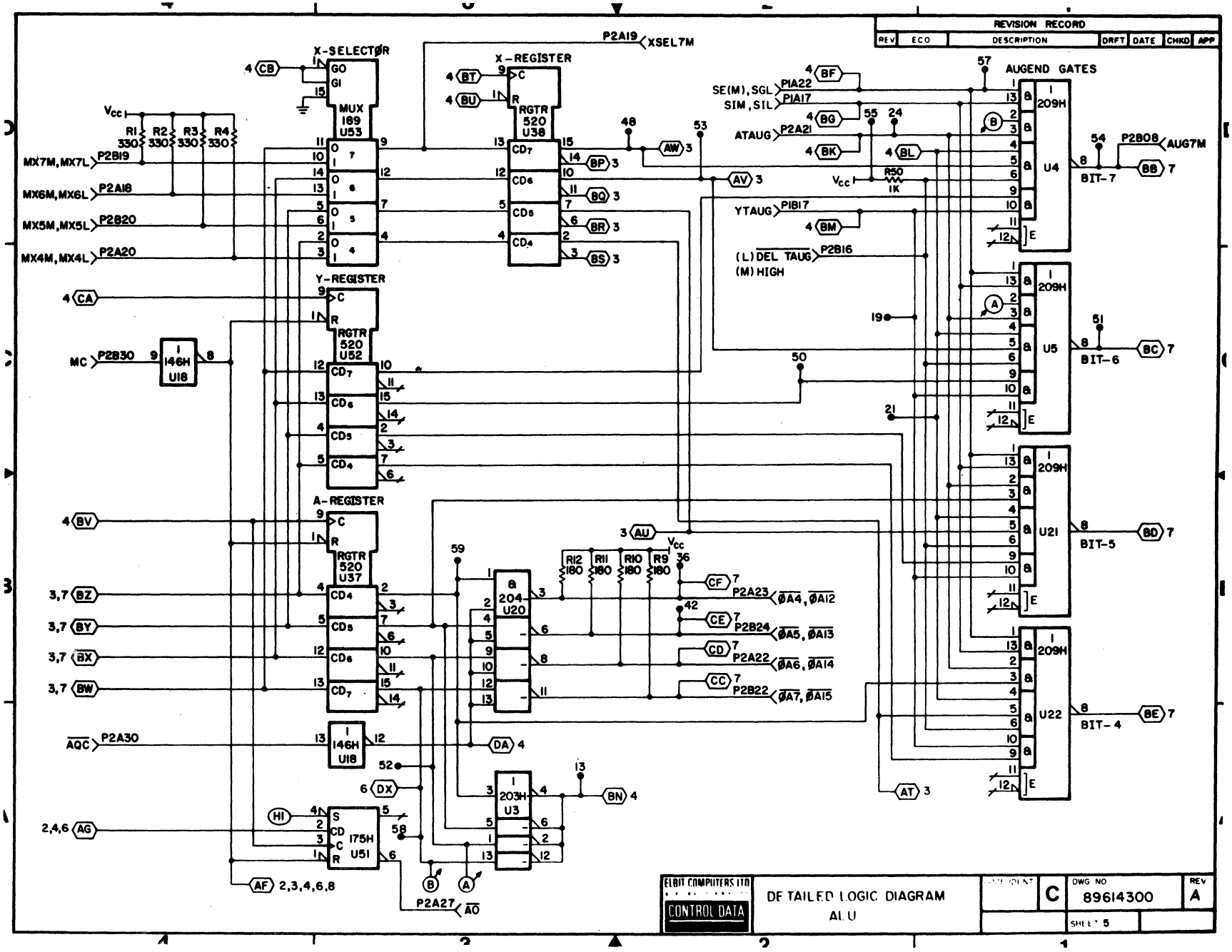
ALU (drawing 89614300) sheets 4,5, cont'd.

The A register outputs supply the A/Q channel bus through open-collector NAND gates. The outputs of these gates are controlled by the A/Q channel control signal, AQC, from the I/O interface.

The A register outputs are wire-ANDed after inversion in U13 and U3 to produce the signal AEZ. This indicates whether the content of the A register is zero.

This circuit includes a flip-flop (U51/6) which stores the least significant bit of the A register. The input to the flip-flop is the least significant bit of the shifter. It is clocked by the A register clock and cleared by Master Clear ($\overline{MC}$). Its output is used during multiply instructions where this bit must be stable early in the cycle.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
X-SELECTOR
MUX 189 U61
X-REGISTER
RGTR 520 U45
Y-REGISTER
RGTR 520 U60
A-REGISTER
RGTR 520 U44
AUGEND GATES
209H U29
209H U12
209H U28
209H U11
204-U30
203H-U13
XEZ PIAI8
XLCK XMCK PIAI5
CLRXM MC (L) PIB20
MX3L MX3M PIAI6
MX2L MX3M PIBI5
MXIL MXIM PIAI9
MXOL MXOM PIBI8
YCK PIA20
ALCK AMCK PIBI9
XTAUGL XTAUGM P2A25
SE(M) SFL PIB22
R5 330 R6 330 R7 330 R8 330
R16 180 R15 180 R14 180 R13 180
R51 1K
R49 1K
BIT-3
BIT-2
BIT-1
BIT-0
P2A05 ØA0, ØA8
P2A02 ØA1, ØA9
PIA30 ØA2, ØA10
P2B04 ØA3, ØA11
PIB16 AL AM
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
ALU
CODE IDENT C
DWG NO 89614300
REV A
SHEET 4


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
X-SELECTOR
MUX 189 U53
X-REGISTER
RGTR 520 U38
Y-REGISTER
RGTR 520 U52
A-REGISTER
RGTR 520 U37
AUGEND GATES
209H U4
209H U5
209H U21
209H U22
146H U18
204 U20
203H U3
175H U51
BIT-7
BIT-6
BIT-5
BIT-4
P2A19 XSEL7M
P2B19 MX7M, MX7L
P2A18 MX6M, MX6L
P2B20 MX5M, MX5L
P2A20 MX4M, MX4L
P2B30 MC
P2A30 AQC
P2A27 A0
P2A23 ØA4, ØA12
P2B24 ØA5, ØA13
P2A22 ØA6, ØA14
P2B22 ØA7, ØA15
P1A22 SE(M), SGL
P1A17 SIM, SIL
P2A21 ATAUG
P1B17 YTAUG
P2B16 (L) DEL TAUG
(M) HIGH
P2B08 AUG7M
R1 330
R2 330
R3 330
R4 330
R50 1K
R9 180
R10 180
R11 180
R12 180
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
ALU
SIZE C
DWG NO 89614300
REV A
SHEET 5

ALU (drawing 89614300) sheets 6, 7

ARITHMETIC AND LOGIC OPERATIONS

Function

The ALU microcircuits U57, U59 form the heart of the ALU board. They perform the nine arithmetic and logical functions used in the computer.

Description

NOTE

As in the rest of the ALU, one card accommodates the circuitry sufficient for eight bits and therefore two boards are used. In the following, the numbers refer to the lower eight bits 00 through 07 (ALU slot location 25); for the board dealing with the upper eight bits (08 through 15), increment the bit number by eight.

The outputs of the addend and augend gates are combined in the ALU microcircuits, the four lower bits going to U59, the four upper bits to U57. The control inputs (S00 through S03, M) are generated in the Decoder board. The carry look-ahead function is provided in the Console Interface circuit which produces the four carry signals for the ALU boards.

The ALU microcircuit outputs (ALU00 through ALU07) form the inputs to the shifter and feed the ALU bus through 33 ohm series termination resistors.

The ALU bus carries CPU memory address and memory data to the memory address card of both the internal and the optional expansion memory banks.

The CNS data gates, (U56, U58) are open collector NAND gates which transfer ALU data to the bi-directional CNS data bus. The CNS data gates are controlled by the signal CLREG from the programmer's console.

ALU (drawing 89614300)sheets 6,7, cont'd.

The ALU Microcircuit (509)

The Arithmetic Logic Unit (ALU) microcircuit is a commercial I.C. package (509 or 74181/9341 described in the Key to Logic Symbols, Control Data publication number 89723700 (or equivalent) and in manufacturer's specifications. Its salient features are repeated here and its specific use in the computer ALU circuit is described.

The parallel ALU is controlled by the four Function Select inputs (S0,S1,S2,S3, having binary designation 1,2,4,8) and the Mode Control input (M). It can perform all the 16 possible logic operations or 16 different arithmetic operations on active high or active low operands. In this computer it operates on active low data because the addend and augend selector gates complement the data.

When the Mode Control input (M) is high, all the internal carries are inhibited and the device performs logic operations on the individual bits. When the Mode Control input is low, the carries are enabled and the device performs arithmetic operations on the two, 4-bit words. The device incorporates full internal look-ahead carry and provides for either ripple carry between devices using the signals PL (carry propagate) and GL (carry generate). PL and GL are not affected by carry in. When speed requirements are not stringent the 74181 can be used in a simple ripple carry mode by connecting the carry out 16 (pin 16) signal to the carry input (C) of the next unit. For high speed operation the 74181 is used in conjunction with the 74182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 74181 devices.

ALU (drawing 89614300) sheets 6,7, cont'd.

The computer ALU circuits utilize nine of the possible 32 functions of the ALU microcircuit. The functions and the control signals are shown in the following table.

MODES OF OPERATION OF ALU MICROCIRCUIT (509)

INPUTS					FUNCTION	DESCRIPTION
M	S3	S2	S1	S0		
H	L	L	L	L	$\overline{\text{AUGEND}}$	1. Complements the register selected by the Augend.
H	L	L	L	H	$\overline{\text{ADDEND}\cdot\text{AUGEND}}$	2. NAND function
H	L	H	L	H	$\overline{\text{ADDEND}}$	3. Complements the register selected by the Addend
H	L	H	H	L	$\overline{\text{ADDEND}\oplus\text{AUGEND}}$	4. Transfers register content (except Q) through the ALU when the computer is stopped.
H	L	H	H	H	AUGEND·ADDEND	5. Transfer the Q register content through the ALU when the computer is stopped. (In this case Augend is zero).
H	H	L	L	H	ADDEND⊕AUGEND	6. Exclusive-OR function
H	H	H	H	L	ADDEND·AUGEND	7. AND function
L	L	H	H	L	AUGEND MINUS ADDEND	8. Subtraction
L	H	L	L	H	AUGEND PLUS ADDEND	9. Addition

H = logic high, L = logic low

ALU (drawing number 89614300) sheets 6,7

SHIFTER

Function

The shifter outputs determine which data is valid at the input of the CPU registers at the end of a cycle.

Description

NOTE

As in the rest of the ALU, one card accommodates the circuitry sufficient for eight bits and therefore two boards are used. In the following the numbers refer to the lower eight bits 00 through 07 (ALU slot location 25); for the board dealing with the upper eight bits (08 through 15) increment the bit number by eight.

The circuit consists of eight-input selectors (505), one for each bit of a computer word, and a flip-flop. Each selector is controlled by three selector lines (three of C0 through C3) which select one of the eight input signals. The table following the next paragraph is the truth table for the shifter, together with the operation of the ALU circuits. The circuit functions are explained in the paragraphs following the table.

Shift Flip-Flop

In addition to the selectors, the ALU board carries the Shift flip-flop and associated gating (U51/8,9 and U26, U3/8,10, U18/2,4,10, U19/8). The flip-flop, located on each ALU board, stores information during the first step of a double-word long shift. The information stored is from the ALU board itself or generated in the current cycle on another board. It is stored here so that it should not be lost at the end of the cycle, as it may be needed during the second step of the long shift. During the first step of a long shift or during a short shift the content of the flip-flop is never used. It is sometimes used in the second step of a long shift.

SHIFTER CIRCUIT OPERATION

Control Signals				Selects Input No.		OUTPUTS				
C3	C2	C1	C0	Bits j	Bits i	Bit 7 (15)	Bit i	Bit 0	Input of flip-flop	Operation
L	L	L	L	0	0	ALU06	ALU_{i-1}	$\overline{Z3}$		Short left shift
L	L	L	H	1	0	ALU06	ALU_{i-1}	SHB	Z5	First step of long left shift; used only during divide instruction. This code used also during second step of any long left
L	L	H	L	2	2	SHC	ALU_{i+1}	ALU01	$\overline{ALU00}$	Second step of any long right shift
L	H	L	L	4	4	ALU07	ALU_i	ALU00		Direct transfer ALU data
L	H	H	L	6	6	Z1	ALU_{i+1}	ALU01	$\overline{ALU00}$	Short right shift or first step of any long right shift
H	L	L	H	1	1	ALU06	ALU_{i-1}	SHB	Q	First step of cyclic long left shift in shift instruction.
H	L	H	H	3	3	H	$\overline{ITA_i}$	$\overline{ITA0}$		Transfer trap address
H	H	L	H	5	5	QA07	QA_i	QA00		Transfer A/Q data
H	H	H	H	7	7	$\overline{CNS07}$	$\overline{CNS_i}$	$\overline{CNS00}$		Transfer CNS data

NOTES:

. i = 01 through 06, j = 00, 07 for ALU board in slot 25 (LSB)
  09 through 14, j = 08, 15 for ALU board in slot 26 (MSB).

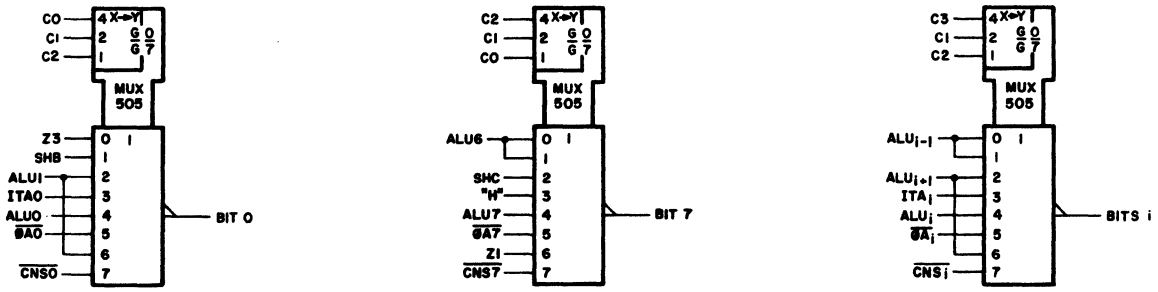
. for i = 01, 06, 10 ÷ 13 connected to H.

. High= logic high; L=logic low

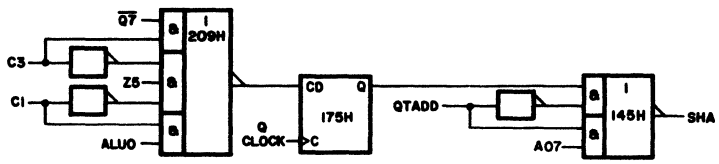
3. Control inputs are connected as follows:

	Control signals			
Bits	C0	C1	C2	C3
i	-	B	C	A

The connections to the shifter selectors and flip-flop are summarized in the following figure.



SHIFTER SELECTORS



SHIFT FLIP-FLOP

ALU (drawing 89614300)sheets 6,7, cont'd.

Shift Operations

NOTE

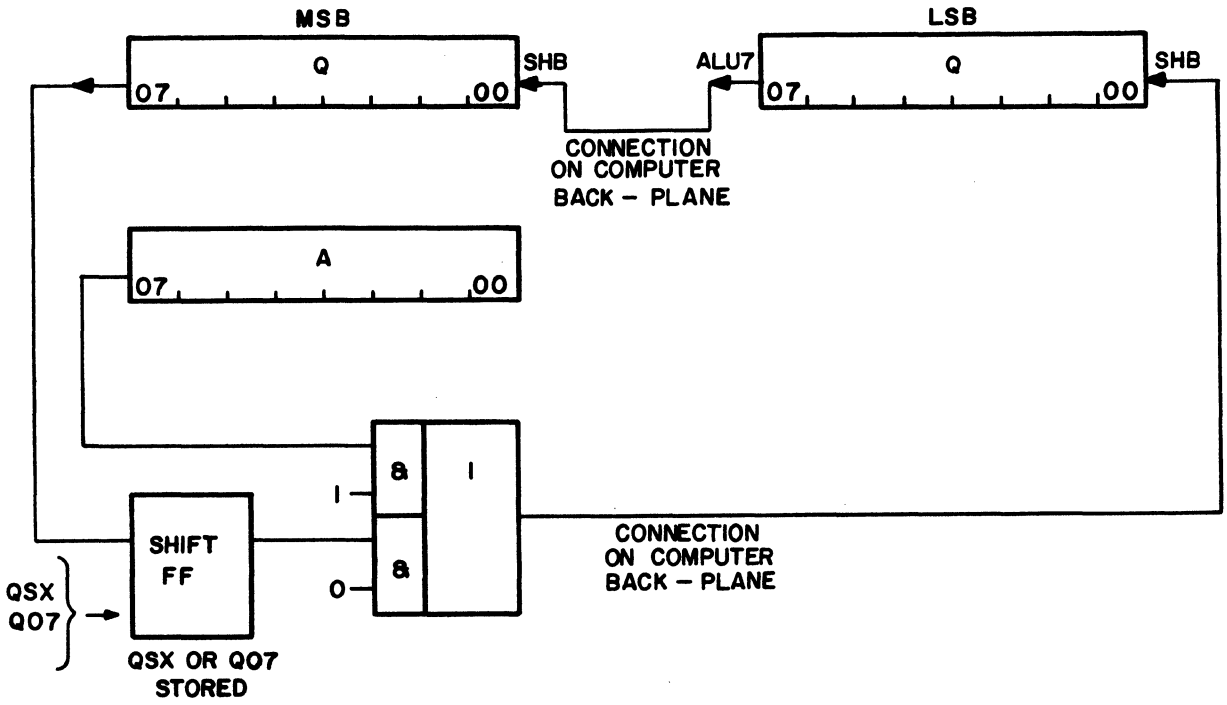
Timing diagrams for shift operations are given in the first sheet for the Timing circuits in section 5.

During a short left shift, each output of the shifter receives the next lowest bit of the ALU. The lowest bit of the shifter (SH00) receives the signal Z3.

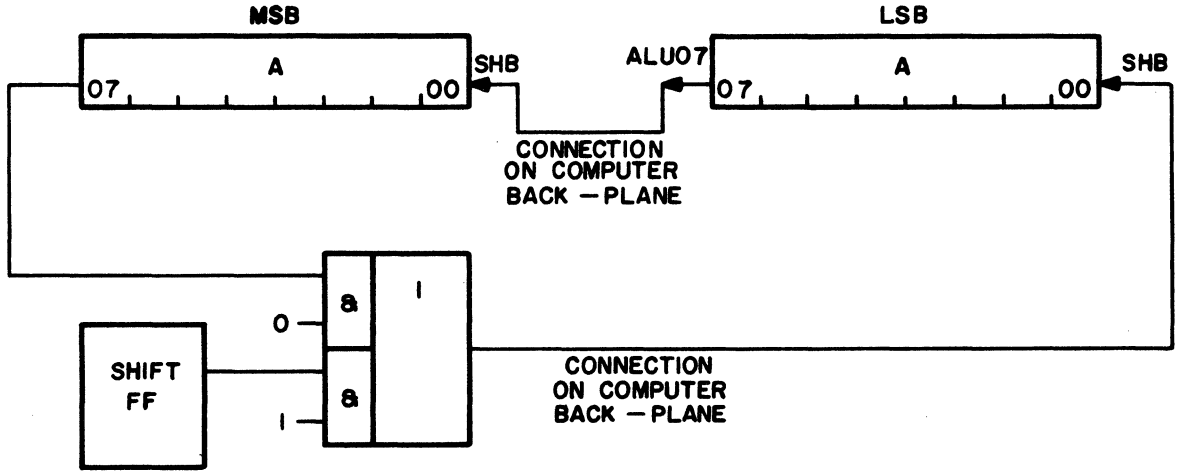
The signal Z3 of each ALU board is wired to the most significant bit of the ALU output on the other ALU board. Thus the shift is cyclic.

The first step of a long left shift is similar to a short shift. During the first step of a long left shift during divide, the SH00 bit is connected to SHB. During this time, the signal QSX is stored in the shift flip-flop. QSX is equivalent to the end-around-borrow resulting from substracting the X register from the content of the Q register (X from Q). In the MSB, SHB is connected to ALU07 of the LSB. In the LSB, SHB is connected to SHA of the MSB. During the first step of a long left shift, the signal QTADD is high so that SHA becomes bit A07 of the MSB.
During the second step, QTADD is low so that SHA becomes the bit that was previously stored in the shift flip-flop.

The first step of a cyclic long left shift differs from a long left shift in that the bit stored in the Shifter/register is Q07 of the MSB. The execution of a long left shift is shown below.



1. First step of double word left shift.



2. Second step of double word left shift.

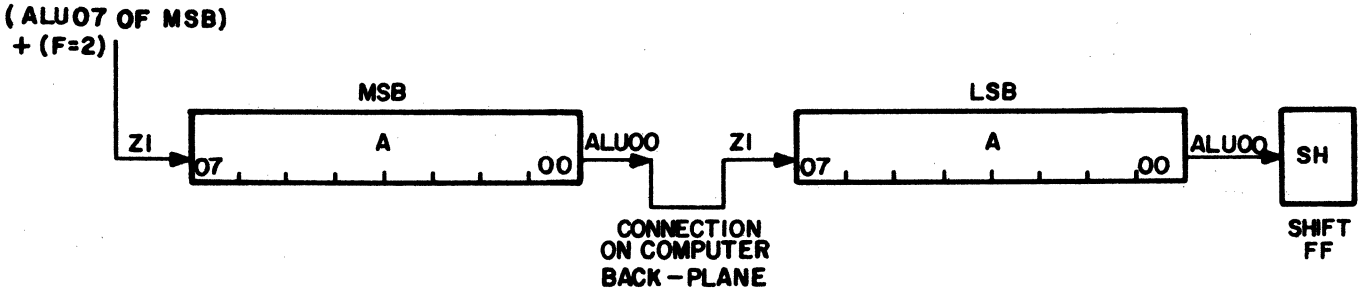
The short right shift may also be used as the first step of a long right shift. During the operation each bit is shifted one place to the right. The least significant bit ALU0 is stored in the shift flip-flop. The most significant bit of the shifter receives Z1. In the LSB Z1 is connected to ALU0 of the MSB. In the MSB Z1 is connected to the function.

(ALU07 of MSB) + (F = 2)

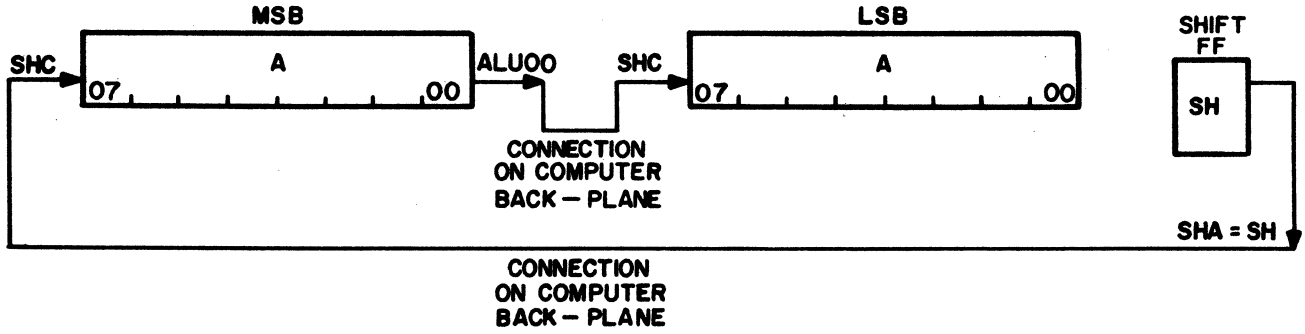
This causes the resulting word to be sign-extended, except during multiplication, when a positive sign is assumed.

The second step of a long right shift is the same as the first except that SH07 receives the input SHC. On the LSB, SHC is connected to ALU00 of the MSB while on the MSB it is connected to SHA of the LSB.

The execution of a long right shift is shown below.



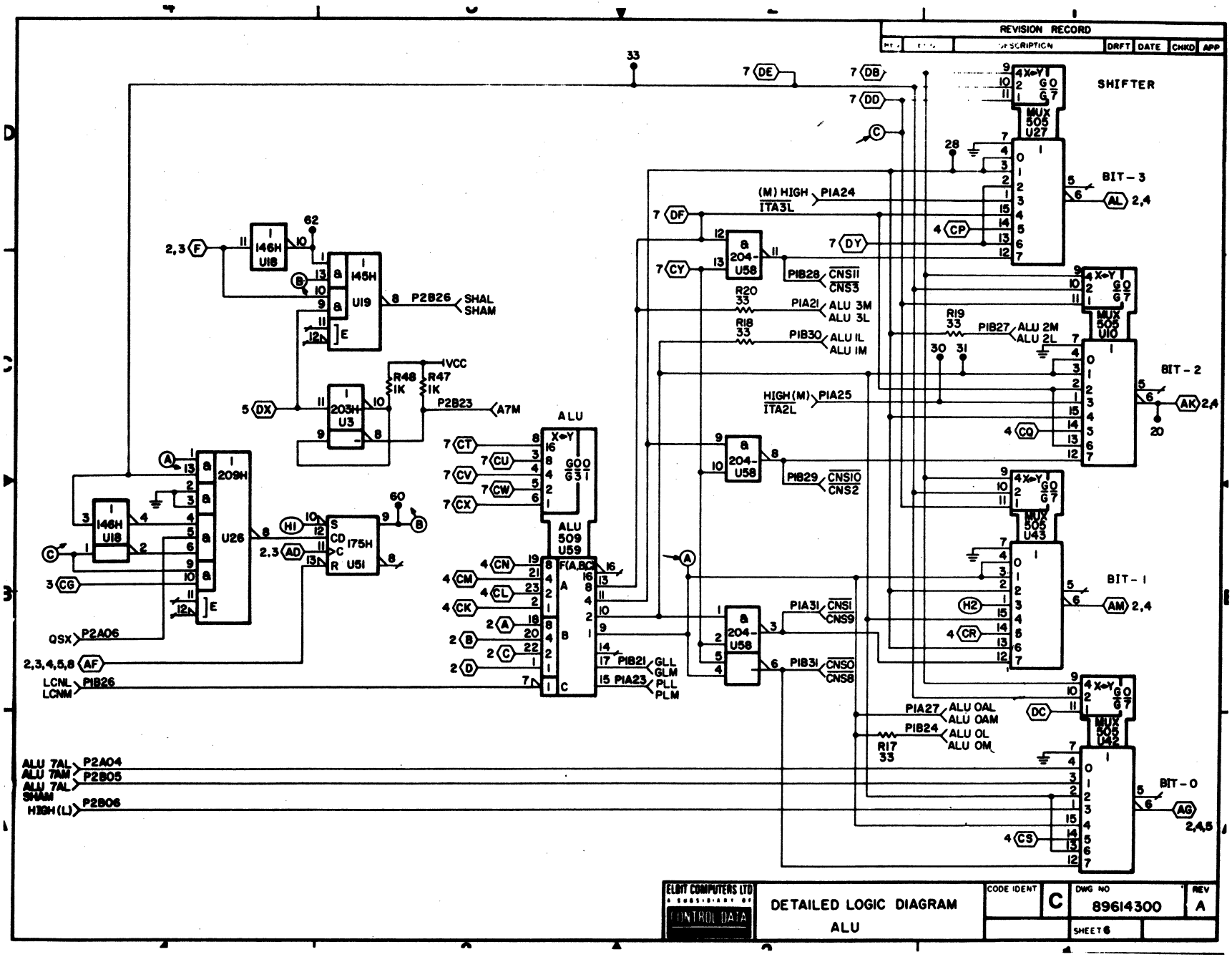
1. First step of double word right shift.

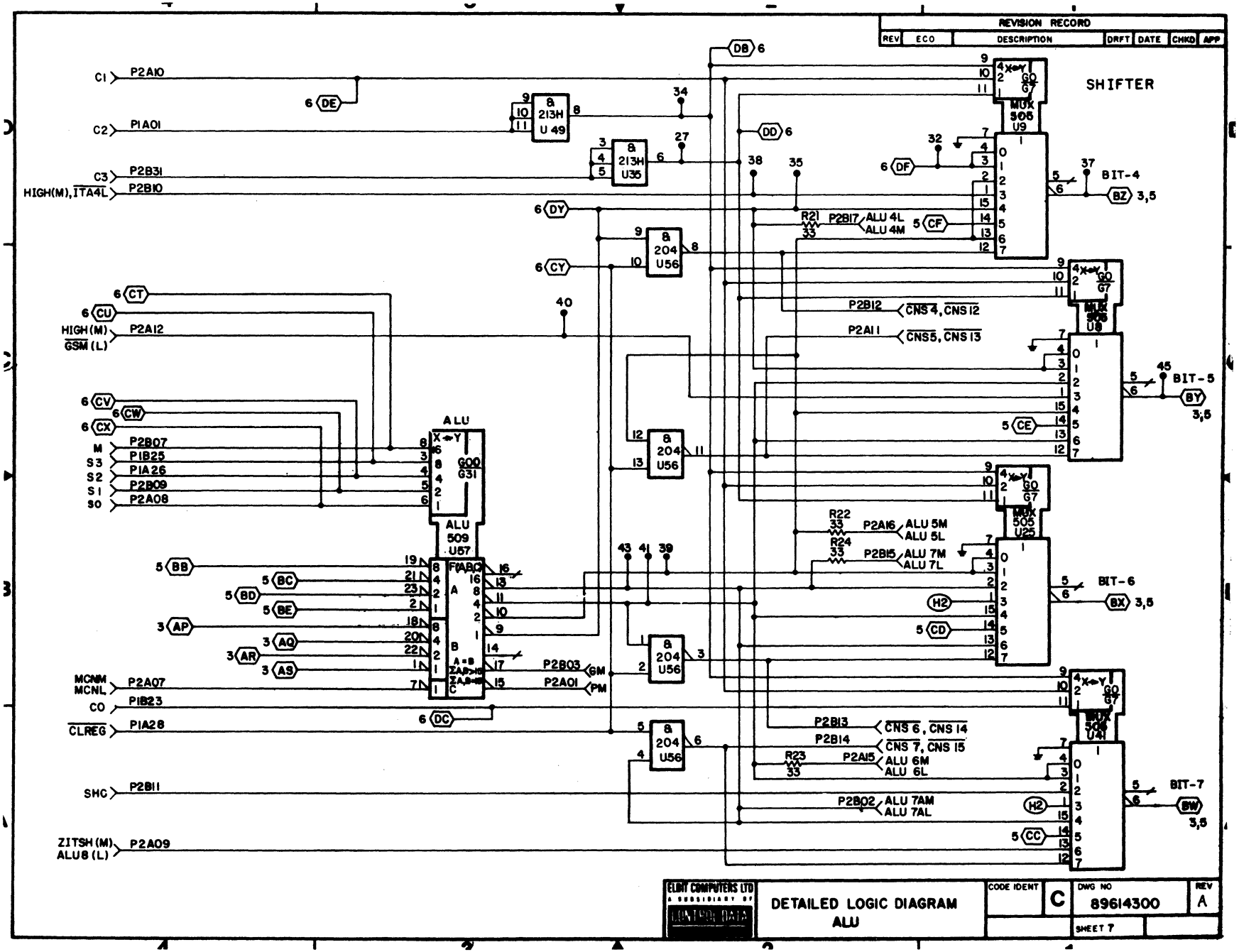


2. Second step of double word right shift.

The signals which are used during double word shifts to control the end bits in the shift flip-flop are connected as follows:

INPUT	SIGNAL	
	Most significant board	Least significant board
Z1	Z1TSH = (F = 2)+(ALU00 of MSB)	ALU00 of MSB
Z3	ALU07 of LSB	ALU07 of MSB
Z5	QSX	QSX
SHB	ALU07 of LSB	SHA of MSB
SHC	SHA of LSB	ALU00 of MSB


REVISION RECORD
DESCRIPTION
DRFT
DATE
CHKD
APP
SHIFTER
ALU
BIT-3
BIT-2
BIT-1
BIT-0
DETAILED LOGIC DIAGRAM
ALU
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
CODE IDENT
C
DWG NO
89614300
REV
A
SHEET 6


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
SHIFTER
ALU
ALU 509 U57
MUX 505 U9
MUX 505 U8
MUX 505 U25
MUX 505 U41
8 213H U49
8 213H U35
8 204 U56
BIT-4
BIT-5
BIT-6
BIT-7
C1 P2A10
C2 P1A01
C3 P2B31
HIGH(M), ITA4L P2B10
HIGH(M) GSM (L) P2A12
M P2B07
S3 P1B25
S2 P1A26
S1 P2B09
S0 P2A08
MCNM MCNL P2A07
CO P1B23
CLREG P1A28
SHC P2B11
ZITSH(M) ALU8(L) P2A09
R21 33 P2B17 ALU 4L ALU 4M
R22 33 P2A16 ALU 5M ALU 5L
R24 33 P2B15 ALU 7M ALU 7L
R23 33 P2A15 ALU 6M ALU 6L
P2B12 CNS4, CNS12
P2A11 CNS5, CNS13
P2B13 CNS6, CNS14
P2B14 CNS7, CNS15
P2B02 ALU 7AM ALU 7AL
P2B03 GM
P2A01 PM
ELBIT COMPUTERS LTD
DETAILED LOGIC DIAGRAM
ALU
CODE IDENT C
DWG NO 89614300
REV A
SHEET 7

ALU (drawing number 89614300) sheet 8

INTERRUPT LOGIC

Function

This circuit accepts the signals on the interrupt lines and processes them to produce outputs according to the content of the mask (M) register and the predetermined interrupt priority.

Description

NOTE

> As in the rest of the ALU, one card accommodates circuitry sufficient for eight bits and therefore two boards are used. In the following the numbers refer to the lower eight bits 00 through 07 (ALU slot location 25): for the board dealing with the upper eight bits (08 through 15) increment the bit number by eight.

The interrupt signals are stored in the interrupt register (U16, U17). This is clocked by the interrupt clock (INTCK) from the Timing board and reset by Master Clear ($\overline{MC}$). The signals on the interrupt lines are active low.

ALU (drawing number 89614300) sheet 8, cont'd.

The outputs of the register are gated through to a priority encoder (U65) under control of the content of the M register. The priority signals coinciding with a logic high in the M register are allowed to pass, and are considered active.

The priority decoders on the two ALU boards are connected in cascade to detect the highest priority interrupt which is active at any time. The interrupts have ascending priority from INT15 to INT08 and from INT07 to INT00,the interrupts on the board dealing with the least significant data bits (LSB) having priority.

The following table shows the operation of the priority encoder:

	INPUTS									OUTPUTS			
EI	0	1	2	3	4	5	6	7	GS	TA2	TA1	TA0	EØ
1	X	X	X	X	X	X	X	X	H	H	H	H	H
0	H	H	H	H	H	H	H	H	H	H	H	H	H
0	X	X	X	X	X	X	X	L	L	L	L	L	H
0	X	X	X	X	X	X	L	H	L	L	L	H	H
0	X	X	X	X	X	L	H	H	L	L	H	L	H
0	X	X	X	X	L	H	H	H	L	L	H	H	H
0	X	X	X	L	H	H	H	H	L	H	L	L	H
0	X	X	L	H	H	H	H	H	L	H	L	H	H
0	X	L	H	H	H	H	H	H	L	H	H	L	H
0	L	H	H	H	H	H	H	H	L	H	H	H	H

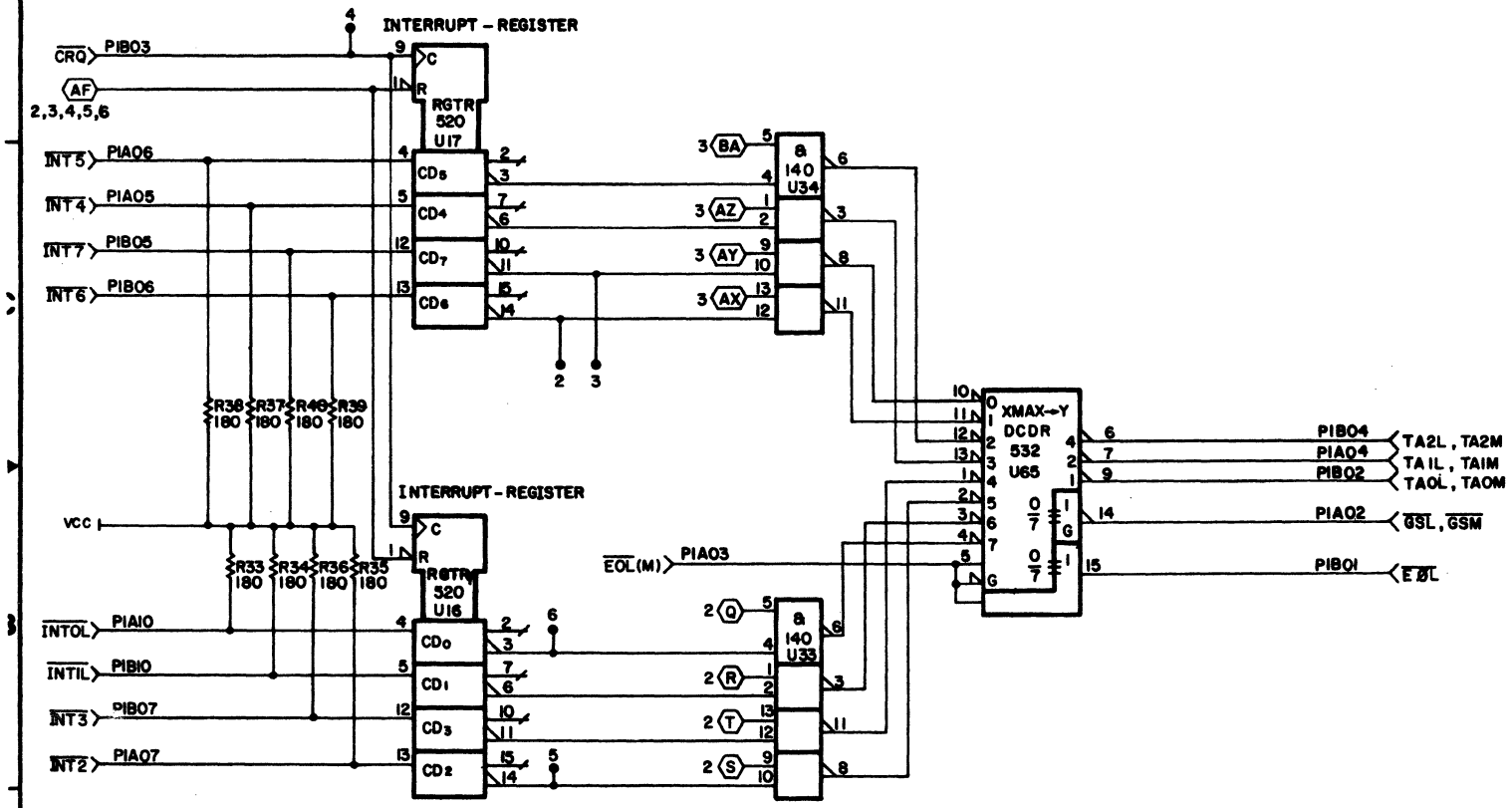
H = Logic High
L = Logic Low
X = irrelevant

The input EI on the LSB is connected to ground while EI on the MSB is connected to EØ on the LSB.

The signal GS from both ALU boards go to the console interface card. GS from the MSB is connected to ITA5 of the LSB.

The outputs TA0, TA1, and TA2 of both ALU boards go to the console interface and are used to produce the trap address bits (ITA2, ITA3, and ITA4) which are connected to the LSB of the ALU (see console interface sheet 7).

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM ALU	CODE IDENT C	DWG NO 89614300	REV A
			SHEET 8	

"Pages 5-206 to 5-210 are unassigned".

DECODER

The Decoder circuits are accommodated on a single 50-PAK printed wiring board. The logic circuit diagram of the unit is given in drawing number 89614900, sheets 1-6.

The Decoder circuits include the instruction register with its decoder and other CPU control circuits. This page lists the functional blocks accommodated on this board. The circuits and signals are described in detail on pages facing the corresponding sheets of the circuit diagram.

MAIN FUNCTIONAL BLOCKS

Designation	Shown on sheet
Instruction Register	2
First Level Decoders	2
Addend Gate Controls	3
Augend Gate Controls	4
Controls for ALU and Addressing	5
Register Clock Controls	6

ØFF - SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN				
		2	3	4	5	6
A	$\overline{DEL}$	D-4	C-3	B-4		
B	DEL	D-3	C-2	B-3	C-1	
D	I7	B-4			B-2	
E	I7	B-3			A-4	
F	RI	B-3	C-2		B-1	
G	$\overline{RI}$	B-4			D-4	
J	$\overline{R2}$	B-4		C-4		
K	R4	B-3	C-2	C-4	B-2	
L	R3	B-3	D-4		C-1	
M	R2	A-3	D-4		D-4	D-2
N	$\overline{R3}$	A-4			D-4	D-2
Q	$\overline{R4}$	A-4	C-4		D-4	D-2
R	T3	C-2	B-4			
S	TI	B-2	B-4	B-2		C-1
T	T4	B-2	B-4			D-3
U	FI=O	B-3			C-1	
V	$\overline{T3}$	D-2		B-3	B-3	D-3
W	FI=A	A-3		C-4		
X	$\overline{TI}$	C-1		B-2		
Y	$\overline{I6}$	B-3	D-3		B-3	B-4
Z	I6	B-3		D-2	A-3	
AA	$\overline{I5}$	C-4		C-3		
AB	I5	B-3	D-3	A-3	A-3	B-4
AD	$\overline{I4}$	C-4	B-3		A-4	
AE	I4	C-4	C-3			
AF	$\overline{I3}$	D-3	B-3		A-4	
AG	I3	D-4	C-4		A-3	
AJ	$\overline{I2}$	C-3			A-4	
AK	I2	C-4				C-3
AL	$\overline{I1}$	C-3			A-4	
AM	I1	C-4				B-3
AN	IO	D-3		D-3		B-4
AQ	IO	C-3			A-3	B-2
AR	I65	B-3		D-2		
AS	I23	B-3			C-2	
AT	F 1=6	B-3	A-4			
AU	F1=7	B-3	A-4			
AV	F1=8	B-2			A-4	
AW	F1=C	A-3		C-4		B-3
AX	F1=D	A-2		C-4	A-4	B-3
AY	F1=F	A-3	A-4			
AZ	F1=D	A-2	D-3			
BA	F=O	C-1	C-4			
BB	F=2	B-1				D-3

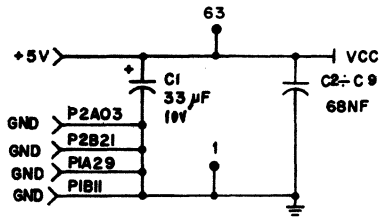
THIS TABLE CØNTINUES ØN SHEET 7

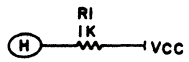
SHEET REVISION STATUS

1	2	3	4	5	6	7
03	03	03	03	03	03	03
04	04	04	04	04	04	04
05	05	04	03	04	04	04
06	05	04	06	04	04	04
07	07	04	07	07	07	04
A	A	A	A	A	A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
03	CK 325	REDRAWN PER CDC STD.	[illegible]	9.12.73	[illegible]	D. WEISS
04	CK421	ADDITION OF TAGS TO FUNCTIONS AND CORRECTION OF DRAWING ERRORS	[illegible]	7.1.74.	[illegible]	D. WEISS
05	CK 474	LOGIC CHANGES FOR PWB REV 09. R2 PLUS LOGIC REV 04 FIT DECODER ASSY 89619200 REV. 01	[illegible]	March, 5 74	[illegible]	D. WEISS
04	CK 637	CORRECTION OF DWG. ERRORS. SH2: U63-9, U41-14, U59-4 U44. SH3: T.P 57 SH5: T.P 50, U21-1 SH6: T.P 47, U3-9, U14-2, U12-6	[illegible]	April, 15 74	[illegible]	[illegible]
06	CK 703	U35-11 AND U35-12 (EXPANDERS FROM U17-6,8) MOVED FROM U35-2,3,4,5,6 TO U35-1,3,8,9,10	[illegible]	May, 23, 74	[illegible]	[illegible]
07	CK785	CORRECT DWG ERRORS	[illegible]	AUG 19 74	[illegible]	[illegible]
A	CK1175	RELEASED CLASS A. FITS ASSY 89834400-A.	M. L.	25.3.75	[illegible]	[illegible]





NØTE: ALL UNMARKED RESISTØRS ARE 0.25 WATT 5%

⚠ ELEMENT IDENTIFIER IS PENDING

AY. 89619200
AW. 89614800
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL N/A

FINISH N/A

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

FIRST USED ON
AB 107-A
AB 108-A

DWN	NEOMY P.	14.11.73
CHKD	AUBREY KAGAN	9.12.73
ENGR	DAVID WEISS	DEC. 9 73
MFG	for Nigel Zeloy	22/4/75
APPR	H. Joseph	5/10/75
QA	H. Salem	22/4/75

TITLE
DETAILED LOGIC DIAGRAM
DECODER

CODE IDENT C

DRAWING NO 89614900

SCALE N/A

HNA: 89626600
89627200

SHEET 1 OF 7

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

(CONTINUED FROM SHEET 1)

OFF - SHEET REFERENCE

OFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION				
		2	3	4	5	6
BC	F=3	B-1				D-3
BD	F=5	C-1	B-2	A-3		
BE	F=6	B-1		A-4		
BF	F=7	B-1		A-4		
BG	F=8	B-1			E-3	
BH	F=B	B-1			B-3	
BJ	F=D	A-1		B-3		
BK	F=E	A-1				B-3
BL	F=F	A-1			B-3	B-3
BM	FI≠1	B-2				C-2
BN	FI≠8	B-2	A-3	C-1		
BP	FI=9	B-2			B-4	D-4
BQ	FI=2		B-4			C-3
BR	FI=0	A-2		D-3		
BS	FI=A	A-3				C-3
BT	FI=E	A-2	B-3	C-3		
BU	F≠0	C-1	A-4	C-3		C-4
BV	F≠9	C-1			C-3	
BW	F≠A	C-1			C-2	
BX	F≠Y	C-1	D-3			
BY	F≠5	C-1	B-3			
BZ	F≠7	B-1		B-3		D-3
CA	F≠C	B-1				D-3
CB	F≠D	A-1	C-3			
CC	F≠F	A-1	B-2	C-3		
CD	RE1F		D-4	C-2		B-4
CE	ITR		D-4	C-2		A-4
CF	$\overline{\text{Ø16}}$		D-3			A-4
CG	RNI21		D-4	D-4	A-3	C-3
CH	ØPE		D-3	A-3		C-3
CJ	CSM		B-4			B-2
CK	FI≠6+7+F		A-4	C-3		
CL	R1,R2,R3,R4		C-3		D-4	C-4
CM	RNI12		C-3	B-4	D-3	
CN	RNI11		A-3	B-4	B-4	D-4
CP	F≠0,FI=2,3		B-4	C-3		D-4
CQ	ØPO		A-3	C-3		
CR	RNI22		B-2	C-3	C-3	C-3
CS	MDSE		D-2	D-4		A-3
CT	$\overline{\text{MDSE}}$		D-1		C-4	
CU			D-1		C-3	
CV	$\overline{\text{CPS}}$		B-1			C-2
CW	ENI2E		B-1	B-2	C-4	
CX	ØDD2		A-2	D-4		
CY	$\overline{\text{ØDD2}}$		A-2	B-3		
CZ	$\overline{\text{ØDD}}$		A-3	D-4		D-4
DA	ØDD		A-2	A-3		C-3

OFF - SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION				
		2	3	4	5	6
DB	ENI20		A-1	B-2	B-4	
DD	RE18		C-4	C-3	D-3	B-3
DE	MDS1			D-3		D-4
DF	FIE23			B-4	B-4	D-1
DH				D-3	A-4	
DG	DELTAUG			A-4	C-4	
DJ	IO+SHI			C-2		B-4
DK				C-1		B-2
DL				C-2	C-4	
DM	SIL			B-1		D-2
DN	II+CNTE2			B-1		B-3
DP				C-1		C-2
DQ	$\overline{\text{CSA}}$			C-1		B-2
DR	$\overline{\text{MD21}}$				C-4	A-4
DS	$\overline{\text{MDT}}$				C-4	A-4
DT	CSQ				C-4	B-2
DU	SHI				A-2	B-4

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM DECODER	CODE IDENT C	DWG NO 89614900	REV A
			SHEET 7	

DECODER (drawing 89614900) sheet 2

INSTRUCTION REGISTER AND FIRST LEVEL DECODERS

Function

This circuit consists of the instruction register and the first level of decoding logic.

Inputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
MDEL	H	P1B20	Δ field zero from memory	2	D4
IRCK	H	P1A21	Instruction Register Clock		D4
MX00	H	P1B16	Data read from memory		C4
MX01	H	P1A16			C4
MX02	H	P1A18			D4
MX03	H	P1A20			D4
MX04	H	P2B19			C4
MX05	H	P2B17			B4
MX06	H	P2A19			C4
MX07	H	P2A18			B4
MX08	H	P1A25			B4
MX09	H	P1A23			B4
MX10	H	P1B14			A4
MX11	H	P1B15			A4
MX12	H	P2B05			C2
MX13	H	P2A08			C2
MX14	H	P2B08			C2
MX15	H	P2A05			C2
CLRIR	H	P1A31	Clear Instruction Register	2	A4

NOTE: An alternative notation, emphasizing the significance of the bits of data read from memory employs the letters L (less significant) and M (more significant). Thus the following pairs are identical:
MX00 - MX0L, MX07 - MX7L, MX08 - MX0M, MX15 - MX7M.

Outputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
R1	H	P1B27		2	A3
R2	H	P1A28	F1 field of instruction		A3
R3	H	P1A24	register		A3
R4	H	P1B28			A3
I0	H	P1B13			D3
I1	H	P1B05			D3
I2	H	P1B10			D3
I3	H	P1A10	Instruction Register bits		C3
I4	H	P2B26			C3
I5	H	P2B24			C3
I6	H	P2B23			C3
$\overline{I7}$	L	P2A23			C3
$\overline{DEL}$	L	P1A14	Δ field zero (stored) see text		D3
DEL2	H	P1A15			D2
T1	H	P2A06			C1
T2	H	P2B09	F - field outputs		D1
T3	H	P2A09			D1
T4	H	P2B06			D1
$\overline{01}$	L	P1B30	F - field content is 1		B1
$\overline{02}$	L	P1B31	F - field content is 2		B1
$\overline{03}$	L	P2B01	F - field content is 3		B1
$\overline{0D}$	L	P2A01	F - field content is D_{16}		A1
I65	H	P2A22	16·15·	2	B2

DECODER (Drawing 89614900) sheet 2, cont'd.

Description

The instruction register is a 16 bit register. Its input is the data read from memory through the memory control board (signals MX00 through MX15). The register is clocked by the IRCK from the timing board and cleared by CLRIR from the console interface.

The register itself uses two types of components. The F1 field of the instruction register are high speed dual D-type flip-flops (U45, U46). These are used because the F1 field must be decoded early in the execution of the instruction. The F field and Δ field are stored in quad D-type flip-flops (U39, U41, U47) like those used in the ALU registers. The outputs of the F field and the F1 field are decoded in two four-to-sixteen decoders (U57, U58) each having sixteen active low outputs, one for each possible input code. Four outputs from F-field decoder ($\overline{01}$, $\overline{02}$, $\overline{03}$, $\overline{0D}$) which are active when F = 1, F = 2, F = 3, and F = D respectively, (hexadecimal notation) are outputs of the Decoder assembly.

The DEL flip-flop, (U60/8), stores the signal MDEL from the memory control assembly This signal indicates when the delta (Δ) field is equal to zero. The flip-flop is clocked by IRCK and cleared by CLRIR. The output of this flip-flop is an output of the assembly, through an inverter, as $\overline{DEL}$ ($\Delta \neq 0$).

The outputs of the instruction register fields are summarized in the following table:

FIELD	OUTPUTS	BITS
F	T1, T2, T3, T4	12 ÷ 15
F1	R1, R2, R3, R4	18 ÷ 11
Δ	10 through 17	60 ÷ 7

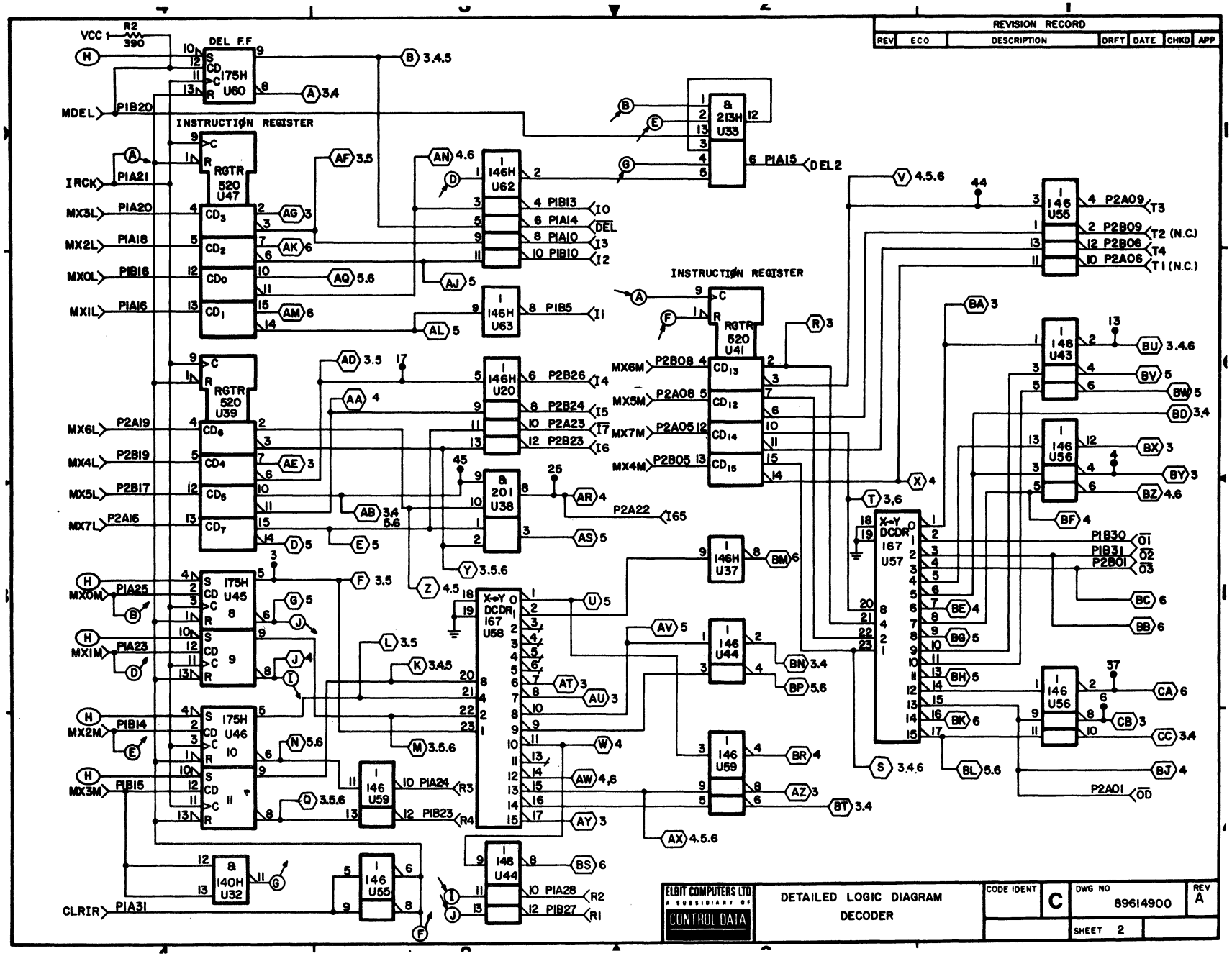
The signal DEL2 is produced by decoding MX data lines. Its equation is:

$$DEL2 = MDEL \cdot \overline{MX11} \cdot MX10 \cdot \overline{MX09} \cdot MX08 = (F1=5) \cdot (\Delta=0)$$

It is used by the interrupt logic to sense the inhibit interrupt instruction and prevent an enter interrupt sequence under certain conditions (see Console Interface sheet 5).

The signal $123 = 17 \cdot \overline{16}$ is produced by U38/3

The signal $165 = 16 \cdot 15$ is produced by U38/8. It is used on the I/O Interface.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
DETAILED LOGIC DIAGRAM
DECODER
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
CODE IDENT C
DWG NO 89614900
REV A
SHEET 2
INSTRUCTION REGISTER
DEL F.F
VCC
R2
390
MDEL
P1B20
IRCK
P1A21
MX3L
P1A20
MX2L
P1A18
MX0L
P1B16
MX1L
P1A16
MX6L
P2A19
MX4L
P2B19
MX5L
P2B17
MX7L
P2A16
MX0M
P1A25
MX1M
P1A23
MX2M
P1B14
MX3M
P1B15
CLRIR
P1A31
P1A15 DEL2
P1B13 I0
P1A14 DEL
P1A10 I3
P1B10 I2
P1B5 I1
P2B26 I4
P2B24 I5
P2A23 I7
P2B23 I6
P2A22 I65
P1B30 O1
P1B31 O2
P2B01 O3
P2A09 T3
P2B09 T2 (N.C.)
P2B06 T4
P2A06 T1 (N.C.)
P2A01 OD
P1A24 R3
P1B23 R4
P1A28 R2
P1B27 R1
P2B08
P2A08
P2A05
P2B05
MX6M
MX5M
MX7M
MX4M

DECODER (drawing 89614900) sheet 3

ADDEND GATE CONTROLS

Function

This circuit contains the logic gates which generate the signals to control the addend gates of the ALU (refer to ALU, sheets 2, 3).

Inputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{\text{ØPE}}$	L	P2B28		3	D4
RE1F	H	P2B15			D4
ITR	H	P2A15			D4
$\overline{\text{RN121}}$	L	P2A29			D4
$\overline{\text{RN112}}$	L	P2B30			C4
N41	H	P2B14			C4
NO	H	P2A14			C4
$\overline{\text{RE18}}$	L	P2A27			C4
$\overline{\text{CSM}}$	L	P2A04			B4
RP	H	P1A08			B4
$\overline{\text{RN122}}$	L	P1A05			B4
$\overline{\text{RN111}}$	L	P1B08			A4
$\overline{\text{ØPO}}$	L	P1A06			A4
$\overline{\text{Ø16}}$	L	P2B16			D3
MDSE	H	P1B01			D2
$\overline{\text{ADR}}$	L	P1B07			A2
ØDD2	H	P1A02			A2
$\overline{\text{ØDD}}$	L	P1B09			A3
$\overline{\text{CSP}}$	L	P1B03			B1
$\overline{\text{EN12E}}$	L	P1B18			B1
$\overline{\text{EN120}}$	L	P1A07		3	A1

Outputs (cont'd.)

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
MTADD	H	P1A17	Addend gate gating signals	3	C3
QTADD	H	P2B22		3	D1
PTADD	H	P1A19		3	B1
XTADD	H	P1A09		3	A1

Description

The logic gates receive signals from the decoder, (logic shown on sheet 2) as well as timing signals from the Timing assembly. The resulting signals, QTADD, PTADD, XTADD and MTADD, determine which register, if any, is gated through the addend gates during each CPU cycle.

The equations of these signals are as follows:

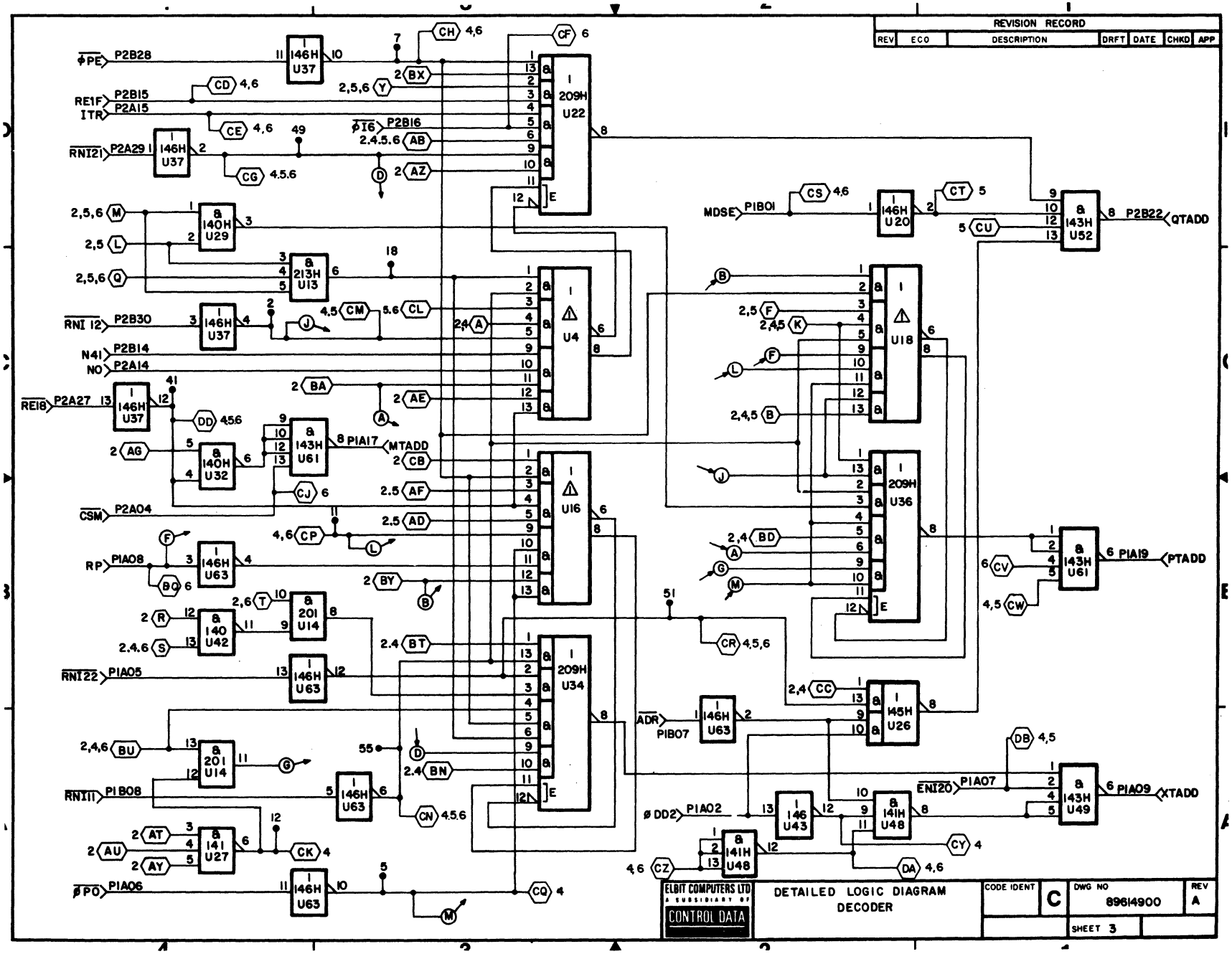
$$\begin{aligned}
XTADD = {} & ENI2 \cdot \emptyset DD + ADR \cdot \emptyset DD \cdot \overline{\emptyset DD2} \\
& + \emptyset P \cdot \emptyset DD \cdot [(F=0) \cdot (FI=2,3) \cdot \overline{RP} + (F=5)] \\
& + \emptyset P \cdot EVEN \cdot [(F=D) + (F=0) \cdot (FI=6,7)] \\
& + RNI \cdot EVEN \cdot (F=0) \cdot (FI=8) \cdot \overline{I5} \cdot \overline{I4} \\
& + RNI \cdot EVEN \cdot (F=0) \cdot (FI=9) \\
& + RNI \cdot EVEN \cdot (F=8,9,A,B,C,E) \\
& + RNI \cdot \emptyset DD \cdot (F=0) \cdot (FI=E)
\end{aligned}$$

$$\begin{aligned}
PTADD = {} & CSP + ENI2 \cdot EVEN + \emptyset P \cdot EVEN \ (F=5) \\
& + \emptyset P \cdot \emptyset DD \cdot [(F=0) \cdot (FI=2,3) \cdot RP + (F \neq 0) \cdot (F \neq 5) + (F=0) \cdot (FI=6,7,F)] \\
& + RNI \cdot \emptyset DD \cdot (F \neq 0) \cdot [DEL + R4] \\
& + RNI \cdot \emptyset DD \cdot (F=0) \cdot (\overline{R2 \cdot R3} + R1 \cdot R4)
\end{aligned}$$

$$
\begin{aligned}
QTADD = {} & CSQ + MDS \cdot EVEN + MD21 + MD1 + ADR \cdot \emptyset DD2 \\
& + (F \neq 0) \cdot N41 \cdot N0 + ITR \cdot \overline{\emptyset 16} \cdot I5 \\
& + RNI \cdot EVEN \cdot (F=0) \cdot (F1=F) \cdot \overline{I6} \\
& + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot I4 \\
& + \emptyset P \cdot EVEN \cdot (F=4) \\
& + RNI \cdot EVEN \cdot (F=F) \\
& + RNI \cdot EVEN \cdot (F=0) \cdot (F1=D) \\
& + RNI \cdot \emptyset DD \cdot (F \neq 0) \cdot (F1=2) \cdot \overline{DEL} \\
& + RNI \cdot \emptyset DD \cdot (F=0) \cdot (F1 = 6,7)
\end{aligned}
$$

$$MTADD = CSM + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot I3$$

The signal $\overline{\emptyset 16} = EVEN \cdot \overline{I6}$ (see Timing, sheet 2).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REV ECO DESCRIPTION DRFT DATE CHKD APP
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
DECODER
CODE IDENT C
DWG NO 89614900
REV A
SHEET 3

DECODER (drawing 89614900) sheet 4

AUGEND GATE CONTROLS

Function

This circuit contains the logic gates which generate the control signals for the augend gates of the ALU (see ALU sheets 4,5).

Inputs

SIGNAL	ACTIVE	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
ENI	H	P1B02		4	D4
MDS1	H	P1A13			D4
$\overline{FS}$	L	P1A03			C4
$\overline{DELTAUG}$	L	P2B10			A4
$\overline{CSX}$	L	P2A21			A4
PRY	H	P1B06			B3
MDS2	H	P2B04			A3
$\overline{IRJ}$	L	P1B17			C3
$\overline{E15}$	L	P2B18			C2
$\overline{CSA}$	L	P2B20			C2
QSX	H	P2B02			B2
$\overline{AO}$	H	P2A02			B2
$\overline{CNTE2}$	L	P2A30		4	B2

Outputs

XTAUGM		P2A20		4	A4
XTAUGL		P2B31			A4
ATAUG		P2A24			C1
SIL		P1B19		4	B1

DECODER (Drawing 89614900) sheet 4, cont'd.

Description

The logic gates combine the decoded instruction with timing signals to produce the control signals XTAUGM, XTAUGL, ATAUG, and SIL. The equations of these signals are as follows:

$$\begin{aligned}
\text{XTAUGM} &= \text{CSX} + \text{ENI}\cdot\text{ØDD2} + \text{MDS1}\cdot\overline{\text{ØDD}} \\
&\quad + \text{MDS}\cdot\text{EVEN}\ (\overline{\text{T1}\cdot\text{QSX} + \text{T1}\cdot\text{A0}}) \\
&\quad + \text{ØP}\cdot\text{ØDD}\cdot(\text{F=0})\cdot(\text{F1=E}) \\
&\quad + \text{RNI}\cdot\text{EVEN}\cdot(\text{F=0})\cdot(\text{F1=8})\cdot\overline{\text{I5}} \\
&\quad + \text{RNI}\cdot\text{EVEN}\cdot(\text{F=F}) \\
&\quad + \text{RNI}\cdot\text{EVEN}\cdot(\text{F=0})\cdot(\text{F1=0,A,C,D})
\end{aligned}$$

$$\begin{aligned}
\text{XTAUGL} &= \text{XTAUGM} + \text{DELTAUG} \\
&\quad + \text{RNI}\cdot\text{ØDD}\cdot(\text{F}\neq\text{0})\cdot\overline{\text{DEL}} \\
&\quad + \text{RNI}\cdot\text{ØDD}\cdot(\text{F=0})\cdot(\text{F1=2,3})
\end{aligned}$$

$$\begin{aligned}
\text{ATAUG} &= \text{CSA} + \text{MDS2}\cdot\text{ØDD} + \text{ITR}\cdot\overline{\text{EI5}}\cdot\text{I6} \\
&\quad + \text{ØP}\cdot\text{EVEN}\cdot(\text{F=6,7}) \\
&\quad + \text{RNI}\cdot\text{EVEN}\cdot(\text{F=0})\cdot(\text{F1=F})\cdot[\text{I5}\cdot\text{I6}\cdot(\overline{\text{K0}} + \text{I0}) + \text{I6}\cdot(\overline{\text{I0}}+\text{SHI})] \\
&\quad + \text{RNI}\cdot\text{EVEN}\cdot(\text{F=0})\cdot(\text{F1=8})\cdot\text{I5} \\
&\quad + \text{RNI}\cdot\text{EVEN}\cdot\overline{\text{T3}} \\
&\quad + \text{RNI}\cdot\text{EVEN}\cdot(\text{F=0})\cdot(\text{F1=9})
\end{aligned}$$

where $\text{K0} = \overline{\text{I1}\cdot\text{I2}\cdot\text{I3}\cdot\text{I4}}$

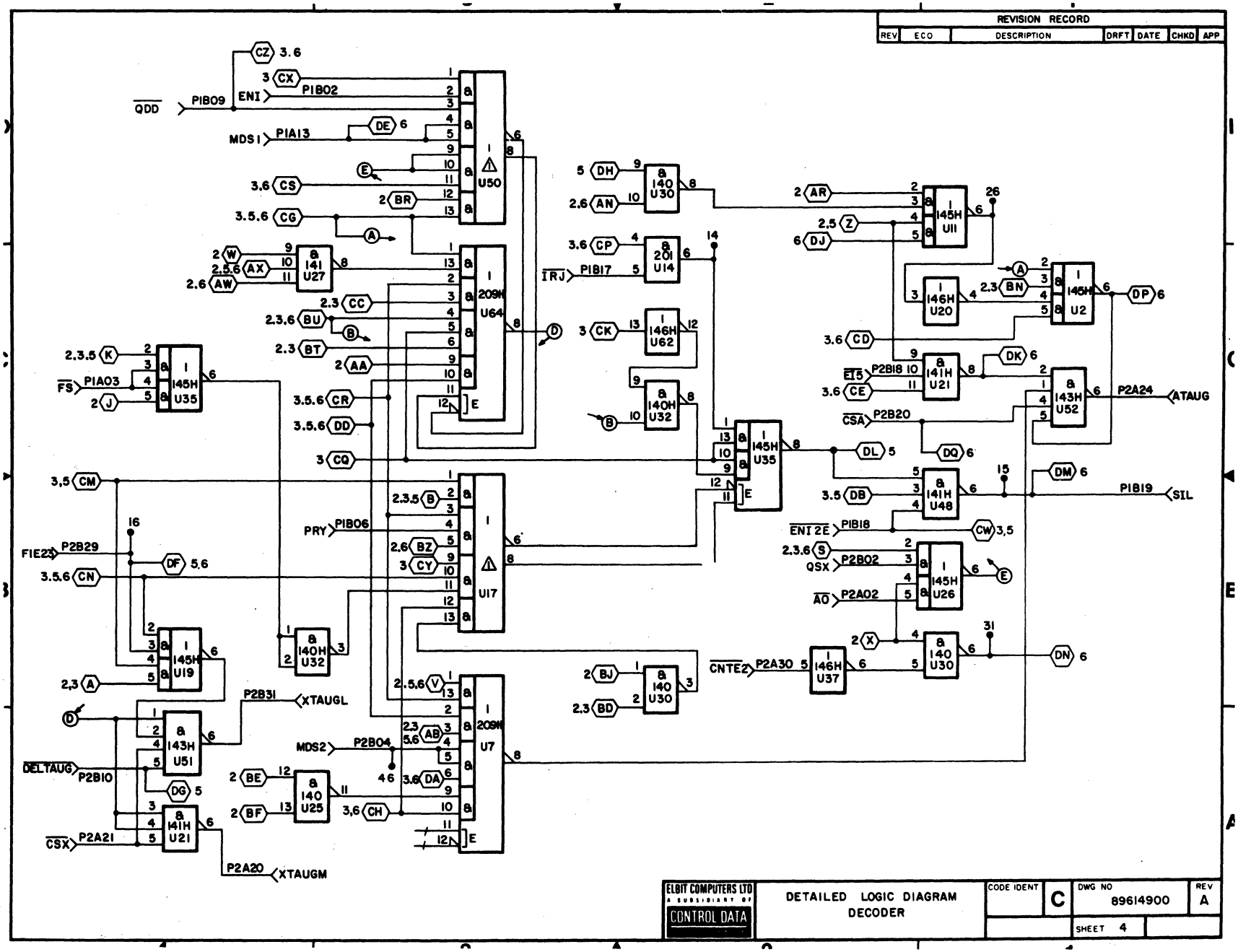
$\text{SHI} = \text{K0}\cdot(\overline{\text{I0}+\text{I5}+\text{I6}})$ - see Decoders

$\overline{\text{EI5}} = \overline{\text{EVEN}} + \text{I5}$ - see Timing 2.

$$\begin{aligned}
\text{SIL} &= \text{ENI2} + \text{ØP}\cdot\text{EVEN}\cdot(\text{F=5,D}) \\
&\quad + \text{ØP}\cdot\text{ØDD}\cdot[\text{F}\neq\text{0}) + (\text{F1=6,7,F}) + (\text{F=0})\cdot(\text{F1=2,3})\cdot\overline{\text{IRJ}}] \\
&\quad + \text{RNI}\cdot\text{EVEN}\cdot(\text{F=7})\cdot\text{PRY} \\
&\quad + \text{RNI}\cdot\text{ØDD}\cdot(\text{F}\neq\text{0})\cdot\text{DEL} \\
&\quad + \text{RNI}\cdot\text{ØDD}\cdot(\text{F=0})\cdot\text{ØDD2}\cdot\overline{\text{FS}}\cdot(\text{R4}+\overline{\text{R2}})
\end{aligned}$$

where IRJ (Internal Reject) comes from the I/O interface assembly.

PRY (Parity) comes from the Console Interface assembly.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REV ECO DESCRIPTION DRFT DATE CHKD APP
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ENI
PIB02
MDS1
PIA13
MDS2
P2B04
DELTAUG
P2B10
CSX
P2A21
P2A20
XTAUGM
P2B31
XTAUGL
FIE23
P2B29
PRY
PIB06
IRJ
PIB17
CNTE2
P2A30
QSX
P2B02
AO
P2A02
CSA
P2B20
ET5
P2B18
ENI2E
PIB18
P2A24
ATAUG
PIB19
SIL
U50
U64
U17
U7
U35
U19
U51
U21
U27
U25
U32
U14
U62
U30
U11
U20
U2
U52
U48
U26
U37
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SHEET 4

DECODER (drawing 89614900) sheet 5

CONTROLS FOR ALU AND ADDRESSING

Function

This circuit generates the following signals:

- ALU control signals S0, S1, S2, S3 and M (refer to ALU circuits, sheets 6,7).
- Counter preset signals AD1, AD2 used on the Timing assembly to preset the counter at the beginning of the effective address calculation (refer to timing circuit, sheet 3).
- The signal SHI.

Inputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{W9A}$	L	P2B13		5	D4
GØCS	H	P2B25			D4
$\overline{MD2I}$	L	P2B12			C4
$\overline{MD1}$	L	P2A11			C4
$\overline{CSQ}$	L	P2A10			C4
$\overline{ADY}$	L	P2B07		5	B3

Outputs

M	H	P2A07	ALU Controls	5	B3
S0	H	P2A12			D2
S1	H	P2A18			C2
S2	H	P2A17			C2
S3	H	P2A13			D2
I23	H	P2A25			C2
SHI	H	P2B11	$\overline{I1}\cdot\overline{I2}\cdot\overline{I3}\cdot\overline{I4}\cdot(\overline{I0}+\overline{I5}+\overline{I6})$		A2
AD1	H	P1B24	Counter preset signals		B1
AD2	H	P1A26		5	A1

Description

The signal SHI is used both on the decoder and I/O interface boards. Its equation is:

$$SHI = K0 \cdot (\overline{I0}+\overline{I5}+\overline{I6})$$

where $$K0 = \overline{I1} \cdot \overline{I2} \cdot \overline{I3} \cdot \overline{I4}$$

This signal is valid during shift instructions. Its significance is as follows:

Signal K0, and therefore SHI, is active when the instruction calls for a shift of zero or a register shift of one place. In this case the entire shift operation is carried out in the RNI state and the ITR state is not used.

The equations for S0, S1, S2, S3, M, AD1 and AD2 are as follows:

$$\begin{aligned} S0 = {} & \overline{W9A} + CSQ + MD21 + MD1 + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot I6 \\ & + RNI \cdot EVEN \cdot (F=0) \cdot [(F1 \neq 8) + \overline{I7}] \\ & + RNI \cdot EVEN \cdot [(F=8,B) + T3] \end{aligned}$$

$$\begin{aligned} S1 = {} & \overline{G\emptyset CS} + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot I7 \cdot \overline{I6} \\ & + RNI \cdot EVEN \cdot (F=9,A) \end{aligned}$$

$$\begin{aligned} S2 = {} & \overline{G\emptyset CS} + CSQ + MD21 + MD1 \\ & + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot I7 \cdot \overline{I6} \\ & + RNI \cdot EVEN \cdot (F=9,A) \end{aligned}$$

$$\begin{aligned} S3 = {} & \overline{W9A} + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot I7 \cdot \overline{I6} \\ & + RNI \cdot EVEN \cdot [(F=8,A,B) + T3] \\ & + RNI \cdot EVEN \cdot (F=0) \cdot [(F1 \neq 8) + \overline{I7}] \end{aligned}$$

$$\begin{aligned} \overline{M} = {} & ADY + SIL + DELTAUG + MDSE \\ & + RNI \cdot \emptyset DD \cdot (F=0) \cdot (F1=2,3) \\ & + RNI \cdot \emptyset DD \cdot (F \neq 0) \cdot [(F1=2) + R4] \\ & + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot \overline{I6} \cdot \overline{I7} \\ & + RNI \cdot EVEN \cdot (F=0) \cdot (F1=9,D) \\ & + RNI \cdot EVEN \cdot (F=8,9,F) \end{aligned}$$

where $\overline{ADY}$ is produced on the Timing Card - see Timing sheet 3.

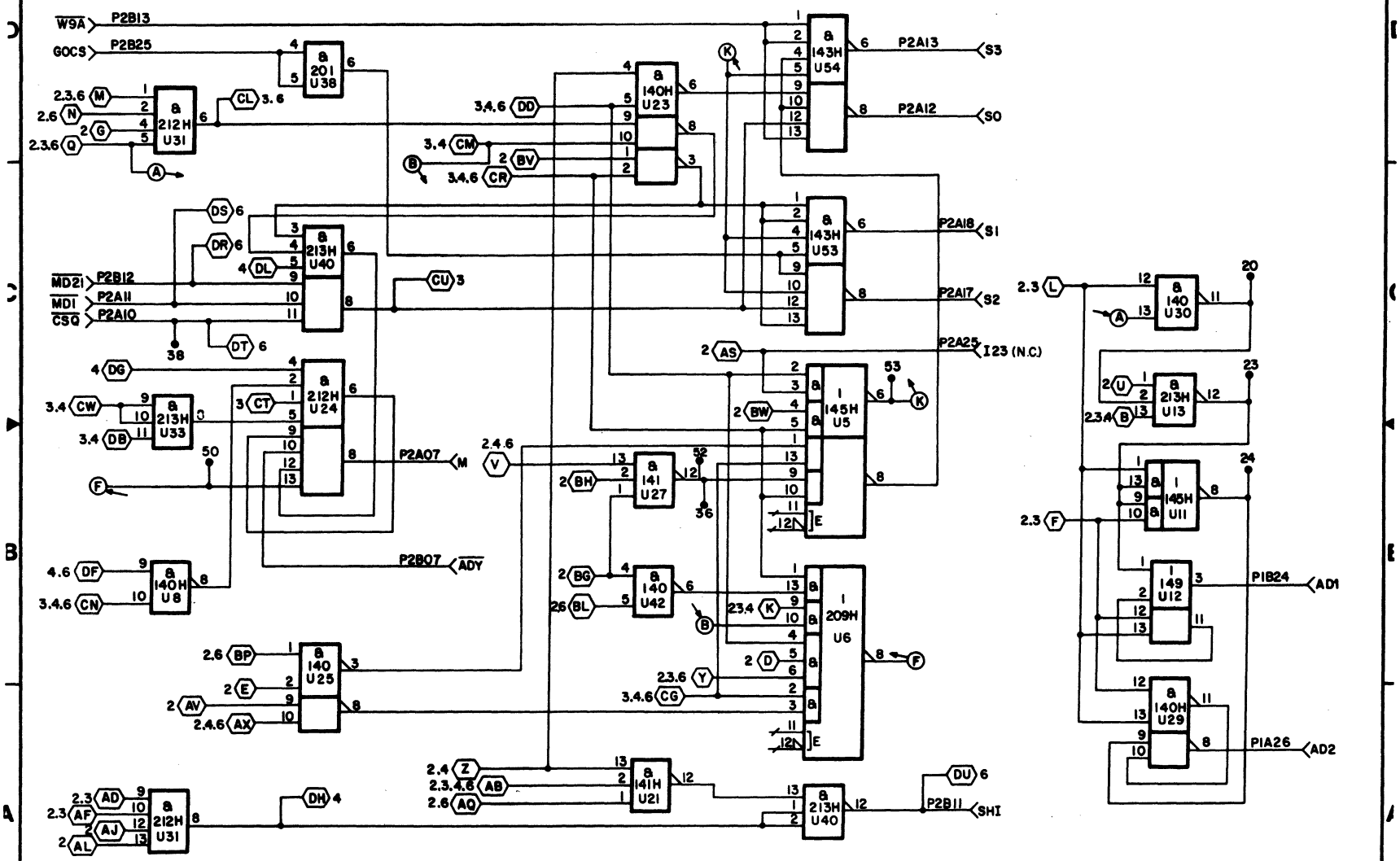
$\overline{W9A}$ is produced on the Timing Card - see Timing sheet 5.

DECODER (Drawing 89614900) sheet 5, cont'd.

$$AD1 = R1 \oplus R3 \oplus [(F1 \neq 0) \cdot (R4 \cdot \overline{R3}) \cdot DEL]$$

$$AD2 = R1 \cdot R3 + R1 \cdot R3 \cdot [(F1 \neq 0) \cdot (R4 \cdot \overline{R3}) \cdot DEL]$$

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



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			SHEET 5	

DECODER (drawing 89614900) sheet 6

REGISTER CLOCK CONTROLS

Function

This circuit generates the register clock controls WP, WA, WQ, WM, WXL1; the bit bucket signal (BB) and the signal F1E23.

The WP, WA, WQ, WM signals are used on the Timing circuit to generate clock pulses for their respective registers (refer to timing circuit, sheet 3). The WXL1 signal is part of the condition for writing into the X register. It is transmitted to the I/O interface board where it generates the signals WXL, WXM.

Inputs

SIGNAL	ACTIVE	CONNECTOR/ PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{\text{PEF}}$	L	P1A27		6	D4
DBB	H	P1B21			D4
BBCK	H	P1A22			D4
WRQ	H	P1A11			D4
$\overline{\text{WE}}$	L	P1B12			D4
BX15	H	P2A28			C4
MDSØ	H	P2B27			B4
Q15	H	P1B28			A4
CRQ	H	P1B26			C2
$\overline{\text{JRNI}}$	L	P1A04			C2
X15	H	P1B22		6	C2

Outputs

$\overline{\text{WXLT}}$	L	P1A12		6	C3
BB	H	P1B25			D1
WP	H	P1B04			C1
WA	H	P2A26			B1
WM	H	P2B03			B1
WQ	H	P1B29			B1
F1E23	H	P2B29	(F1=2)+(F1=3)	6	D1

Description

The BB flip-flop (U60/5) stores DBB from the console interface. This signal is used during multiply and divide instructions (see Console Interface, sheet 7). The flip-flop is clocked by the signal BBCK from the Timing assembly. The output is used on the Decoder assembly and is also transmitted to the I/O interface.

The signal F1E23 = (F1 = 2) + (F1 = 3) is produced by the AND gate U13/8. It is used on this assembly and also transmitted to the I/O interface.

The equations of the register clock control are as follows:

$$WP = JRNI + CSP + CRQ \cdot SIL + RNI \cdot \emptyset DD \cdot (F=0) \cdot (F1=1)$$

where

CRQ is generated in the timing circuit and is active during the first part of a CPU memory cycle. This is an ØDD cycle in which data is sent from the CPU to memory. SIL is active whenever the P register is changed (incremented or decremented) by one.

$$WM = CSM + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot I0$$

$$\begin{aligned} WQ = {} & CSQ + MD1 \cdot BX15 + MD21 \cdot Q15 \\ & + MDS \cdot EVEN \cdot (\overline{CNTE2} + T1) \\ & + ITR \cdot \overline{016} \cdot I5 \\ & + RNI \cdot EVEN \cdot (F=0) \cdot (F1=C,D) \\ & + RNI \cdot EVEN \cdot (F=E,F) \\ & + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot I1 \\ & + RNI \cdot EVEN \cdot (F=0) \cdot (F1=F) \cdot I5 \cdot \overline{I6} \cdot (SHI + \overline{I0}) \end{aligned}$$

$$\begin{aligned} WA = {} & CSA + MDS \cdot \emptyset DD \cdot (\overline{CNTE2} + T1) + MDS1 \cdot \emptyset DD \cdot BX15 \\ & + ITR \cdot \overline{E15} \cdot I6 + \emptyset P \cdot EVEN \cdot (F=0) \cdot (F1=2) \\ & + RNI \cdot EVEN \cdot (F=0) \cdot (F1=F) \cdot [I5 \cdot I6 \cdot (\overline{K0} + I0) + I6 \cdot (\overline{I0} + SHI)] \\ & + RNI \cdot EVEN \cdot (F=0) \cdot (F1=8) \cdot I2 \\ & + RNI \cdot EVEN \cdot (F=0) \cdot (F1 = 9,A) \\ & + RNI \cdot EVEN \cdot (F \neq 0) \cdot [T4 \cdot T3 + (F=C) + (F=7) \cdot PEF + (F=2,3) \cdot BB] \end{aligned}$$

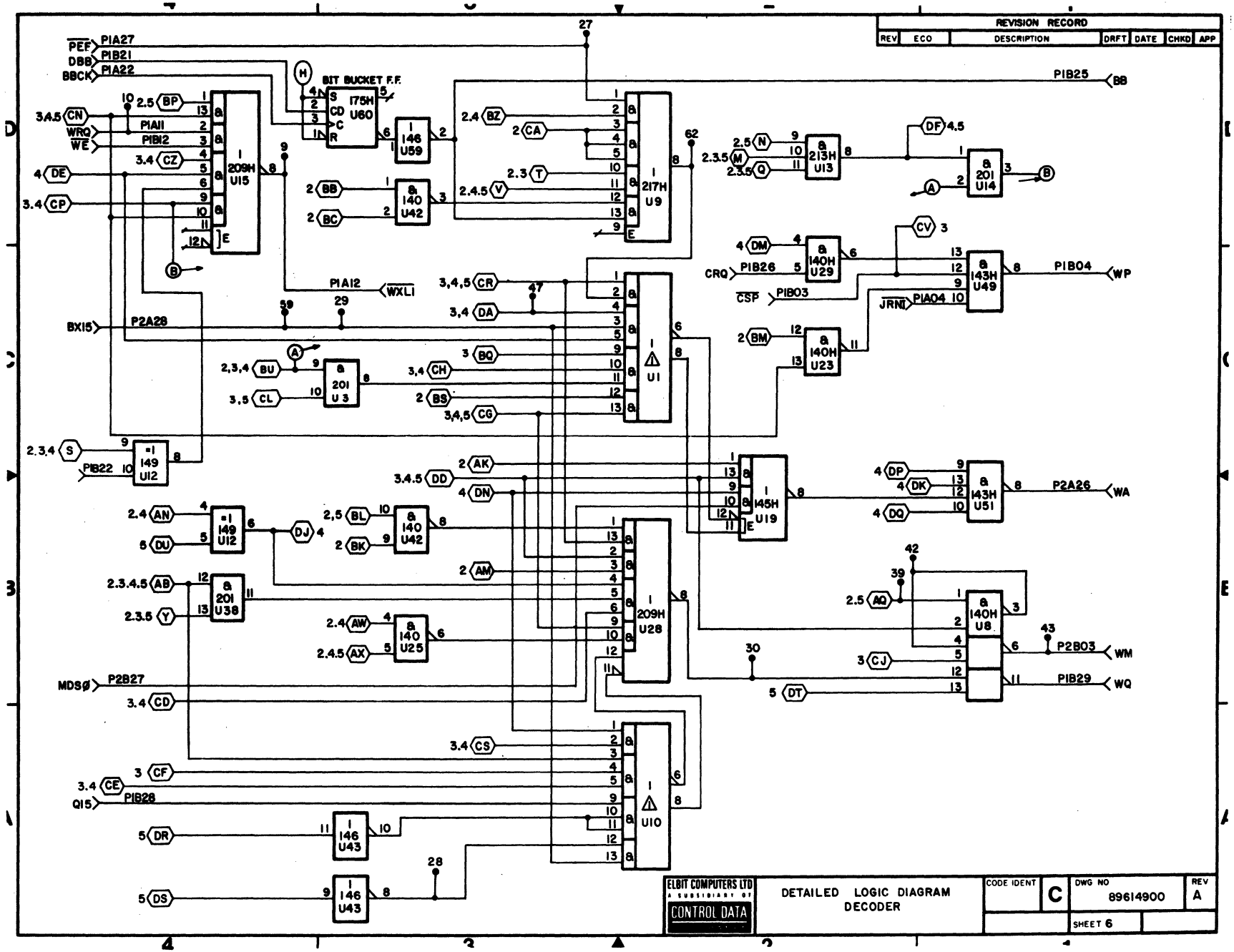
$$WXL1 = WRQ \cdot \overline{WE} + MDS1 \cdot \overline{\emptyset DD} \cdot (X15 + T1) + RN1 \cdot \emptyset DD \cdot (F=0) \cdot (F1=2,3,8)$$

where

- WRQ is produced on the Console Interface and is high during the second pass (EVEN) of each CPU memory cycle

- $\overline{WE}$ is produced on the I/O interface and is high during a CPU memory read cycle.

Thus the term $WRQ \cdot \overline{WE}$ clocks data read from the memory into the X register.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DBB PIB21
BBCK PIA22
BIT BUCKET F.F.
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209H U15
146 U59
140 U42
217H U9
213H U13
201 U14
140H U29
143H U49
140H U23
201 U3
U1
149 U12
145H U19
143H U51
209H U28
201 U38
140H U8
146 U43
U10
PIB25 BB
PIA12 WXLI
BXI5 P2A28
PIB04 WP
P2A26 WA
P2B03 WM
PIB29 WQ
MDSØ P2B27
Q15 PIB28
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SHEET 6

"Pages 5-236 to 5-240 are unassigned."

TIMING

The Timing circuits are accommodated on a single 50-PAK printed wiring board. The logic circuit diagram is given in drawing number 89617000, sheets 1-6.

The Timing circuit provides the main timing control signals for the CPU. This page shows typical timing sequences, gives state equations and lists the functional blocks making up the Timing assembly. The circuit and signals are described in detail on pages facing the corresponding sheets of the circuit diagram.

MAIN FUNCTIONAL BLOCKS

Designation	Shown on Sheet
Clock (oscillator and phase generator)	2
Even, odd flip-flops	
Counter	3
Interrupt timing, Y register control logic	4
Main sequence flip-flops	5
Auxiliary sequence flip-flops	6
Register clocks	6

TIMING (drawing 89617000)

STATE EQUATIONS

The following signals are produced by J-K flip-flops clocked by the signal JKCK.

EVEN: JEVEN = ØDD2 + $\overline{\text{EXT}}$

KEVEN = 1

CLEARED BY MPC

ØDD : JØDD = 1

KØDD = ØDD2 + $\overline{\text{EXT}}$

CLEARED BY SGI AFTER DELAY OF 2 CLOCK PULSES

ØDD2: JØDD2 = ØDD · EXT

KØDD2 = ØDD2

CLEARED BY MPC

RNI : JRNI = ØP · ØDD + EAD·(F=1) + ENI20

KRNI = RNI·ØDD·(F=0)·[(FI = 2,3,6,7) + ØDD2·(FI = E)
+ $\overline{\text{SHI}}$ · (FI = F)]
+ RNI·ØDD·(F ≠ 0) [(F ≠ 1) + $\overline{\text{SHADD}}$ + ENI3] ·$\overline{\text{KENII}}$

PRESET BY MPC

TIMING (drawing 89617000)

ADR: $JADR = RNI \cdot \emptyset DD\ (F \neq 0) \cdot \overline{SHADR}$

$KADR = \emptyset DD \cdot (COUNTER = 0) \cdot \overline{[(F1 = 4,6,C,E) \cdot 32KW \cdot X_{15}]}$

CLEARED BY (MPC + ENI)

ØP : $J\emptyset P = RNI \cdot \emptyset DD \cdot (F = 0) \cdot [(F1 = 2,3) + \emptyset DD2 \cdot (F1 = E)]$
$+ EAD \cdot (F \neq 1) \cdot (F \neq D) + \emptyset P2 \cdot \emptyset DD + KITR + MDI$

$K\emptyset P = \emptyset P \cdot \emptyset DD + \emptyset P \cdot EVEN \cdot (F = 2,3)$

CLEARED BY (MPC + ENI)

ØP2: $J\emptyset P2 = RNI \cdot \emptyset DD\ (F = 0)\ (F1 = 6,7) + EAD \cdot (F=D)$

$K\emptyset P2 = \emptyset DD$

CLEARED BY (MPC + ENI)

ITR: $JITR = RNI \cdot \emptyset DD \cdot (F = 0) \cdot (F1 = F) \cdot \overline{SHI}$

$KITR = ITR \cdot EVEN \cdot [(COUNTER=2) \cdot SHI + COUNTER \leq 1]$

CLEARED BY MPC

ENI : $JENI = [(RNI \cdot \overline{EPS} + INDIND) \cdot (GSM + GSL) \cdot WRQ \cdot EINT] \cdot$
$\cdot \overline{[RNI \cdot MX17A \cdot MX17 \cdot PRFA]} \cdot$
$\cdot \overline{[RNI \cdot MX17A \cdot MX17 \cdot DFEO \cdot DEL2]}$
$\cdot \overline{[RNI \cdot PRTSW \cdot DFEO \cdot DEL2]}$

KENI1: $ENI2 \cdot \emptyset DD + ENI \cdot RNI \cdot \overline{GSL} \cdot \overline{GSM}$

CLEARED BY MPC

TIMING (drawing 89617000)

EN12: JEN12 = EN1 • ØDD2

KEN12 = EN12•ØDD

CLEARED BY MPC

MD21: NOTE: - This signal is produced with simple logic gates

MD21 = ØDD • (F = 2,3) • (COUNTER = 21)

MDS1: JMDS1 = MD21

KMDS1 = MDS1 • ØDD

CLEARED BY MPC

MDS: JMDS = MDS1 • ØDD

KMDS = ØDD • (COUNTER = 2)

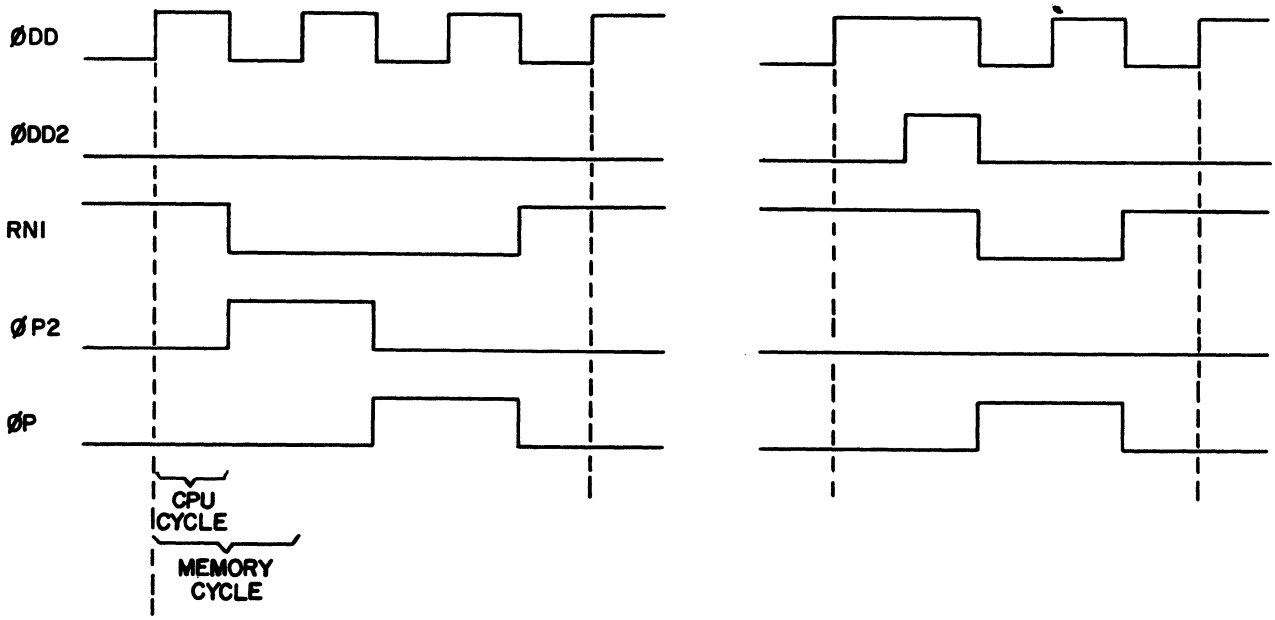
CLEARED BY MPC

MD1 : MD1 = $\overline{\text{ADR}}$ • (F = 2,3) • (COUNTER = 1)

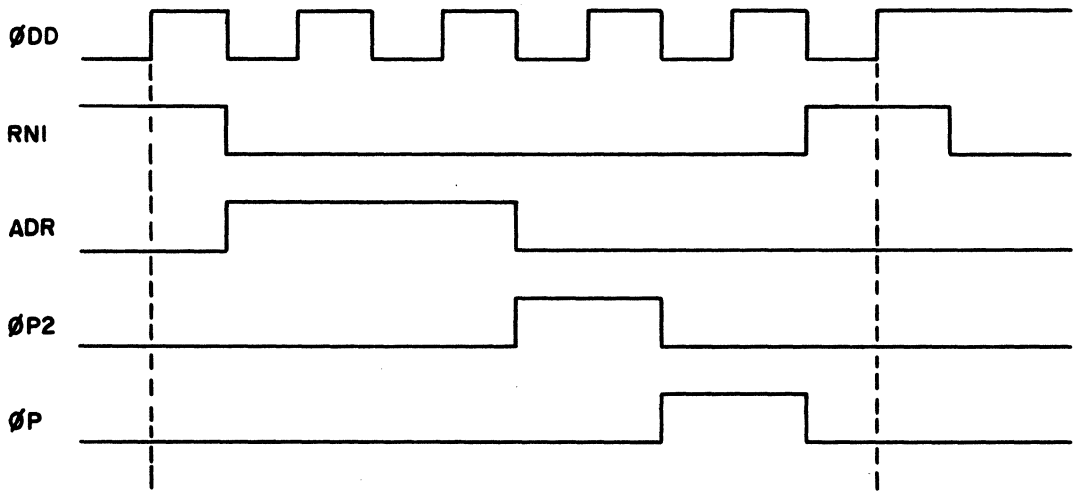
TIMING

TYPICAL TIMING SEQUENCES (drawing 89617000)

Register Reference Instructions:

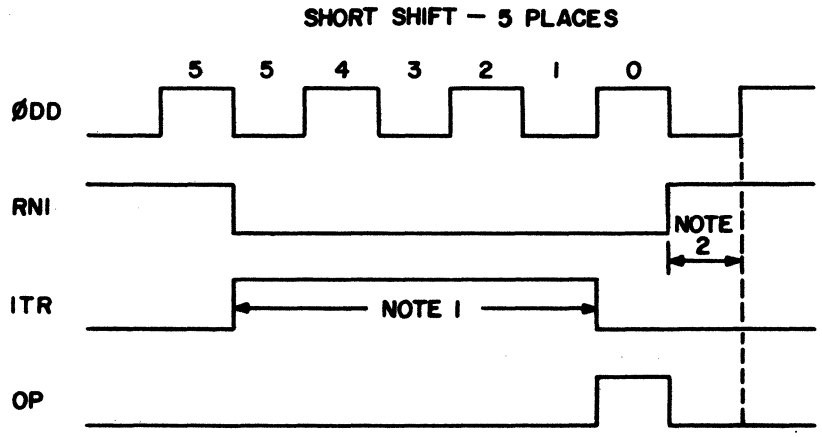


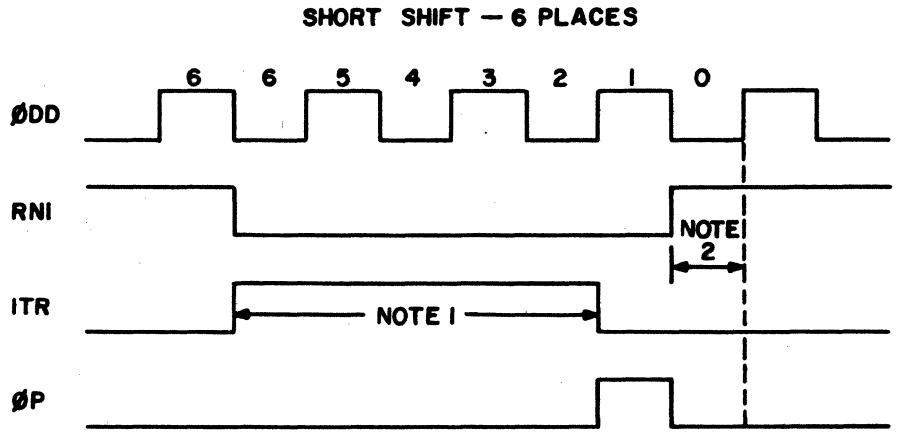
Storage Reference Instructions



TIMING

Timing for Shift Instructions (drawing 89617000)

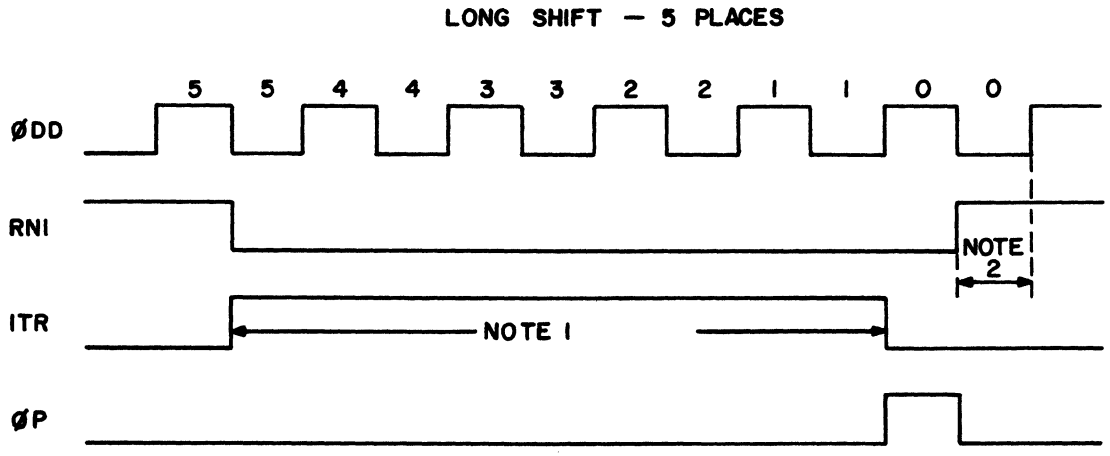




For notes refer to next page

TIMING

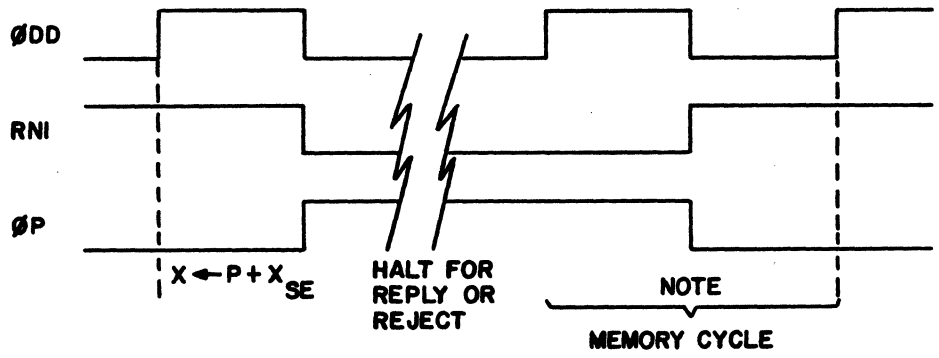
Timing for Shift Instruction (drawing 89617000)



NOTES:

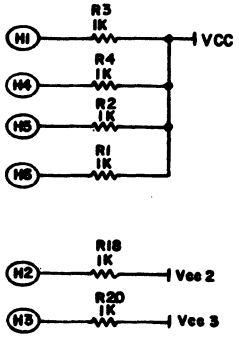
1. Q shifted on condition
   (EVEN·1S + $\overline{16}$·15)
   A shifted on condition
   (ØDD·16 + $\overline{15}$·16)
2. Q shifted on condition
   [15·$\overline{16}$. (One place or EVEN number of places)]
   A shifted on condition
   [15·16. (One place or EVEN number of places + 15·16. (One or more places)]

Timing for Input/Output Instructions



ØFF — SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SHEET LOCATION 2	3	4	5	6
A		C-1	D-3		
B		C-3	D-3		
D			C-1		A-2
E	D-1				B-4
F				B-3	B-2
G		B-3			A-4
K	B-2	B-2	C-3	B-2	C-2
L	C-3		D-2		A-4
M		A-2			D-1
N	B-2	B-2	C-2	B-3	C-2
P		B-1			C-3
R	C-4	A-3	C-3	C-4	C-3
S	B-4	C-4	B-4	D-4	C-4
T		C-4	B-3	C-3	
U		B-3	C-2	D-2	
V	C-3		C-3		
W	D-3	D-3			
X			C-2	D-3	A-4
Y		D-1		C-1	
Z				B-3	B-2
AA		B-4	D-3	C-4	
AB			D-4	B-4	
AC			C-4	C-4	
AD		B-1	D-4		
AE		D-4		C-2	
AF			B-1	B-2	
AG		C-1		B-2	
AK		B-4	C-3	C-4	
AL		D-4			D-2
AM		B-2		B-4	
AN		B-4		C-2	C-4
AP		B-3	C-3		
AQ			D-1	D-1	
AR		C-4		D-2	
AS	B-4	C-4	B-4	D-3	C-4
AT		C-1			D-4
AU		C-2			D-4
AV	D-1	D-4			D-4
AW			C-3	B-4	B-3
AX		C-3	D-3		
AY			C-2	C-2	
AZ		B-4		D-2	
AH		A-3			C-1
AJ				C-2	C-1



NOTES:
1. ALL RESISTOR ARE 1/4 WATT, 5%
2. FOR ASSY. 89779200 Y1 IS 12.2222 MHZ.
   89778201 Y1 IS 18.3333 MHZ
3. THE OSCILLATOR CIRCUIT (SHEET 2, ZONE A-2) FOR ASSEMBLY 89779200 HAS :
   C16 - 0.47 F IS NOT CONNECTED
   R19 - 130 OHMS IS NOT CONNECTED
   C15 - 47PF IS SHORT - CIRCUITED BY JUMPER WIRE S.
4. ELEMENT IDENTIFIER ARE PENDING. U16 AND U43 ARE 74S140.

SHEET REVISION STATUS

1	2	3	4	5	6
04	04	04	04	04	04
05	05	04	04	05	05
07	07	05	05	05	05
06	07	06	06	06	06
09	07	06	06	06	09
10	10	10	06	10	10
A	A	A	A	A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP'D
04	CK 239	REDRAWN PER C.D.C. STD.				
05	CK 421	ADDITION OF TABS TO FUNCTIONS				
06	CK 653	LOGIC DWG. CHANGES TO FIT PL AND ASSY				
07	CK 786	IMPROVED OSCILLATOR CIRCUIT FOR 900 NS ON SHT. 2, ZONES A -2,3 C16, 0.47μF. DISCONNECTED R10, 180 OHMS DISCONNECTED C15, 47 PF, SHORTED OUT				
08	CK 722	R21, 470 OHMS U64, ZONE B-2) ADDED FROM U64-12 TO +5V FITS PWB 89698600 REV 0 FOR ASSY 89769600 REV 0				
09	CK 815	ASSY. REV. 08 USES LOGIC REV 08 PLUS REWORK: ISOLATE U58-9,10 CONNECT U28-9,10 TO GROUND (SHT 6, B-5)				
10	CK 1067	860 CK 479 CANCELLED. FITS ASSY 89779200, -01 89778201 AND 02. SH1: REF. LTR. AE ADDED. REF LTR. W REVISED. SH5, D-5: PIN 14 REPL. AT U18-9 SH5, B-4: GATE U19-M, N, P, S, DELETED. PINS REPL. U19-8 AT U19-10 SH5, C-5: ING U53-5, 6 CUT AND MOVED TO SHT 6, C-4. SH5, A-5: JUMPER WIRE S ADDED AT TERMINALS OF C15, 47 PF SH3, D-3: C DELETED FROM REF. LTR W SH5, C-5: WIRE ADDED FROM U33-10 TO U34-13 ON SH5 (REF. LTR AJ). H ADDED TO ELEMENT IDENTIFIER OF INVERTER U27-11, 12 SH5, D-5: INVERTER U58-10, 11 DELETED SH6, B-5: TO FIT PL, 0.22 (430 OHMS) ADDED FROM +5V TO PIN 8 OF U51. SH6, A-2: GATE U35-1, 2, 3, 4, 5, 6 DELETED SH6, C-1: R19 (180) AND C16 U31-13, 1, 2, 12 ADDED; PIN 8 OF U31 REPL; U9-10 AT U33-5, U31-1, 2 REVS; PINS 8 AT U58-6 U31-12 REPL; U35-4 AT U51-4		5-20-76		
A	CK 1176	RELEASED CHANGE A. NOTE 4 ADDED ALL +5V TO VCC.				

DO NOT SCALE DRAWING

MATERIAL: 1/1

FINISH: N/A

DETACHED LISTS: AY 89779201, AY 89779200, AW 89778200

ELBIT COMPUTERS LTD

CONTROL DATA

FIRST USE ON: AB107-A, AB108-A

DRN	DAIAN	
CHK		
ENGR		
MFG		
APPD		5.11.75
Q.A.		

TITLE: DETAILED LOGIC DIAGRAM TIMING

CODE IDENT: C

DRAWING NO: 89617000

SCALE:

SHEET 1 OF 6

TIMING (drawing 89617000 sheet 2)

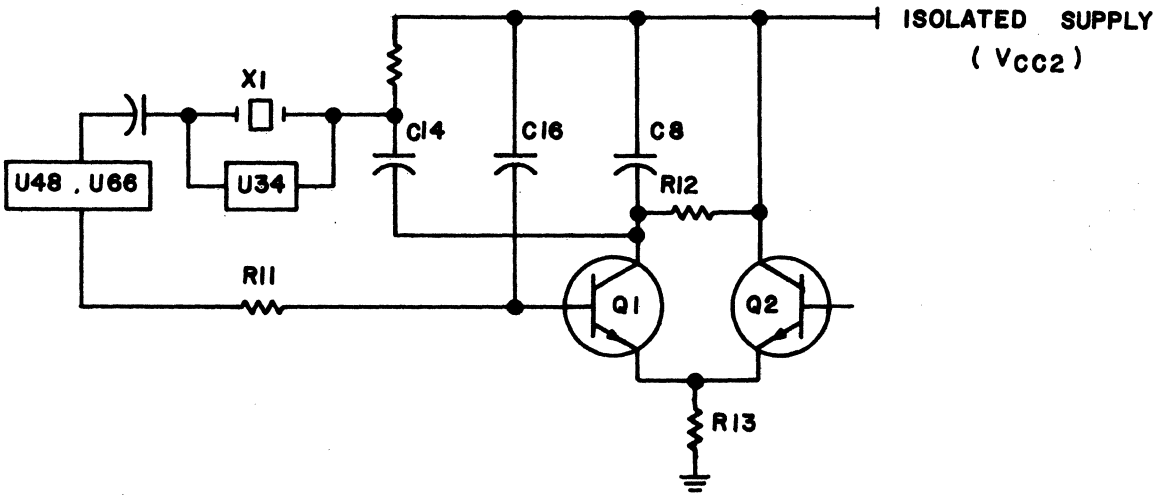
OSCILLATOR AND PHASE GENERATOR

Function

The oscillator and phase generator form the basic clock of the CPU and therefore of the computer. The basic oscillator frequency is determined by crystal Y1. This frequency differs in the two versions of the computer as shown in the table:

Equipment	Memory Cycle Time	Basic Clock Frequency
AB107	900 nsec	12.222 MHz
AB108	600 nsec	18.333 MHz

The oscillator circuit itself is a resonant circuit using the crystal Y1 as the frequency determining element in the base-collector circuit of transistor Q1; the simplified circuit diagram shows this clearly. The output of the comparator acting on the threshold of the logic circuits in the feedback path ensure that the oscillator output signal is a symmetrical square wave. Transistor Q2 and the common emitter resistor R13 stabilize Q1 of the oscillator; series stabilizing transistor Q3 isolates the V_{CC2} supply line from the oscillator signals.



Oscillator Simplified Circuit Diagram

TIMING - (Drawing Number 89617000, sheet 2, cont'd.)

Inputs:

SIGNAL	ACTIVE	CONNECTOR	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{\text{VIØ}}$	L	P1A06	Program Protect Violation	2	D-4
$\overline{\text{GØAQ}}$	L	P1B16	Hold CPU during I/O operation	2	D-2
$\overline{\text{GØM1}}$	L	P1A08	Hold CPU on busy Memory (bank 1)	2	D-2
$\overline{\text{GØM2}}$	L	P1A05	Hold CPU on busy Memory (bank 2)	2	D-2
CSPR	H	P1A04	Clocks registers to enter data from Programmer's Console	2	D-2
				2	D-2
$\overline{\text{SGI}}$	L	P2B22	Set Go	2	B-4
SSI	H	P1A19	Set Stop	2	D-4
EXT	H	P1B27	Extended odd CPU cycle (compare ØDD2)	2	C-4
STPCK	H	P1B07	Stop Clock	2	B-3
EXCK	H	P1B02	External Clock	2	A-2
CLREQ	H	P2A15	Clear Request	2	C-2
MMRQ	H	P1B03	Memory request	2	B-2

TIMING (drawing 89617000, sheet 2, cont'd.)

Outputs:

SIGNAL	ACTIVE	CONNECTOR	FUNCTION	LOCATION SHEET	LOCATION SQUARE
PH1	H	P1A15	Phase generator outputs	2	C-2
PH2	H	P1B08		2	C-2
PH3	H	P1A22		2	C-2
PH4	H	P1B25		2	D-1
JKCK	H	P2B05	Phase 5 of Phase generator	2	C-1
GØCS	H	P1B21	Computer running	2	D-3
EVEN	H	P2A18	Even CPU cycle	2	B-1
$\overline{\text{ØDD}}$	L	P2B19	Odd CPU cycle	2	B-1
ØDD2	H	P1B22	Two consecutive odd CPU cycles	2	C-3
$\overline{\text{ØDD2}}$	L	P2B11		2	B-3
CRQ	H	P1A03	CPU cycle request to Memory Control card	2	B-1
$\overline{\text{CRQ}}$	L	P1B19		2	B-1
$\overline{\text{ØSC}}$	L	P1A07	Clock to Memory system	2	A-1
DCK	H	P1B06	Not connected	2	D-1

TIMING (drawing 89617000, sheet 2, cont'd.)

Description

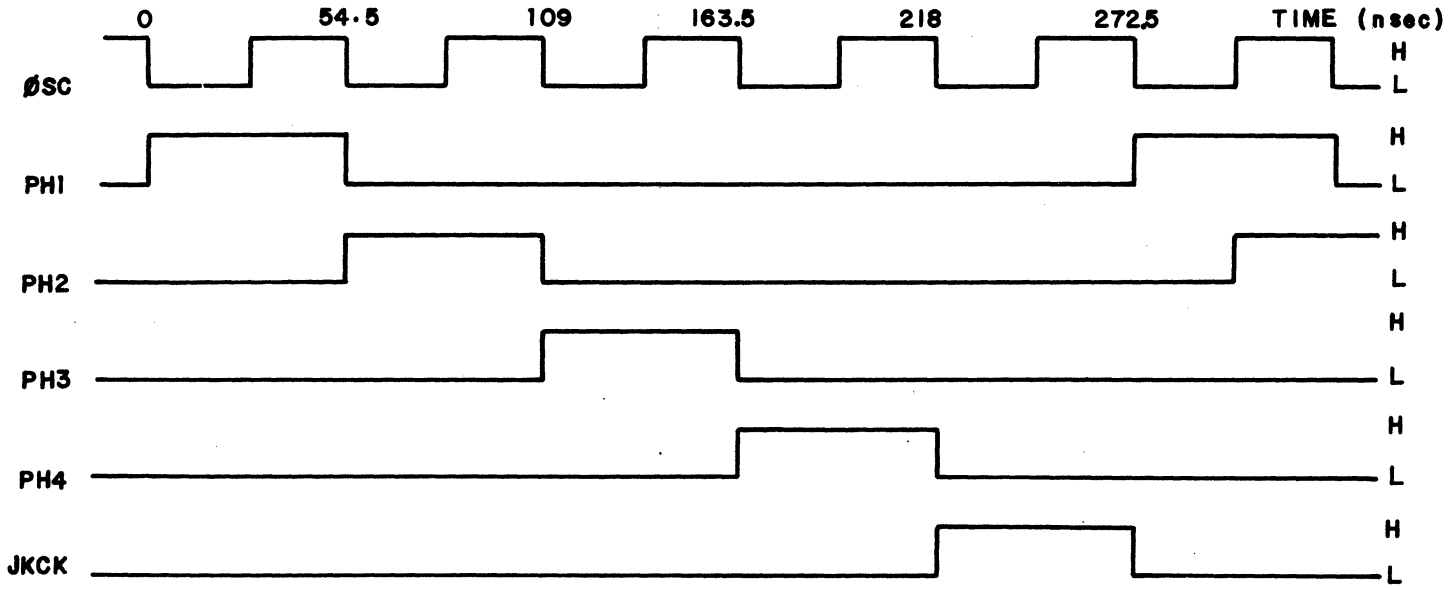
The output at U66/6,8 provides the clock signal to the memory system ($\overline{\text{ØSC}}$); the output at U48/8 (ØSC) drives the phase generator.

The oscillator is stopped by a low on signal STPCK. In this case an external clock signal may be connected at EXCK.

The oscillator output drives the five-phase generator (PG). This consists of three-stage counter PG1, PG2, PG3 (U17, U18) and associated gates forming a five-state machine. The equations of the phase generator outputs are as follows:

$$PH1 = \overline{PG1} \cdot \overline{PG2} \cdot \overline{PG3}$$
$$PH2 = PG1 \cdot PG2$$
$$PH3 = PG1 \cdot PG2$$
$$PH4 = \overline{PG1} \cdot PG2 \cdot \overline{V10}$$
$$PH5 = JKCK = PG3$$

The output waveforms of the oscillator and phase generator are shown below. Note that the waveforms are the same for the two equipments AB107 and AB108, the time scale shown applies to the AB108. To obtain the timing for the AB107 (900 nsec memory cycle), multiply the figures by 1.5.



The fifth phase of the clock (JKCK) is the last phase of the CPU cycle. Its trailing edge forms the main timing data for all state flip-flops.

TIMING (drawing 89617000, sheet 2, cont'd.)

The signal V10 causes the phase generator to jump directly from PH4 to PH1, avoiding the JKCK clock. This occurs during program protect violation (types 2, 3) (see program protect: 1784 Reference Manual, publication number 89633400, pages 4-9, 4-10, 5-3, 6-4, 6-7).

The signal GØAQ stops the phase generator while waiting for the Reply or Reject in an I/O operation.

The CSPR is active when the computer is not running. It enables D-type clocks used for setting bits in registers of Programmer's Console, while J-K clocks are avoided. In this circuit it gates flip-flop PG3.

The signals GØM1 and GØM2 are generated by the Memory Control (upper and lower banks) and are used to hold the CPU on phase five; this occurs in two cases:

1) When a CPU Memory Request arrives while the memory is busy with a DSA request (CPU held just before end of an odd cycle);

2) When the CPU is waiting for data or sending data to the memory (CPU held just before end of even cycle).

Computer Active/Inactive

The GØCS flip-flop (U61) indicates whether the computer is running or not; its output (GØCS) is connected to the CPU INACTIVE indicator on the programmer's console (computer not running). The GØCS signal also stops the computer on phase 1 (PH1) of the phase generator, just after the beginning of an odd cycle.

The GØCS flip-flop is set by signal SG1 and is cleared by SS1, both from the console interface board. The flip-flop is synchronized by the clock output (ØSC); flip-flop U61/14,15 acts as a synchronizing buffer for the GØCS flip-flop.

TIMING (drawing 89617000, sheet 2, cont'd.)

Even - Odd Circuit

Every CPU cycle is defined as either an even or an odd cycle. The even and odd flip-flops (U4) determine the state of the machine. Usually even and odd cycles will alternate so that one flip-flop will be set and the other reset on the first cycle, and both flip-flops will change state on the following cycle. In some cases the odd state continues for two successive cycles. In such a condition a third flip-flop, called ØDD2 (U8) will be set during the second odd cycle. The ØDD2 flip-flop is set by the signal EXT from the I/O Interface board and resets itself after one cycle.

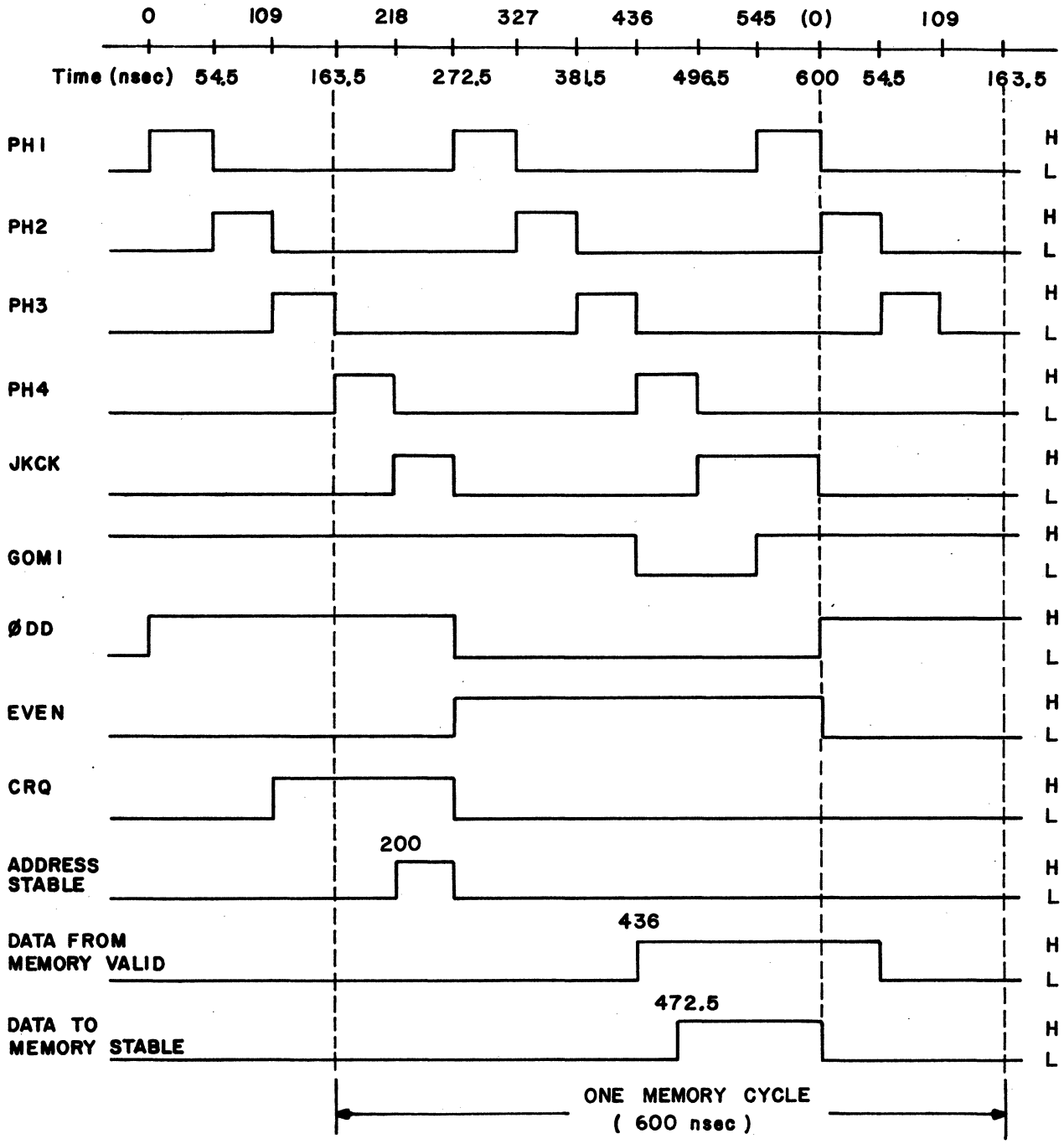
The flip-flops EVEN, ØDD and ØDD2 are clocked by JKCK. The input equations are as follows:

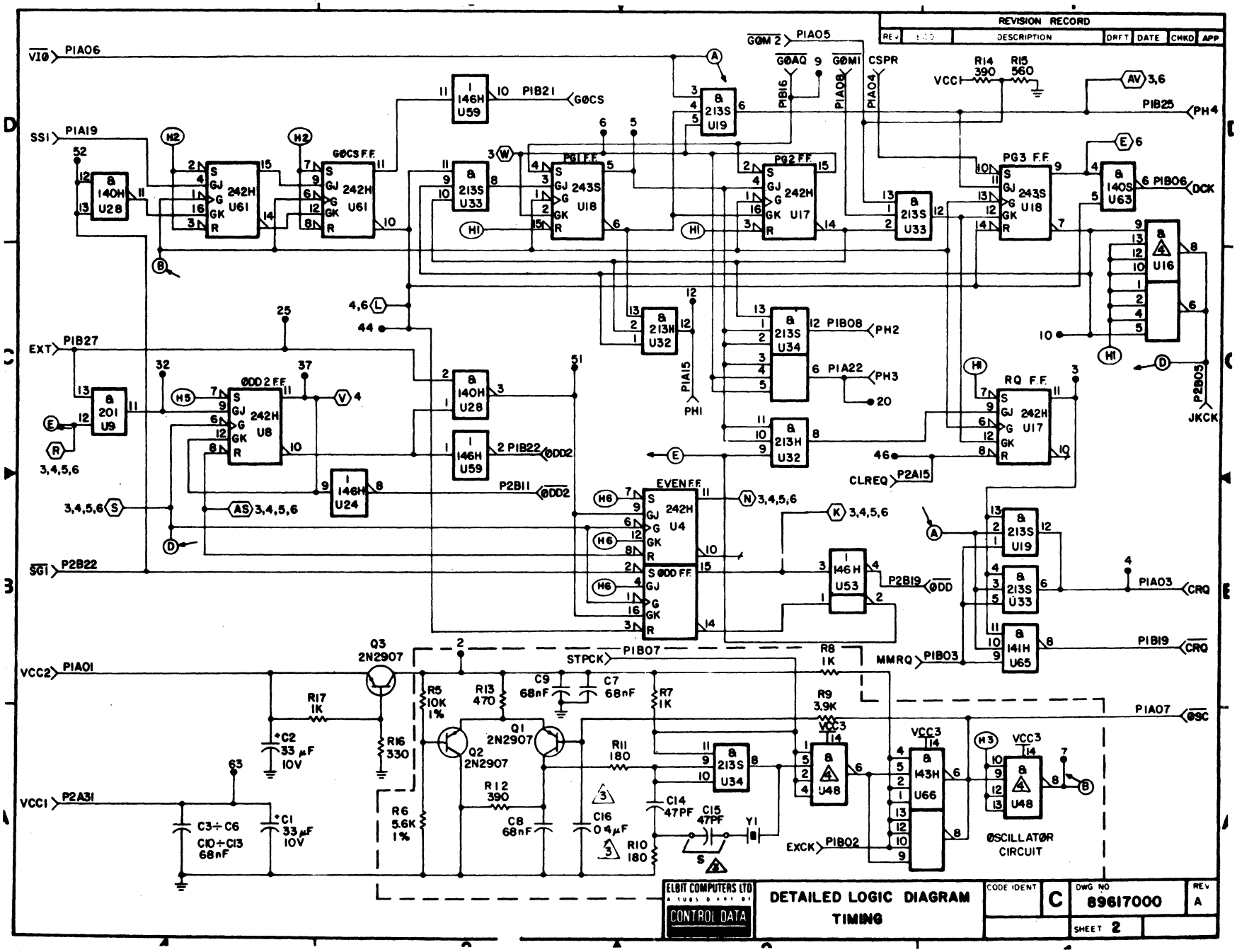
Flip-flop	SET	RESET	J	K
EVEN	H	$\overline{MPC}$	ØDD2 + $\overline{EXT}$	H
ØDD	SG1	GØCS	H	ØDD2 + $\overline{EXT}$
ØDD2	H	$\overline{MPC}$	ØDD·EXT	ØDD2

The RQ flip-flop (U17) produces a timing signal for CPU memory requests. It is set at PH3 on odd CPU cycles and cleared at the end of the cycle. The output of this flip-flop is multiplied by V10 and by the signal MMRQ from the I/O Interface to product CRQ which is transmitted to the Memory Control Card.

TIMING (drawing 89617000, sheet 2, cont'd.)

A timing diagram for typical CPU Memory Cycles is shown below. Note that the JKCK signal is extended in the even part of the cycle when the CPU is stopped by the GØM1 or GØM2 signals, the timing of the CRQ signal is determined by the RQ flip-flop. The timing shown is for the 600 nsec memory cycle. To obtain the timing for the 900 nsec memory cycle multiply the figures by 1.5.




REVISION RECORD
REV | DESCRIPTION | DRFT | DATE | CHKD | APP
VIØ PIA06
SSI PIA19
EXT PIB27
SGI P2B22
VCC2 PIA01
VCC1 P2A31
GØM 2 PIA05
GØAQ 9 GØMI CSPR
PIB16 PIA08 PIA04
VCC1 R14 390 R15 560
AV 3,6
PIB25 PH4
PG3 F.F.
6 PIB06 DCK
RQ F.F.
P2B05 JKCK
PIA15 PHI
PIB08 PH2
PIA22 PH3
20
CLREQ P2A15
46
EVEN F.F.
ØDD2 F.F.
S ØDD F.F.
2 PIB22 ØDD2
P2B11 ØDD2
3,4,5,6
P2B19 ØDD
PIA03 CRQ
PIB19 CRQ
MMRQ PIB03
PIB07 STPCK
PIA07 ØSC
EXCK PIB02
Q1 2N2907
Q2 2N2907
Q3 2N2907
R1 180
R2 390
R3 470
R4 1K
R5 10K 1%
R6 5.6K 1%
R7 1K
R8 1K
R9 3.9K
R10 180
R11 180
R12 390
R13 470
R16 330
R17 1K
C1 33 µF 10V
C2 33 µF 10V
C3÷C6 C10÷C13 68nF
C7 68nF
C8 68nF
C9 68nF
C14 47PF
C15 47PF
C16 0.4µF
Y1
ØSCILLATØR CIRCUIT
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
TIMING
CODE IDENT C
DWG NO 89617000
REV A
SHEET 2

TIMING (Drawing number 89617000, sheet 3)

COUNTER

Function:

The 5-bit binary count down counter is used for the following:

1. During shift instructions it is used to count the number of times a word is shifted.

2. During Multiply/Divide instruction it is used to count the number of iterations necessary to complete the operation. In this case it is loaded with the number 10110_2.

3. During any memory reference instruction it may be used to count the number of memory reference cycles needed to calculate the effective address of the operand. In this case it may be loaded with either 00000_2, 00010_2, 00100_2, or 00110_2.

Inputs

SIGNAL	ACTIVE	CONNECTOR/ PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{MPC}$	L	[AS]	Master clear or clear-to-P-register	3	C4
$\overline{ENI}$	L	[T]	CPU in interrupt state		C4
JKCK	H	[S]	Clock from phase generator (sheet 2)		C4
I0	H	P1B17	Least significant bits of instruction register		D4
I1	H	P1B18			D4
I2	H	P1A17			D3
I3	H	P1B05			D2
I4	H	P1B24			D2
I5	H	P2A10			A4
I6	H	P2B10			A4
$\overline{JITR}$	L	P2B09	Set ITR flip-flop		A4
PH4	H	[AV]	Clock phase generator (sheet 2)		B4
F23	H	[AN] see [Y]	Instruction register F=2 or F=3		
PG2	H	[W]	Second stage of phase G		D3
AD1	H	P1A16			D4
AD2	H	P1B20			D3
Outputs					
N0		P1B28	Least significant bit of counter		B3
$\overline{CNTE2}$	L	P2A09	Counter content = 00010_2		B1
N41	H	P2B07	Counter content $\leq 00001_2$		B1
$\overline{\emptyset I6}$	L	P2A16	$\overline{\emptyset DD \cdot I6}$		B1
$\overline{EI5}$	H	P2A17	$\overline{EVEN \cdot I5}$		A1
$\overline{MD1}$	L	P2B01	$\overline{N4 \cdot N3 \cdot N2 \cdot N1 \cdot N0 \cdot ADR} \cdot F23$	3	B3

TIMING (Drawing number 89617000, sheet 3, cont'd.)

Description

The counter itself is made up of five flip-flops; N0, N1, N2, N3 and N4 (U13, U14, U12). The most significant bit is N4 and the least significant is N0. All the flip-flops are clocked by phase 5 of the clock (JKCK) and they are cleared by either the clock signal $\overline{MPC}$ or by signal $\overline{ENI}$. $\overline{MPC}$ is active when the CPU receives a Master Clear signal or a Clear to the P register. $\overline{ENI}$ is active when the CPU goes into an interrupt state.

The counter is loaded through the set (S) input of each flip-flop, as follows:-

For Shift instructions the counter is loaded with the five least significant bits of the instruction register, I4, I3, I2, I1, I0. The setting of the flip-flops is enabled by the signal JITR·PH4 which is produced at U58/11.

For Multiply/Divide instructions the counter is loaded with the number 10110_2. The flip-flops are set by the signal ØP·EVEN·PG2·F23. The signals ØP·EVEN and PG2 define a specific time period while F23 is active, that is, when the F field of the instruction register is decoded as F = 2 or F = 3.

For Memory Reference instructions the counter is set by the signals AD1 and AD2. These signals are produced on the Decoder assembly. They determine whether the counter will be preset to 00000_2, 00010_2, 00100_2, or 00110_2. The setting of the flip-flops is enabled by the signal RNI·ØDD·FE0·PH4, where RNI, ØDD and PH4 define a specific time period and FE0 is active when the F field of the instruction register is not equal to zero.

Each flip-flop changes state on JKCK when its J and K inputs are high. This occurs on the signal transmission (high-to-low) when the previous flip-flop changes state. Thus the counter counts down.

TIMING (Drawing number 89617000, sheet 3, cont'd.)

The least significant flip-flop (N0) changes state on every JKCK clock except when one of the following conditions is true (signal at U45/6):

1. (Counter = 0)·RN112·(AD1 + AD2) at U44/8.

   This function enables the counter to decrement immediately on loading the memory reference instruction.
   Note that the function N41·$\overline{N0}$ determines that the (Counter = 0) and that this situation exists most of the time.
   Here N41 = $\overline{N4}$·$\overline{N3}$·$\overline{N2}$·$\overline{N1}$

2. ADR·(Counter = 2)[(F1 = 5, 7, D, F)·32KW·X15 + EVEN].

   This occurs during multi-level indirect addressing, when the counter is not decremented until the last level is reached.

3. JITR

   This occurs when the counter is loaded at the beginning of a shift instruction.

4. MDS·EVEN

   This occurs during multiply/divide instructions, when the counter is decremented only on odd cycles.

5. ITR·ØDD·I5·I6

   This occurs during Double Word Shift operations, when the counter is decremented only on EVEN cycles.

A simplified diagram of the loading and decrementing counter is given on page 5-264.

TIMING (Drawing 89617000, sheet 3, cont'd.)

Three signals derived from the counter are also used on other assemblies of the CPU. These are:

Signal	Connector/pin	Counter content
$\overline{\text{CNTE2}}$	P2A9	00010_2
N41	P2B7	00000_2 or 00001_2
NO	P1B28	odd number

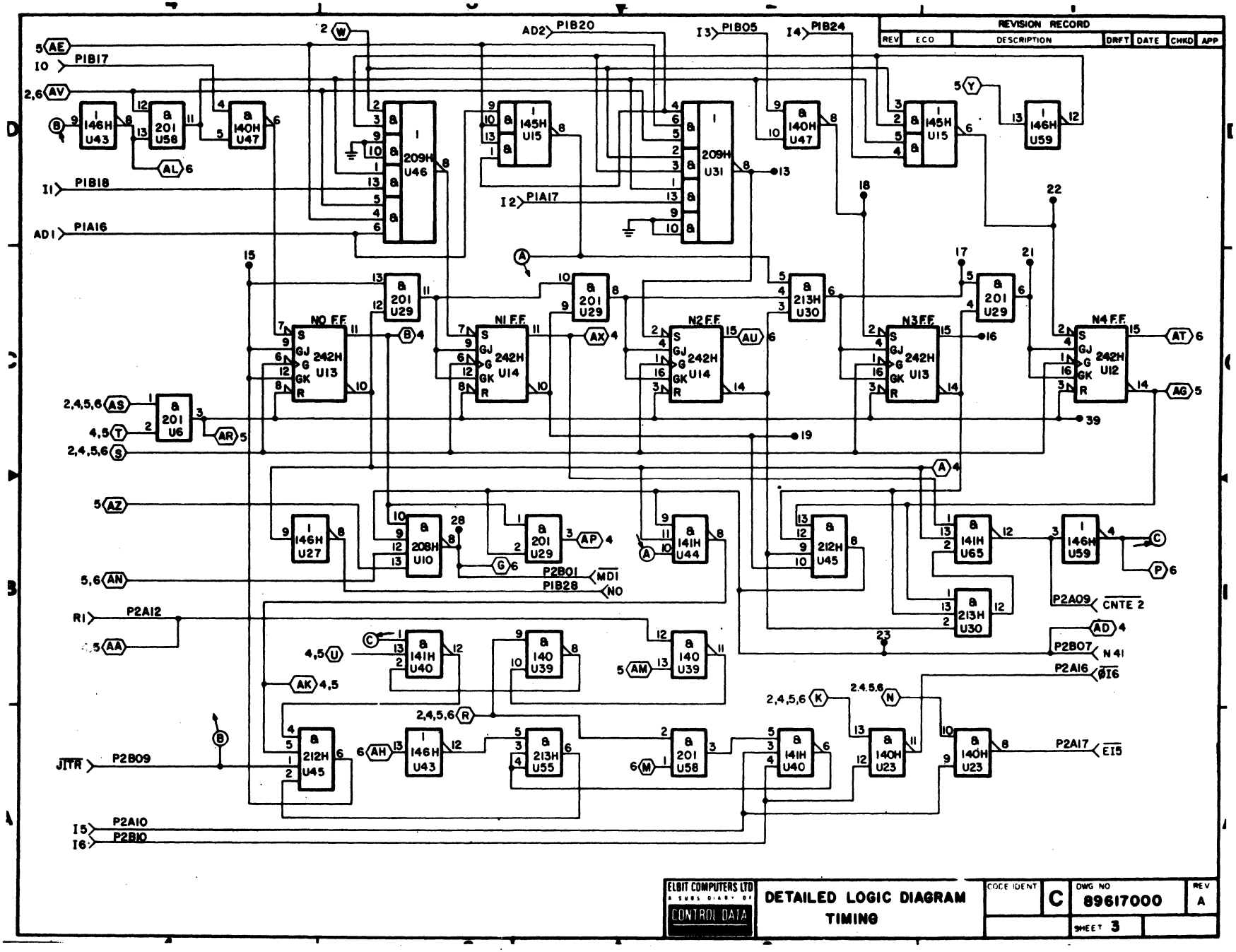
The following signals produced on the Timing assembly are used by the Decoder:

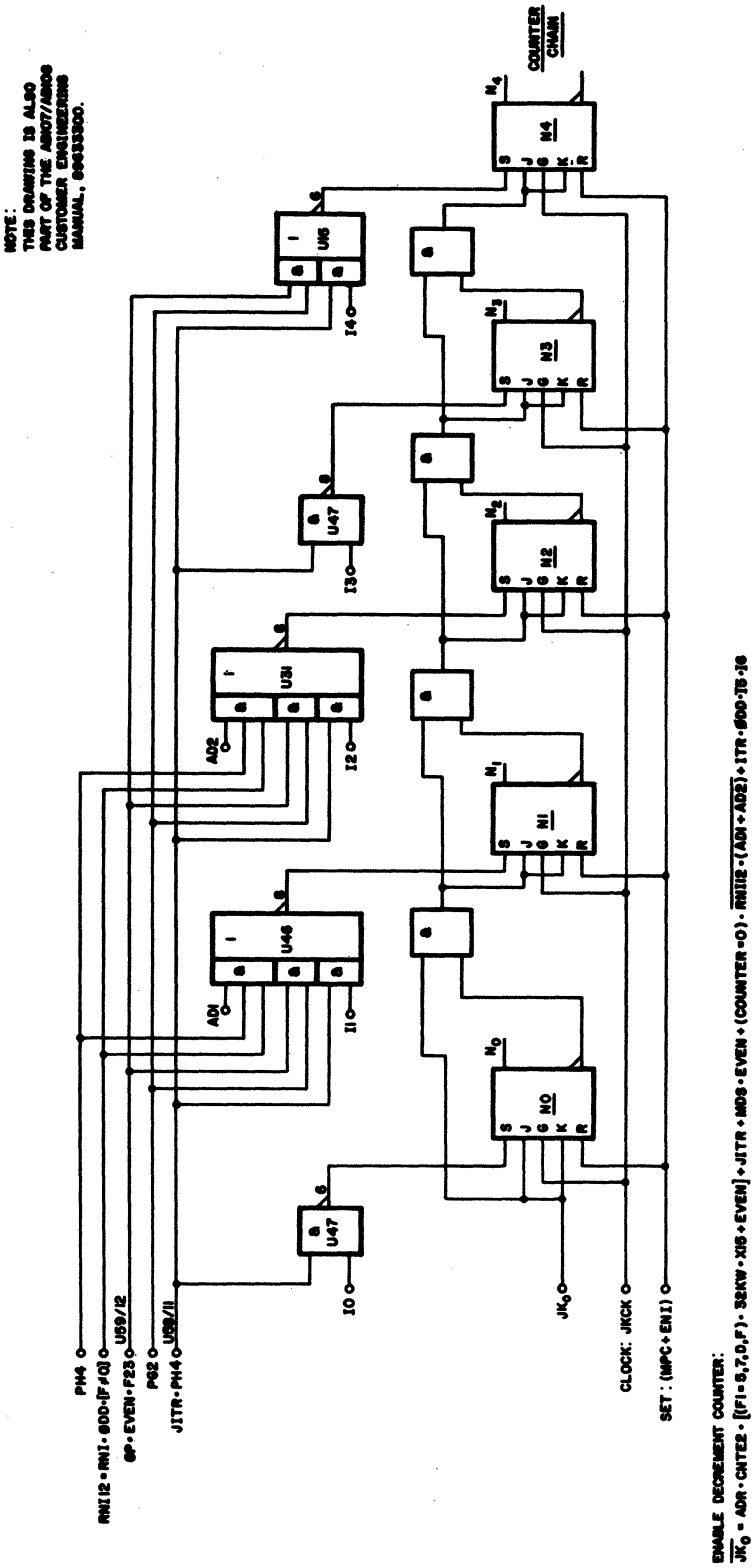
1. MD1, (at U10/8), is active during multiply/divide instructions when the counter is at 00001_2

2. $\overline{\text{Ø16}} = \overline{\text{ØDD}} + \overline{\text{16}}$

3. $\overline{\text{E15}} = \overline{\text{EVEN}} + \overline{\text{15}}$

$\overline{\text{Ø16}}$ and $\overline{\text{E15}}$ are used during Shift Instructions.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
I 146H U43
A 201 U58
A 140H U47
I 209H U46
I 145H U15
I 209H U31
A 140H U47
I 145H U15
I 146H U59
A 201 U29
A 201 U29
A 213H U30
A 201 U29
N0 F.F.
N1 F.F.
N2 F.F.
N3 F.F.
N4 F.F.
S GJ G GK R
242H U13
242H U14
242H U14
242H U13
242H U12
A 201 U6
I 146H U27
A 208H U10
A 201 U29
A 141H U44
A 212H U45
A 141H U65
I 146H U59
A 213H U30
A 141H U40
A 140 U39
A 140 U39
A 212H U45
I 146H U43
A 213H U55
A 201 U58
A 141H U40
A 140H U23
A 140H U23
PIB17
PIB18
PIA16
PIA17
PIB20
PIB05
PIB24
P2A12
P2B09
P2A10
P2B10
P2B01 MDI
PIB28 NO
P2A09 CNTE 2
P2B07 N41
P2A16 ØI16
P2A17 EI5
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
TIMING
CODE IDENT C
DWG NO 89617000
REV A
SHEET 3


NOTE:
THIS DRAWING IS ALSO
PART OF THE ABOT/ABOB
CUSTOMER ENGINEERING
MANUAL, 89633300.
COUNTER
CHAIN
N4
N3
N2
N1
N0
U46
U47
U35
U36
I4
I3
I2
I1
I0
AD0
AD1
AD2
PH4
RNI2•RNI•@OD•(F≠0)
GP•EVEN•F23
P02
JITR•PH4
US0/12
US0/11
JK0
CLOCK: JKCK
SET: (MPC+ENI)
ENABLE DECREMENT COUNTER:
JK0 = ADR·CHTE2·[(FI=5,7,D,F)+38KW+XIS+EVEN]+JITR+MDS+EVEN+(COUNTER=0)·RNIIE·(AD1+AD2)+ITR·@DD-15-16

TIMING (Drawing number 89617000, sheet 4)

INTERRUPT TIMING, Y REGISTER CONTROL LOGIC

Function:

This circuit includes timing signals which control the transition into the interrupt state and logic for controlling the Y register in the ALU.

Inputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
IN0	H	P1A21		4	D3
IN41	H	P1A25	(F1=4)+(F1=C)		D4
IN32	H	P2A07	(F1=6)+(F1=E)		C4
JENI	H	P2A13	Sets ENI		C4
$\overline{\text{KENI1}}$	L	P1A20	Resets ENI		B4
R2	H	P2B12	Bit 9 of IR		C4
R3	H	P2A28	Bit 10 of IR		D4
R4	H	P2B18	Bit 11 of IR		D4
$\overline{\text{CSY}}$	L	P1B29	Programmer's Console selects Y-register		D2
32KW	H	[AC]	See sheet 5		
N41	H	[AD]	See sheet 3		
$\overline{\text{MPC}}$	L	[AS]	See sheet 5		
		[AK]	$\overline{\text{RNI12}\cdot(\text{AD1}+\text{AD2})\cdot\overline{\text{N0}}\cdot\overline{\text{N1}}\cdot\overline{\text{N2}}\cdot\overline{\text{N3}}\cdot\overline{\text{N4}}}$		
		[AP]	$\text{N0}\cdot\overline{\text{N1}}\cdot\overline{\text{N2}}\cdot\overline{\text{N3}}\cdot\overline{\text{N4}} = \text{N0}\cdot\text{N41}$		
$\overline{\text{ØDD}}$	L	[K], [R]	See sheet 2		
$\overline{\text{N0}}$	H	[A]	See sheet 3		
ØDDO2	H	[V]			
		[AP]	N41·N0		
GØCS	H	[L]			
ADR	H	[V]			
$\overline{\text{EAD}}$	L	[AY]			
ØP2	H	[AQ]	See sheet 5		
RNI	H	[X]	See sheet 5		
EVEN	H	[N]	See sheet 2	4	

TIMING (Drawing number 89617000, Sheet 4, cont'd.)

Outputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
ENI	H	P2B15	Enter interrupt	4	A3
$\overline{\text{ENI03}}$	H	P2B16	ENI·$\overline{\text{IN12}}$·GØCS		A3
ENI02	H	P2A06	ENI·ØDD2		B3
$\overline{\text{ENI20}}$	L	P2A21	ENI2·ØDD		A2
$\overline{\text{ENI2E}}$	L	P2A20	ENI2·EVEN		B1
$\overline{\text{ØP2Ø}}$	L	P2A24	ØP2·ØDD		D1
YTAUG	H	P1A30	Controls output of Y register		C1
SGL	H	P2A14	-1 or -0 to Augend gates		B1
$\overline{\text{ADY}}$	L	P1A24	Add Y register	4	D1

Description

The Enter Interrupt Sequence is initiated by the signal JENI from the Console Interface card. This signal causes the ENI flip-flop (U7/15) to be set. The flip-flop is clocked by phase 5 of the timing chain, JKCK (see Timing, sheet 2) and is reset by $\overline{\text{MPC}}$ (see Timing, sheet 5). The output of the flip-flop is at U24/2. At the end of time ENI·ØDD2 the ENI2 flip-flop (U7/11) is set. This flip-flop is also clocked by JKCK and cleared by $\overline{\text{MPC}}$. The output of the ENI2 flip-flop is ANDed with EVEN and ØDD (see Timing, sheet 2) to produce ENI2E and ENI20 respectively. ENI20 is used to reset the ENI and ENI2 flip-flops. This is the normal end of the enter interrupt sequence and is followed by the setting of the RNI flip-flop (see Timing, sheet 5).

The Enter Interrupt Sequence may be aborted prematurely by the signal KENI1 which resets the ENI flip-flop and prevents the RNI flip-flop from resetting.

TIMING (Drawing number 89617000, sheet 4, cont'd.)

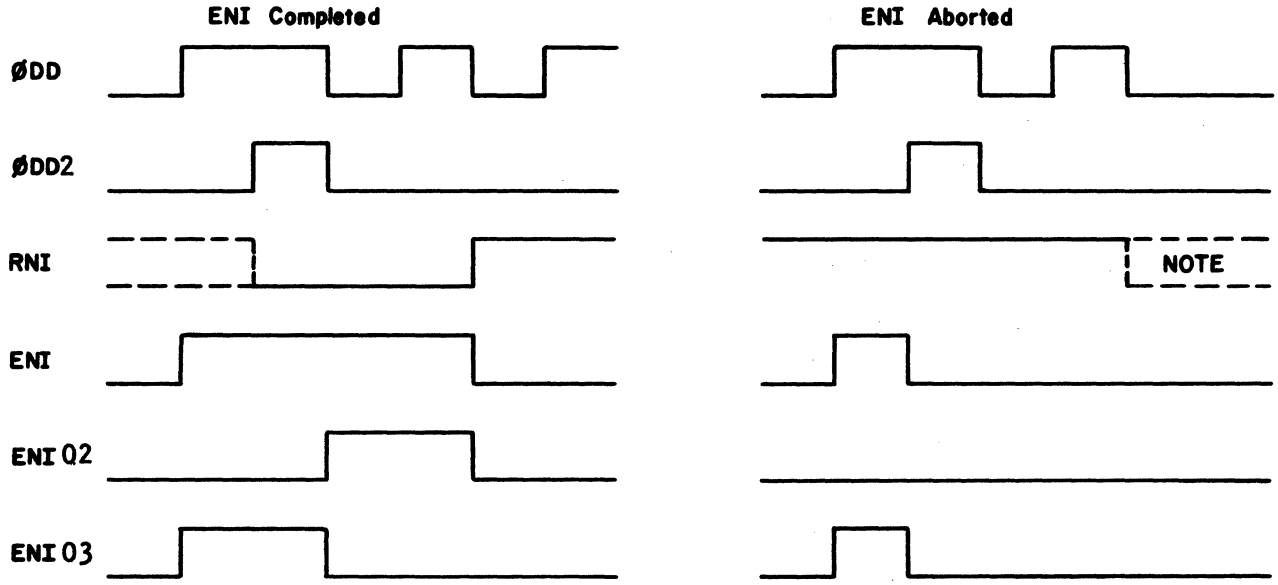
Other signals produced by this logic circuit are:

$\overline{ENI03} = \overline{ENI \cdot \overline{ENI01} \cdot G\emptyset CS}$

and SGL = ENI02·EVEN = ENI2E (at P2A14)

SGL is an ALU control.

Timing diagram for this logic circuit is shown below.



NOTE: RNI may or may not be active at this time.

ALU Y register control

The signal YTAUG is produced in this section. This signal allows the output of the Y register to be enabled through the augend gates to the adder in the ALU circuit. The logic equation of this signal is as follows:

YTAUG = CSY + ØP20 + ADY

where

$ADY = ADR \cdot G\emptyset CS \cdot \overline{N1 \cdot R1 \cdot (\overline{R4}+R3)} \cdot \overline{NO \cdot INO} \cdot \overline{\overline{NO} \cdot N41 \cdot (IN4+IN32 \cdot 32KW \cdot X15)}$

The first two terms of ADY are GØCS (see Timing, sheet 2) and ADR (see Timing, sheet 5). This restricts the YTAUG to situations where the computer is in the addressing state, and is running.

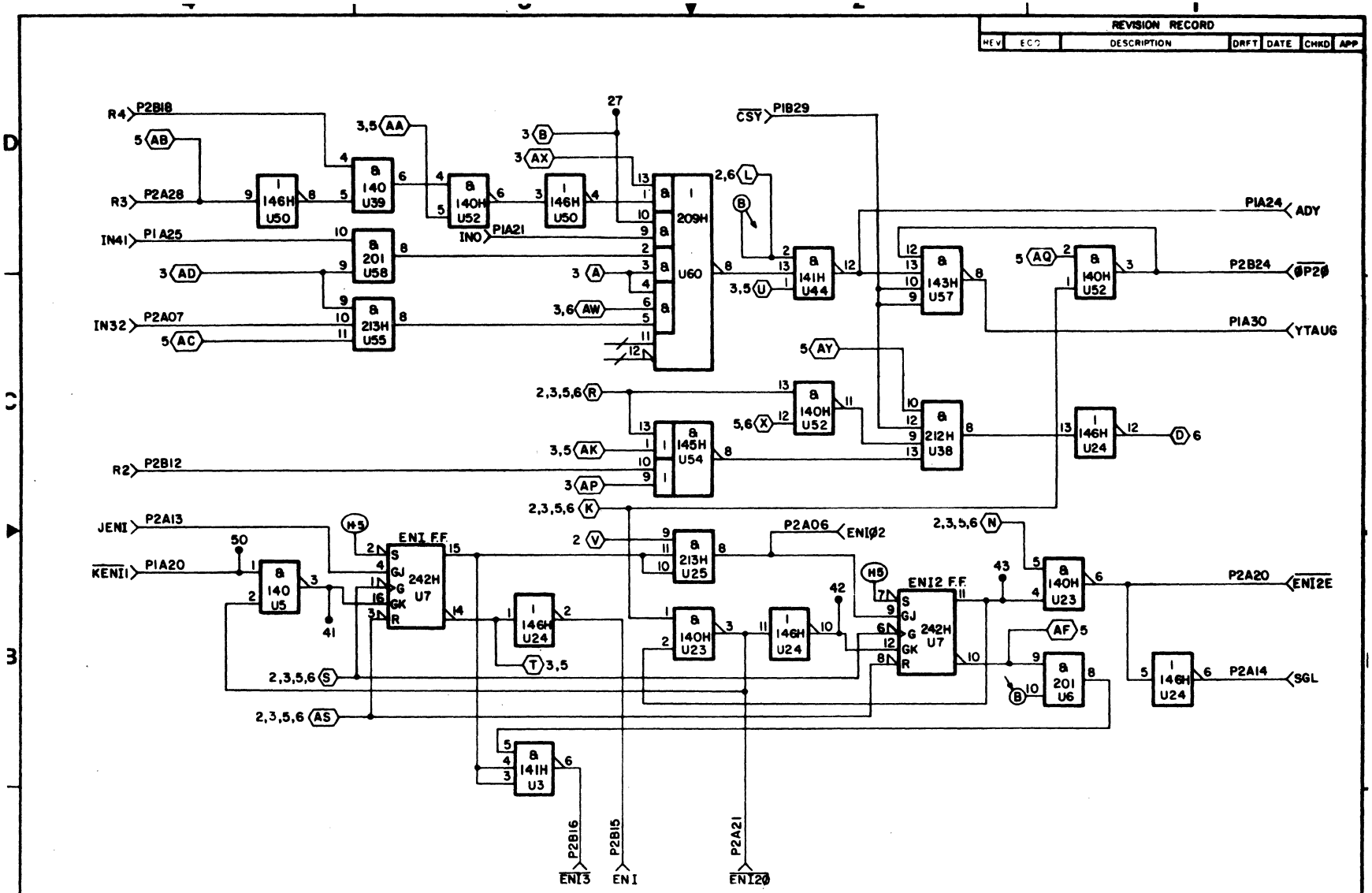
The remaining terms of ADY define specific cycles of the addressing state where the YTAUG signal is not active. The signals N0, N1, and N4, are produced by the counter (see Timing, sheet 3). The signals R1, R3 and R4 are equivalent to bits 08, 10, and 11 respectively of the instruction register. Signals IN0, IN32, and IN41 are produced on the I/O Interface and are decoded from the F1 field of the instruction register. The signal X15 is the most significant bit of the X register which is stored in a flip-flop (see Timing, sheet 6); the signal 32KW is connected to the 65K/32K mode switch on the programmer's console. In addition, the terms CSY and ØP20 produce a YTAUG signal when the Y register is selected by pushbutton on the Programmer's Console or when the ØP20 timing signal is active.

The signal WY at the output of U24/12 is the decoded condition for writing in the Y register. It is transmitted to the Timing circuit (sheet 6) where it is ANDed with a clock signal to produce the Y register clock. The logic equation of this signal is:

$$WY = EAD + CSY + RN1 \cdot \text{ØDD} + \text{ØDD} \cdot (COUNTER \neq 0) + (COUNTER = 1) \cdot R2$$

The signal EAD (End of Address or End of effective Address) is generated in the Timing circuit (sheet 5). It is active on the last CPU cycle of the addressing sequence for the memory reference instruction. CSY is active when the computer is stopped and the Y register is selected on the programmer's console.

The signal RN1·ØDD is active during the first CPU cycle of each instruction. The signal R1 is active when the counter is at 1 and bit 9 of the instruction register is such that F1 = 2, 3, 4, 7, A, B, E, or F.


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
R4 P2B18
5 AB
R3 P2A28
IN41 P1A25
3 AD
IN32 P2A07
5 AC
3,5 AA
27
3 B
3 AX
3 A
3,6 AW
CSY P1B29
2,6 L
B
3,5 U
P1A24 ADY
P1A30 YTAUG
5 AQ
P2B24 ØP2Ø
5 AY
2,3,5,6 R
5,6 X
3,5 AK
R2 P2B12
3 AP
2,3,5,6 K
JENI P2A13
KENI1 P1A20
50
41
H5
ENI F.F.
242H U7
2 V
P2A06 ENIØ2
2,3,5,6 N
H8
ENI2 F.F.
43
42
P2A20 ENI2E
AF 5
B
P2A14 SGL
2,3,5,6 S
T 3,5
2,3,5,6 AS
INO P1A21
P2B16 ENI3
P2B15 ENI
P2A21 ENIØ2
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
TIMING
CODE IDENT C
DWG NO 89617000
REV A
SHEET 4

TIMING (Drawing number 89617000, sheet 5)

MAIN SEQUENCE FLIP-FLOPS

Function:

This section contains four of the main sequence flip-flops;

Signal	Flip-Flop/Output Pin
RNI	U22/11
ADR	U8/15
ØP2	U41/15
ØP	U41/11

One of these flip-flops is usually set except during multiply/divide, shift instructions or the enter interrupt sequence (refer to Timing, sheet 4). No more than one of these flip-flops may be set during any one cycle.

Inputs

SIGNAL	ACTIVE	CONNECTOR/ PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{\text{JRNI}}$	L	P2A24	J input to RNI flip-flop	5	D4
KRNI	H	P2B25	K input to RNI flip-flop		D4
MPC	H	P1A26	Master clear, clear P register		C4
ØDD	H	[R],[K]			
EVEN	H	[N]			
32KW	H	P2B08	Main/Expansion memory selector		C4
FIEF	H	P2B20			A4
INR	H	P2A27			A4
R3	H	[AB]	See sheet 4		
X15	H	[AW]	See sheet 6		
SHADR	H	P2B13	Short Address = [(F1=0)+(F1=2,8)·(Δ≠0)]		D3
JØP	H	P2B04			D1
JØP2	H	P2A05			D2
F23	H	[AN]			
N4	H	[AG]		5	

TIMING (Drawing number 89617000, sheet 5, cont'd.)

MAIN SEQUENCE FLIP-FLOPS

Outputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
RNI	H	P2A29	Read Next Instruction	5	D3
$\overline{\text{RNI11}}$	L	P2B27	RNI·ØDD·(F=0)	|	C2
$\overline{\text{RNI12}}$	L	P2B28	RNI·ØDD·(F≠0)	|	B2
$\overline{\text{RNI21}}$	L	P2B26	RNI·EVEN·(F=0)	|	B2
$\overline{\text{RNI22}}$	L	P2A25	RNI·EVEN·(F=0)	|	B2
$\overline{\text{ADR}}$	L	P1A31	Multicycle addressing	|	C1
RE1F	H	P2A19	RNI·EVEN·(Shift)	|	B2
$\overline{\text{RE18}}$	L	P2A26	RNI·EVEN·(F=0)·(F1=8)	|	A2
$\overline{\text{EAD}}$	L	P2B14	{Effective Address, End of Address	|	C1
ØP	H	P1A27	Operand 1	|	C1
ØPIND	H	P1B23	Operand Indicator	|	B1
$\overline{\text{ØPØ}}$	H	P2B06	$\overline{\text{ØP·ØDD}}$	|	B1
$\overline{\text{ØPE}}$	H	P2A04	$\overline{\text{ØP·EVEN}}$	5	B1

TIMING (drawing 89617000, sheet 5, cont'd.)

Description

The RNI state exists in every instruction. Each instruction begins with an RNI•ØDD cycle and ends with an RNI•EVEN cycle (refer to Timing, sheet 2 for an explanation of the signals ØDD and EVEN).

The ADR flip-flop is active in memory reference instructions while the effective address is being calculated. In some cases the entire effective address can be calculated during the RNI•ØDD cycle so the ADR state is not needed. This is referred to as SHort ADDRessing (SHADR).

The ØP flip-flop is usually active in memory reference instructions after addressing. It is also used in some register reference instructions. The ØP2 flip-flop is active before the ØP flip-flop during three instructions: RAO, SPE and CPB.

TIMING (drawing 89617000, sheet 5, cont'd.)

Circuit Description

The RNI, ADR, ØP2 and ØP flip-flops are all type J-K and are all clocked by JKCK (refer to Timing, sheet 2). ADR, ØP2 and ØP are reset by $(\overline{MPC} + \overline{ENI})$ where:

$\overline{MPC}$ is active during master clear and P register clear.

$\overline{ENI}$ is active during the enter interrupt sequence.

Thus when the computer enters an interrupt, the main sequence flip-flops are immediately cleared, except for RNI which is usually cleared later in the sequence.

RNI is set by $\overline{MPC}$ and therefore the RNI state already exists after master clear or P register clear, when the computer is set in operation.

The inputs of the RNI flip-flop, JRNI and KRNI are produced on the I/O Interface and the Console Interface assemblies.

The J input of the ØP2 flip-flop, JØP2, is produced on the I/O Interface assembly. The K input is connected to the signal ØDD. The J input of the ØP flip-flop, JØP, is also produced in the I/O Interface.

Thus the RNI, ADR and ØP2 states always finish at the end of an odd cycle while the ØP state can also terminate after an even cycle during multiply/divide instructions.

The J input of the ADR flip-flop is the signal:

$$RNI \cdot ØDD \cdot (F \neq 0) \cdot \overline{SHADR}$$

The K input is the signal:

$$KADR = ØDD \cdot (Counter = 0) \cdot [\overline{(FI = 4,6,C,E) \cdot 32KW \cdot X15}]$$

Thus the ADR state is entered after an RNI·ØDD cycle for memory reference instructions, as long as short addressing is not called for. The counter (Timing, sheet 4) is loaded during the RNI·ØDD cycle and decrements on following cycles.

TIMING (drawing 89617000, sheet 5, cont'd,)

When the counter reaches zero and ØDD is active, the ADR state will be terminated unless the computer is performing indirect addressing, or an interrupt sequence is entered during indirect addressing.

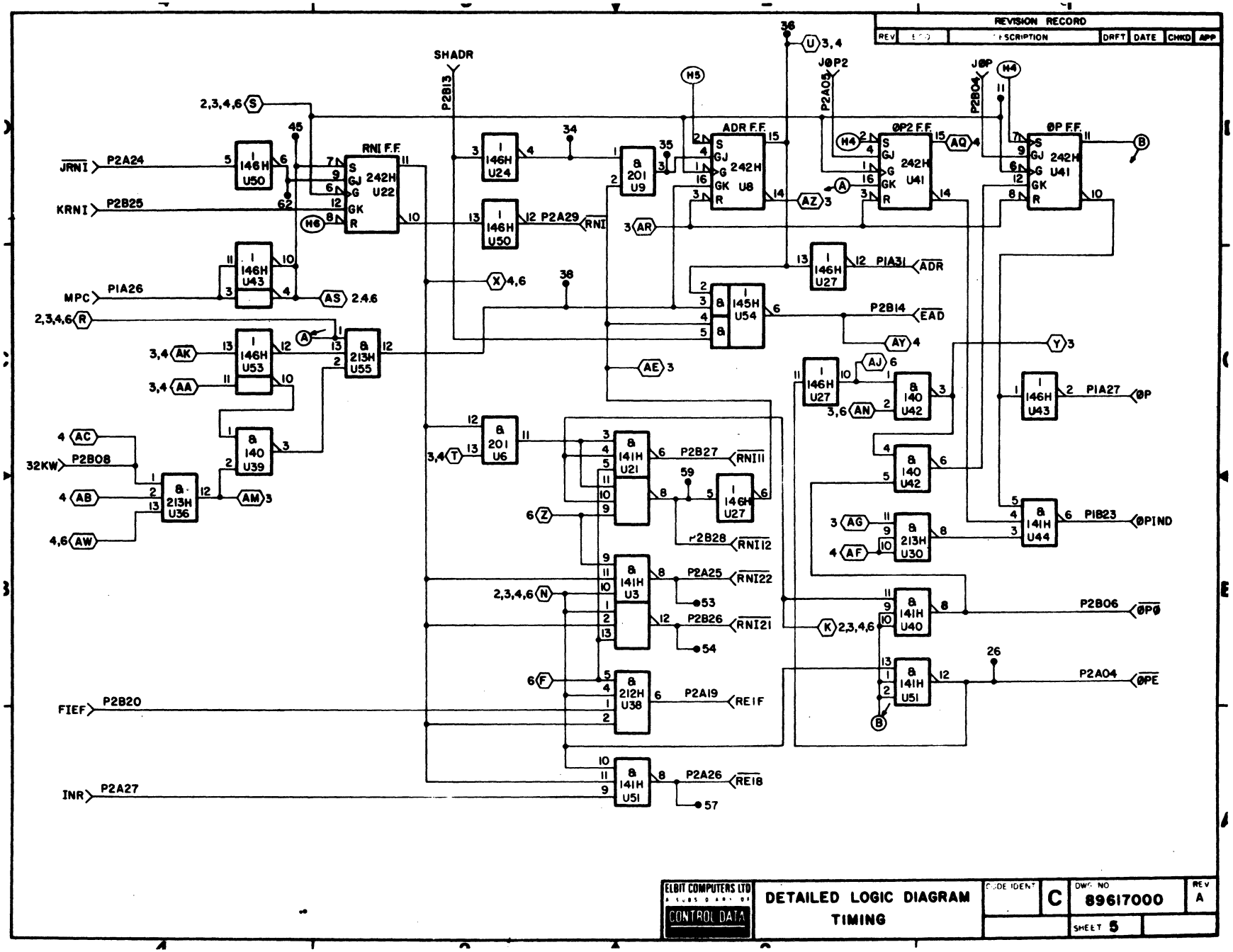
The signal $\overline{\text{EAD}}$ is active during the last cycle of addressing. It is used on Timing, sheet 4 and is also transmitted to the I/O Interface card Its equation is:

$$\overline{\text{EAD}} = \text{ADR} \cdot \text{KADR} + \text{SHADR} \cdot \text{RNI} \cdot \text{ØDD} \cdot (\text{F} \neq 0)$$

The signal ØPIND goes to the OPerand INDicator on the programmer's console. It is active during the following:

- operand and ØP2
- memory reference cycles of multiply/divide instructions (MD21)
- enter interrupt sequence (no main sequence flip-flop active).

The remaining signals in this section are produced by combining the main sequence signals with EVEN and ØDD and with signals decoded from the output of the instruction register.


REVISION RECORD
REV
DESCRIPTION
DRFT
DATE
CHKD
APP
SHADR
P2B13
RNI F.F.
ADR F.F.
ØP2 F.F.
ØP F.F.
JRNI P2A24
KRNI P2B25
MPC PIA26
FIEF P2B20
INR P2A27
32KW P2B08
P2B27 RNII1
P2B28 RNII2
P2A25 RNI22
P2B26 RNI21
P2A19 RE1F
P2A26 RE18
P2B14 EAD
PIA31 ADR
P2A29 RNI
P2A27 ØP
PIB23 ØPIND
P2B06 ØPØ
P2A04 ØPE
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
TIMING
CODE IDENT
C
DWG NO
89617000
REV
A
SHEET 5

TIMING (Drawing number 89617000, sheet 6)

AUXILIARY SEQUENCE FLIP-FLOPS

Function:

This section includes the flip-flops MDS, MDS1, ITR, X15 and FE0 and generates the corresponding signals.

Inputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
WXM	H	P1B15	Register clock selection	6	B4
WXL	H	P1B10			B4
WA	H	P1A14			A4
WM	H	P2B23			A4
WQ	H	P1B12			B3
WP	H	P1A13			B3
F23	H	P2B02	F = 2,3		C4
$\overline{\text{CHI}}$	H	P2B31			A4
$\overline{\text{Ø3}}$	H	P2A30	F≠3		B4
ØDD	H	[K],[R]	See sheet 2		
EVEN	H	[N]	See sheet 2		
XSEL7M	H	P1A02			C4
GØCS	H	[L]			
PG3(JKCK)	H	[E]	Phase 5 of clock		B3
CLRIR	H	P1A23	Clear Index Register		B3
DFE0	H	P1B01			B3
CNTE2	H	[P]	(Counter = 2)		
KITR	H	P2A23			D2
JITR	H	[AL]			
$\overline{\text{MDI}}$	H	[G]	(Counter=1)·(multiply)·$\overline{\text{ADR}}$	6	

TIMING (Drawing number 89617000, sheet 6, cont'd.)

Outputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
MDS	H	P2B30	Timing during multiply/divide instructions	6	C1
MDSO	H	P2A08			C1
MDSE	H	P2B03			C1
MDS1	H	P2A02			D3
MDS2	H	P1A28			D3
$\overline{\text{MD21}}$	L	P1B31			C4
$\overline{\text{W9A}}$	L	P2A01			A3
X15	H	P1B26			B3
BBCK	H	P1B30	Bucket clock		D3
ITR	H	P2B29	Timing for shift		D1
$\overline{\text{FEO}}$	H	P2B17	F = 0		B1
QCK	H	P1A11	Register clocks		B1
YCK	H	P1A12			A1
PCK	H	P1B13			A1
MCK	H	P2A22			A1
ALCK	H	P1B14			A1
AMCK	H	P2A11			A1
XLCK	H	P1A10			B3
XMCK	H	P1B09			B3
IRCK	H	P1A09		6	B3

TIMING (drawing 89617000, sheet 6, cont'd.)

Description

Signals MDS and MDS1 are active during multiply/divide instructions. During the ØP•EVEN cycle of multiply/divide, the counter (Timing, sheet 4) is loaded with 10110_2 (22_{10}). On the next cycle, the ØP state is not active, the counter decrements to 21_{10} and the signal MD21 defines the timing. MD21 is the J-input of the MDS1 flip-flop. MDS1 is active for the following two cycles and its K input is connected to the function MDS1 •ØDD. The MDS flip-flop becomes active immediately after MDS1 and remains active for 34 cycles. The K input is connected to the function CNTE2•ØDD where CNTE2 means "counter equals 2_{10}".

The MD21 signal is also combined with the fourth clock phase, signal PH4, to produce BBCK which is a clock to the bit bucket on the decoder card. The bit bucket is used to restore the sign of the result in multiply/divide instructions.

The ITR flip-flop (U22) is active during shift instructions. Its J and K inputs are produced on the I/O Interface board. The flip-flops MDS1, MDS and ITR are all clocked by the fifth phase clock signal JKCK and reset by MPC.

The X15 flip-flop (U64) always holds the most significant bit of the X register except during multiply/divide. Its D input is XSEL7M which is the input to the X register taken from the ALU assembly. Its clock is

$$PG3 \cdot WXM \cdot \overline{MDS1}$$

The FEO flip-flop (U64) stores the signal DFEO which is active when the F field of a word read from the memory is equal to zero. The predecoding for DFEO is on the Memory Control assembly. The clock to this flip-flop is:

$$IRCK = RNI \cdot EVEN \cdot PG3$$

TIMING (drawing 89617000, sheet 6, cont'd.)

IRCK is also used to clock the instruction register. The flip-flop is set by the signal CLRIR which clears the instruction register. Thus this flip-flop indicates whether the F field of the instruction register is zero.

Register Clocks

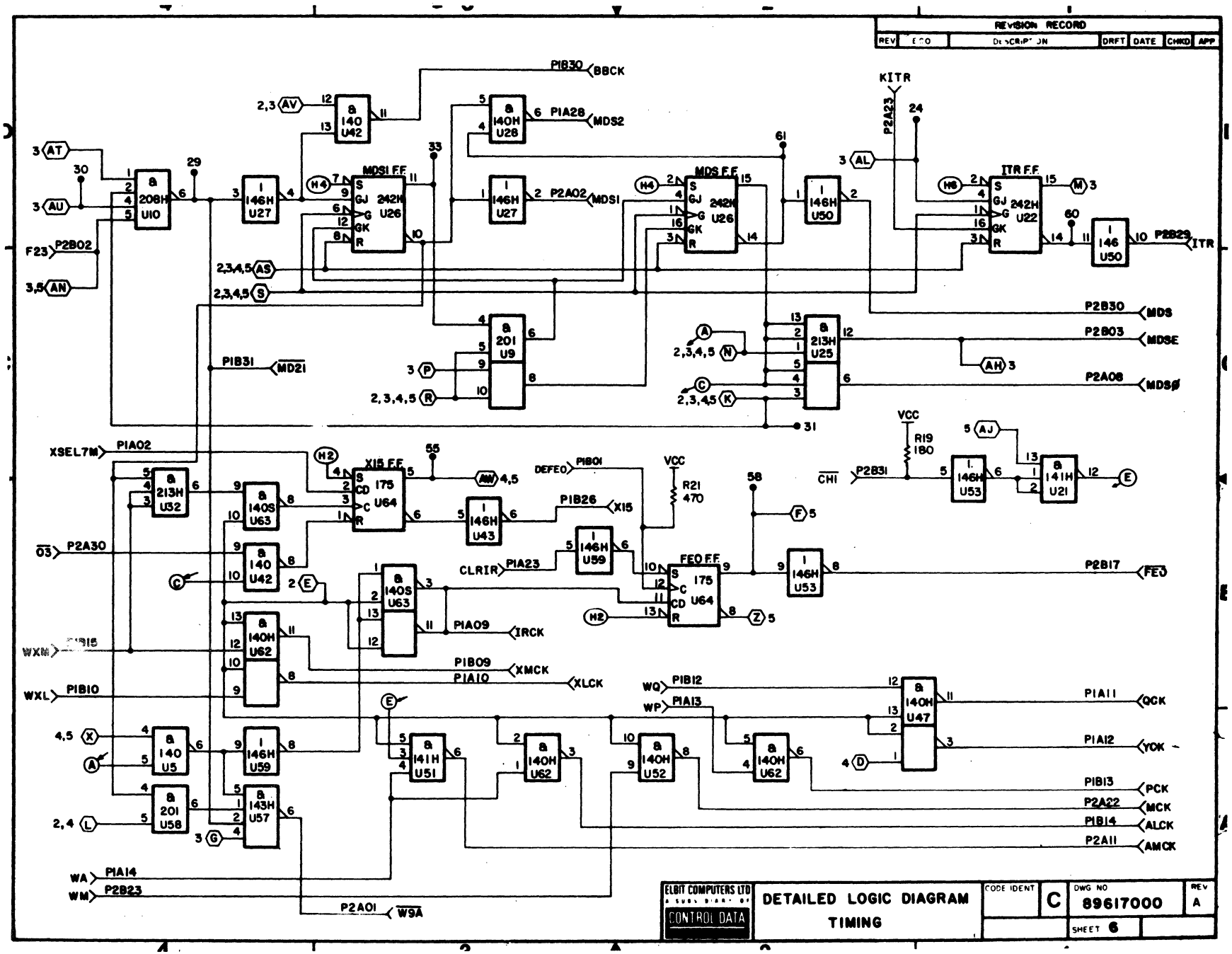
Clock signals for the registers in the ALU are produced in this section. The clock signals of the various registers are produced by multiplying JKCK (phase 5 of the clock)(Timing, sheet 2) with the appropriate signals (W):

Register	Q	P	Y	M	A	X
Signals for clock generation	WQ	WP	WY	WM	WA	WXM

The signal AMCK which clocks the most significant 8 bits of the A register can be blocked by the $\overline{CHI}$ signal. This is used by peripheral devices which transfer only 8 bits of data on each input on the A/Q channel.

The signal W9A is transmitted to the decoder card ALU/shifter. Its equation is:

$$W9A = RNI \cdot EVEN + MD21 + MD1 + MDS1 + \overline{GØCS}$$


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
P1B30 BBCK
KITR
P2A23
MDS1 F.F
MDS F.F
ITR F.F
P2B30 MDS
P2B03 MDSE
P2A08 MDSØ
P2B29 ITR
P1B31 MD2I
XSEL7M P1A02
X15 F.F
DEFEO P1B01
VCC
R19 180
R21 470
CHI P2B31
P1B26 X15
FEO F.F
P2B17 FEO
CLRIR P1A23
P1A09 IRCK
P1B09 XMCK
P1A10 XLCK
WXL P1B10
WQ P1B12
WP P1A13
P1A11 QCK
P1A12 YCK
P1B13 PCK
P2A22 MCK
P1B14 ALCK
P2A11 AMCK
WA P1A14
WM P2B23
P2A01 W9A
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
TIMING
CODE IDENT C
DWG NO 89617000
REV A
SHEET 6

"Pages 5-282 to 5-290 are unassigned."

INPUT/OUTPUT (I/O) INTERFACE

The I/O Interface circuits are accommodated on a single 50-PAK printed wiring board. The logic circuit diagram of the unit is given in drawing number 89619700, sheets 1-10.

The I/O Interface circuits generate control signals for the main input-output (A/Q) channel and for the circuits commanding the peripheral controllers. It also generates control signals for the CPU. This page lists the functional blocks accommodated on this board. The circuits and signals are described in detail on pages facing the corresponding sheets of the circuit diagram.

MAIN FUNCTIONAL BLOCKS

Designation	Shown on Sheet
A/Q channel control	2
Memory request logic	3
Index (i) address and write enable controls	4
Decoder for Fl field	5
Augend controls and X register clock control	6
Controls for shifter and A/Q channel direction	7
Main sequence flip-flop controls	8
Overflow logic	9
Enable-Interrupt logic	10

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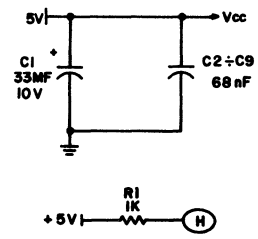
SHEET REVISION STATUS											
1	2	3	4	5	6	7	8	9	10	11
04	04	04	04	04	04	04	04	04	04	04
A	A	A	A	A	A	A	A	A	A	A

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
04	CK 323	REDRAWN PER CDC STD	R.S.	Nov 13		
05	CK 421	ADDITION OF TAGS TO CONNECT AND CORRECTION OF DRAWING ERRORS				
06	CK 626	CORRECTION OF DWG. ERRORS				
07	CK 785					
08	CK 1054	U 28 WAS IC 7400. RG ADDED FOR PNA 89791300 REV. 01				
A	CK 1174	RELEASED CLASS A				

ØFF SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SHEET LOCATION								
	2	3	4	5	6	7	8	9	10
A	C-4		D-1					C-3	C-3
B	D-3				D-2			C-3	C-3
D	C-3	C-4			B-4		C-2		
E	C-3	A-2			C-2		C-2		C-2
F	B-3		B-3		B-4				
G	B-2				D-4				
J	B-2								C-3
K	A-2	B-3	A-4		D-2	B-3			
L	B-1			C-2					
M	B-1			B-3					
N		D-4			C-3		C-2		
Q		D-4					B-1		
R		D-4					D-3		
S		D-4					C-3		
T		C-4						C-1	
U		B-4			A-3				
V		C-3	C-3						
W		B-4				C-3			
X		C-4	D-4	A-2	B-4				
Y		C-3					B-1	A-4	
Z		D-3					D-2		
AA		B-3					C-4		
AB		B-3	A-3	D-2				A-3	
AD		C-3	D-1			C-2		C-2	
AE									
AF		C-2	D-4		A-3		C-4		C-4
AG		C-2		D-3	C-4				
AJ		A-2	C-4		B-4		C-4		
AK		B-4		C-3		C-4	C-2		
AL		B-2					C-2		
AM		C-2					C-4		
AN		D-2		D-2			C-4		
AQ		D-2		C-3	C-2				
AR		C-1						C-2	
AS			D-4					C-4	
AT			D-4					A-4	
AU			C-4				C-4		



NØTES:

1) ALL RESISTØRS ARE 0.25 WATT 5%

2) THIS SHEET IS CØNTINUED ØN SHEET II.

AY 89791300
AW. 89791400
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL N/A

FINISH N/A

ELBIT COMPUTERS LTD
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CONTROL DATA

FIRST USED ON
AB107-A
AB108-A

DWN	RACHEL	Nov. 13. 73
CHKD	Uzi Levin	Dec. 5. 73
ENGR	DAVID WEISS	DEC. 5. 73
MFG	O.B. HAGAI	15 Nov. 73
APPR	HAIM J. ZA	3.17.75
Q.A		

TITLE
DETAILED LOGIC DIAGRAM
I/O INTERFACE

CODE IDENT C

DRAWING NO 89619700

SCALE

SHEET I OF II

8963300 A

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

OFF SHEET REFERENCE

OFF SHEET REFERENCE LETTER	SHEET LOCATION								
	2	3	4	5	6	7	8	9	10
AV			B-4				C-4		
AW			B-4		A-3				B-3
AX		C-4	B-4						
AY			A-4	D-3					
AZ	A-3			C-2					
BA	B-4								C-2
BB			D-3	C-4					
BD			A-3				C-2		
BE				D-2					C-3
BF				C-4	B-4				
BG				C-4	C-4				
BJ			A-4	C-3					
BK				B-3		C-3			C-4
BL				D-2	C-4				
BM				D-2					B-3
BQ				D-2				A-3	C-2
BR				A-1			C-3		
BS		D-3				C-3			
BT					B-3	C-2			
BU					D-3	B-3		B-4	
BV					C-2	C-3			
BW					B-2		B-4		
BX					D-2	B-2	D-4	B-4	
BY						B-4		A-2	
BZ						C-3	B-4		C-2
DA						A-2	D-2		
DB						B-3	D-4		
DD					C-3		A-4		
DE							D-4	D-2	
DG		D-2			B-2	C-4	B-3		
DH			C-2			B-4	D-3	B-4	
DS					B-3	C-4			
EA			D-3	C-4					
DP						B-2	D-3		

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM I/O INTERFACE	CODE IDENT C	DWG NO 89619700	REV A
			SHEET 11	

INPUT/OUTPUT (I/O) INTERFACE (drawing 89619700, sheet 2)

A/Q CHANNEL CONTROL

Function

This circuit controls the A/Q data channel. The A/Q data channel is used to transfer data, controller status, or controller instructions between a peripheral controller in the computer and the A register. The Q register defines the address of the peripheral controller.

This circuit transmits two control signals (READ, WRITE) to the peripheral controllers via the A/Q channel bus and receives one of two responses (REPLY, REJECT) from the controller addressed.

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
P4M	H	P2A21		2	D4
MC	L	P2A23		|	D4
$\overline{\text{REJECT}}$	L	P2A24		|	C4
$\overline{\text{REPLY}}$	L	P2B25		|	C4
RNI	H	P1B20		|	B4
JKCK	H	P2A19		2	B4

Outputs

RP	H	P2A22		2	B2
$\overline{\text{IRJ}}$	L	P2A25		|	C1
$\overline{\text{READ}}$	L	P2B02		|	B1
$\overline{\text{WRITE}}$	L	P2B01		|	B1
$\overline{\text{GØAQ}}$	L	P2A26		2	A1

(I/O) INTERFACE (drawing number 89619700,sheet 2 continued)

Description

The A/Q input/output sequence is initiated by the signal RN111•F1E23•JKCK (U2/12). This clears the A/Q flip-flop (U1/10) and clears the reply latch (U2/6, U2/8).

The output of the A/Q flip-flop gates the signal P4M through U3/8 to the count-up of the internal reject counter (U19). This is a four-digit binary up/down counter with a carry output. P4M is a clock signal generated on the memory control board with a repetition rate of approximately 0.88 µsec for the AB108, 1.30 µsec for the AB107.

The output of the A/Q flip-flop is ANDed with OP•EVEN•JKCK•FE0 to generate $\overline{\text{GØAQ}}$ at U51/8. Its function is to stop the basic timing chain in the ØP•EVEN state, with phase 4 and JKCK of the phase generator both high (see Timing sheet 2). $\overline{\text{GØAQ}}$ is also used to set the READ/WRITE latch (U20/3, U20/6). The output of the latch gates the output buffer-gates (U27/3, U27/11) to generate either a $\overline{\text{READ}}$ or a $\overline{\text{WRITE}}$ signal according to the code (R1 through R4) present on decoder U58 (refer to sheet 5). The $\overline{\text{READ}}$, $\overline{\text{WRITE}}$ signals control the direction of data flow in the A/Q channel.

The read/write latch (U20/3) gates the response signal (REPLY or REJECT) from the peripheral controller in reply to the signal READ or WRITE.

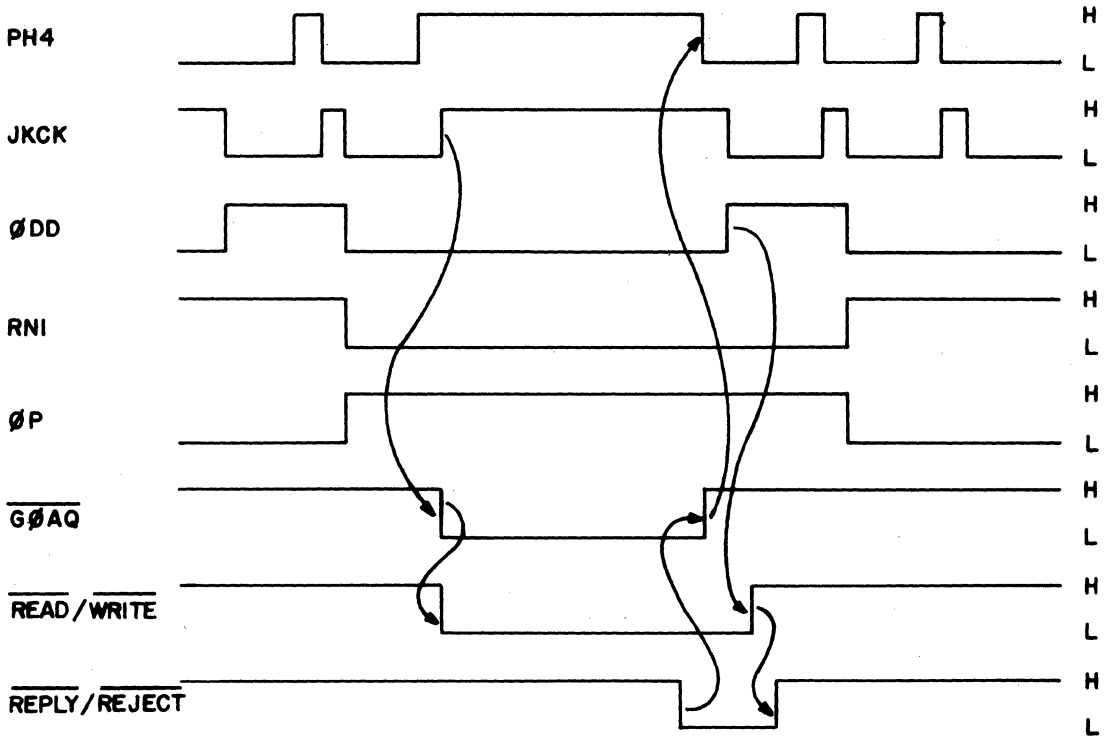
The timing chain remains stopped until a $\overline{\text{REPLY}}$ or $\overline{\text{REJECT}}$ is received from the channel. If no $\overline{\text{REPLY}}$ or $\overline{\text{REJECT}}$ is received within 12.8µsec in equipment AB108 (19.2 µsec in equipment AB107) of the Read or Write signal, an Internal Reject signal (IRJ) is generated at the carry output of the internal reject counter (P2A25).

(I/O) INTERFACE (drawing number 89619700, sheet 2, continued)

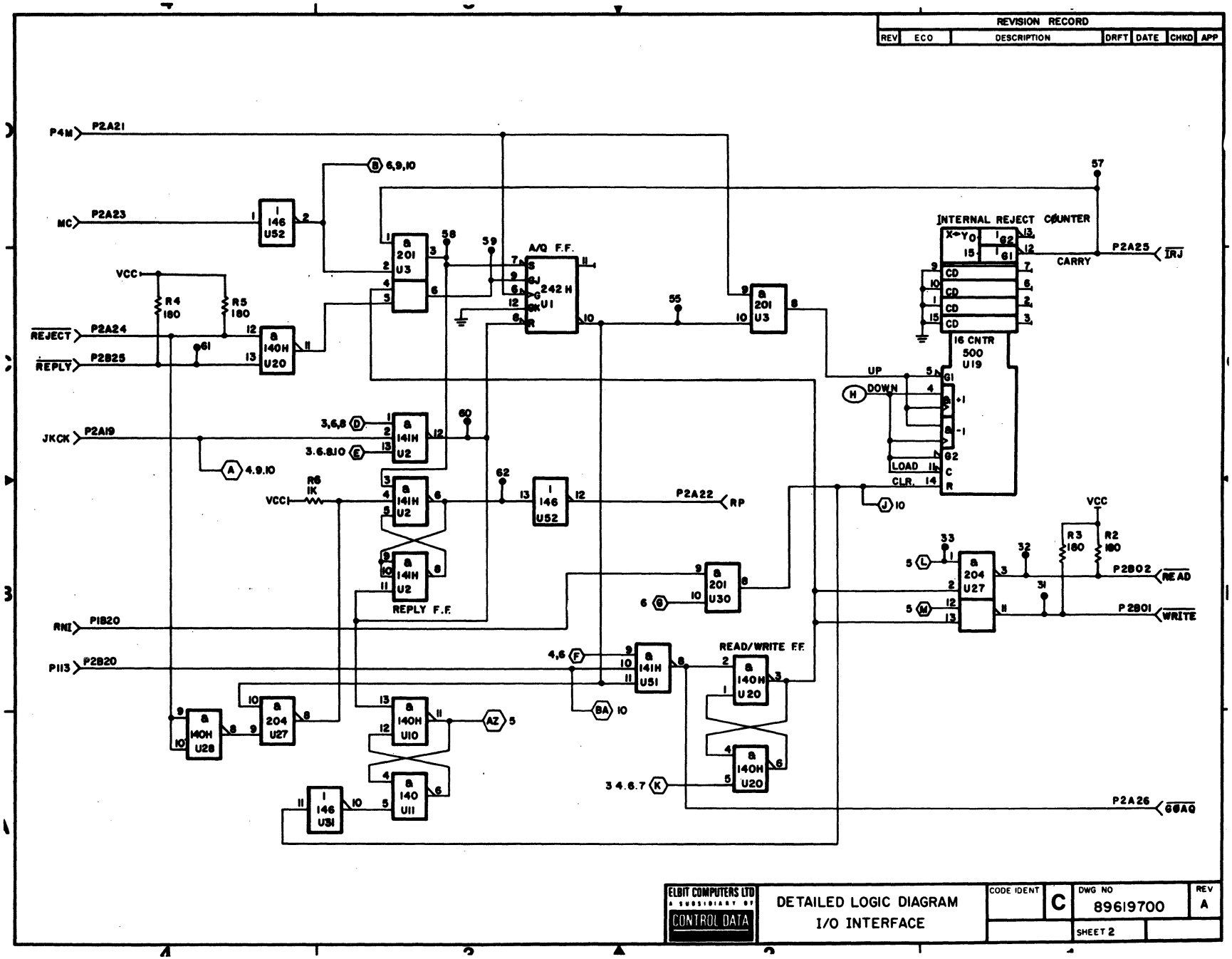
$\overline{IRJ}$ is transmitted to the Decoder and is also used to preset the A/Q flip-flop and clear the reply latch. The signal $\overline{GØAQ}$ goes high, allowing the timing chain to continue running. As the timing chain continues, the read/write latch is cleared by GØCS·$\overline{ØDD}$ and both $\overline{READ}$ and $\overline{WRITE}$go high. The computer increments the P register according to the state of signals $\overline{IRJ}$ and RP (both sent to the decoder). In the next CPU cycle, the internal reject counter (U19) is cleared by RNI·WRQ. The timing diagram of the sequence is shown below.

If a $\overline{REJECT}$ signal is received before the internal reject (IRJ) is generated, then $\overline{REJECT}$ resets reply latch U2, causing signal RP to go low. $\overline{REJECT}$ is also gated through U3/6 to set the A/Q flip-flop, which is clocked by P4M. Therefore, the input/output sequence terminates synchronously, as described above.

If a $\overline{REPLY}$ signal is received before the internal reject (IRJ) is generated, then $\overline{REPLY}$ is gated through U3/6 to set the A/Q flip-flop. The input/output sequence terminates as described above.



89633300 A



5-297/5-298

INPUT/OUTPUT (I/O) INTERFACE (drawing number 89619700, sheet 3)

MEMORY REQUEST LOGIC

Function

This circuit generates the memory request signal (MMRQ) to initiate the CPU memory cycle by way of the signal CRQ on the Timing assembly.

Inputs

Signal	Active	Signal Source/ Connector Pin	Function	Location Sheet	Location Square
$\overline{\text{ØP20}}$	L	P1A06		3	D4
ØDD2	H	P1A28	Second Odd Cycle		D4
$\overline{\text{EN120}}$	L	P1A05			D4
N41	H	P1B05			D4
ØP	H	P1B14			C4
$\overline{\text{ADR}}$	L	P2B22	Multicycle addressing		C4
$\overline{\text{ØDD}}$	L	P1B12	Odd Cycle		C4
FIE23	H	P1A20			B4
$\overline{\text{FEØ}}$	L	P1A18			B4
GØCS	H	P1A11			B4
$\overline{\text{RN112}}$	L	P2A06	RN1·ØDD·(F≠0)		A4
$\overline{\text{RN111}}$	L	P2B04	RN1·ØDD·(F=0)		A4
$\overline{\text{EN13}}$	L	P1A08		3	D2

Outputs

MMRQ	H	P1A07	Memory Request	3	C1
FIEF	H	P1B18		3	B1

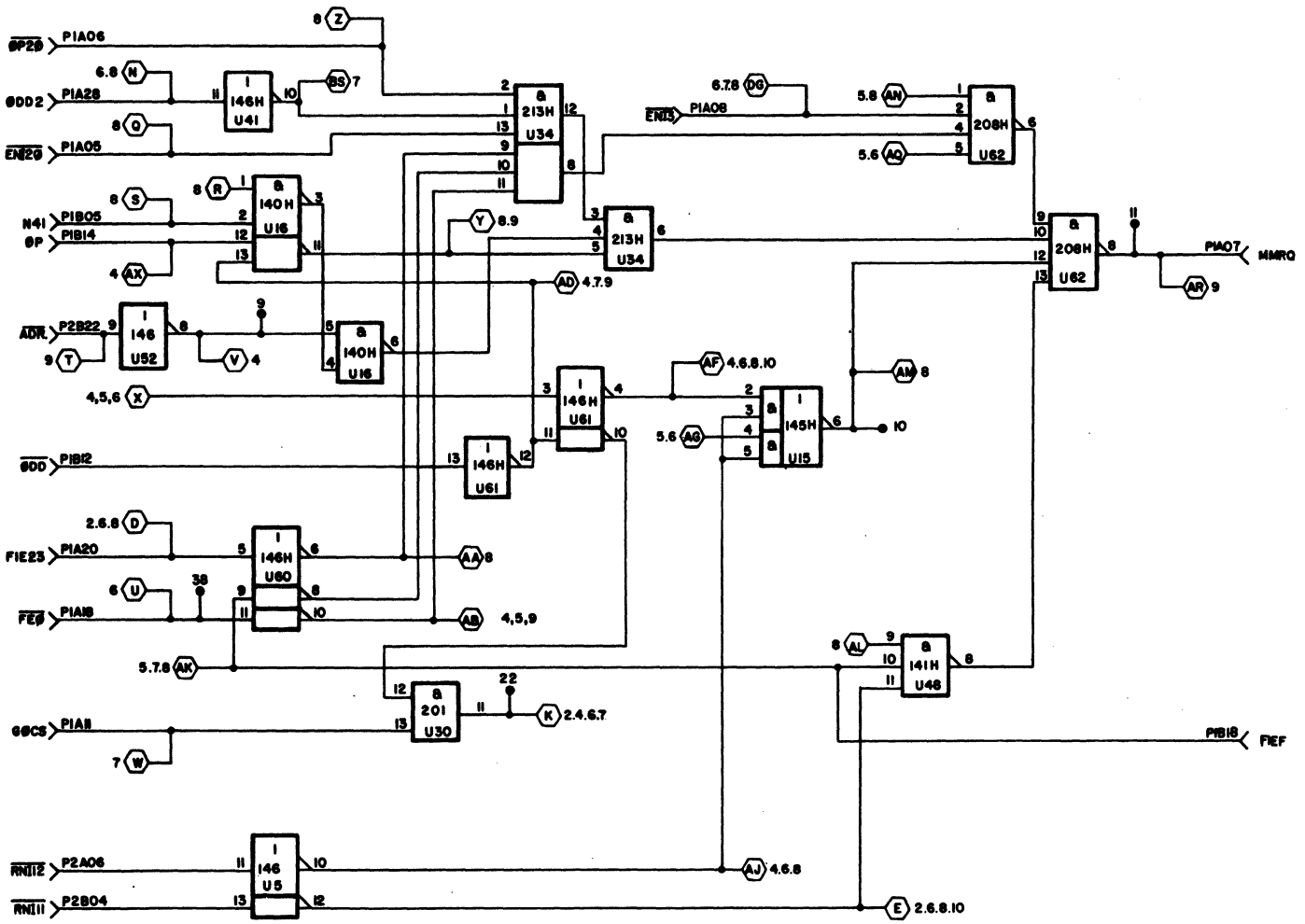
(I/O) INTERFACE (drawing number 89619700, sheet 3, cont'd.)

Description

The MMRQ signal is generated by high speed gates (series 74H) to conform to the constraints of the memory access time. The equation of the signal is as follows:

$$
\begin{aligned}
MMRQ = ADR\ & \overline{[N41 \cdot (F=2,3,8,9,A,B,C,E,F) \cdot (F1=1,2,3) \cdot DEL]} \\
& + \emptyset P \cdot \emptyset DD \\
& + \emptyset DD2 \\
& + \emptyset P2 \cdot \emptyset DD \\
& + EN12 \cdot \emptyset DD \\
& + RN1 \cdot \emptyset DD \cdot (F \neq 0) \cdot \overline{(F1=A) \cdot (\Delta \neq 0)} \\
& + RN1 \cdot \emptyset DD \cdot (F = 0) \cdot (F1EF) \cdot SH1 \\
& + (F=0) \cdot \overline{F1 = 1,2,3,E,F} \cdot \overline{EN13}
\end{aligned}
$$

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM I/O INTERFACE	CODE IDENT C	DWG NO 89619700	REV A
			SHEET 3	

INPUT/OUTPUT (I/O) INTERFACE (drawing number 89619700, sheet 4)

INDEX (i) ADDRESS AND WRITE ENABLE CONTROLS

Function

This circuit generates control signals for an index (i) address operation and Write Enable involving:

a. the second index register (location $00FF_{16}$)

b. the memory write cycle (signals WE, SPBM, CPBM, ØPST)

Inputs

Signal	Active	Signal Source/ Connector Pin	Function	Location Sheet	Location Square
X15	H	P2B17		4	D4
$\overline{\text{DEL}}$	L	P1A15			D4
$\overline{\text{CNTE2}}$	L	P1A17			C4
MPC	H	P2B15			C4
T3	H	P1A14			C4
T4	H	P1B16			C4
$\overline{\text{ØD}}$	L	P1B10			B4
$\overline{\text{ENTER}}$	H	P2B11			B4
$\overline{\text{EN12E}}$	L	P1B15		4	B4

Outputs

RIND	H	P2A17		4	D1
$\overline{\text{INDIND}}$	L	P2A08			C1
$\overline{\text{CRI}}$	L	P1A12	Index Register Address Control		C1
ØPST	H	P1A19			C1
$\overline{\text{WE}}$	L	P1B25			B1
$\overline{\text{SPBM}}$	L	P1A25	Set Protect Bit Indicator		
$\overline{\text{CPBM}}$	L	P1B17	Clear Protect Bit Indicator	4	

(I/O) INTERFACE (drawing number 89619700, sheet 4, cont'd.)

Description

The signal CRI is defined by:

$$\overline{CRI} = ADR \cdot CNTE2 \cdot (FI = 5,7,D,F) \cdot \overline{X15 \cdot 32KW}$$
$$+ [ADR \cdot CNTE2 \cdot DEL + RNI \cdot \emptyset DD \cdot (F \neq 0) \cdot \overline{DEL}] \cdot [FI = 1,3,9,B]$$

It is used on the Memory Address board to force the current memory reference to be made to the second index register (memory location $00FF_{16}$) rather than the address specified by the ALU lines (indirect addressing).

The output of the index flip-flop (RIND) controls the INDEX indicator on the Programmer's Console. It is active during the second pass of a CPU memory cycle in which the index location is addressed.

The signal INDIND = $ADR \cdot \overline{RIND}$ controls the INDIRECT ADDRESS indicator on the programmer's console. It is also used on the Console Interface board to determine the timing in which an interrupt is accepted (see JENI, console interface).

The signal $\overline{WE}$ is active when a CPU memory write cycle must be performed. It acts on circuits on the memory control board. Its equation is:

$$\overline{WE} = ENTER + ENI2 \cdot EVEN$$
$$+ \emptyset P \cdot (F = 4,5,6,7,D)$$
$$+ \emptyset P \cdot G\emptyset CS \cdot \overline{\emptyset DD} \cdot FE0 \cdot DEL \cdot (FI = 6,7)$$

(I/O) INTERFACE (drawing number 89619700, sheet 4, cont'd.)

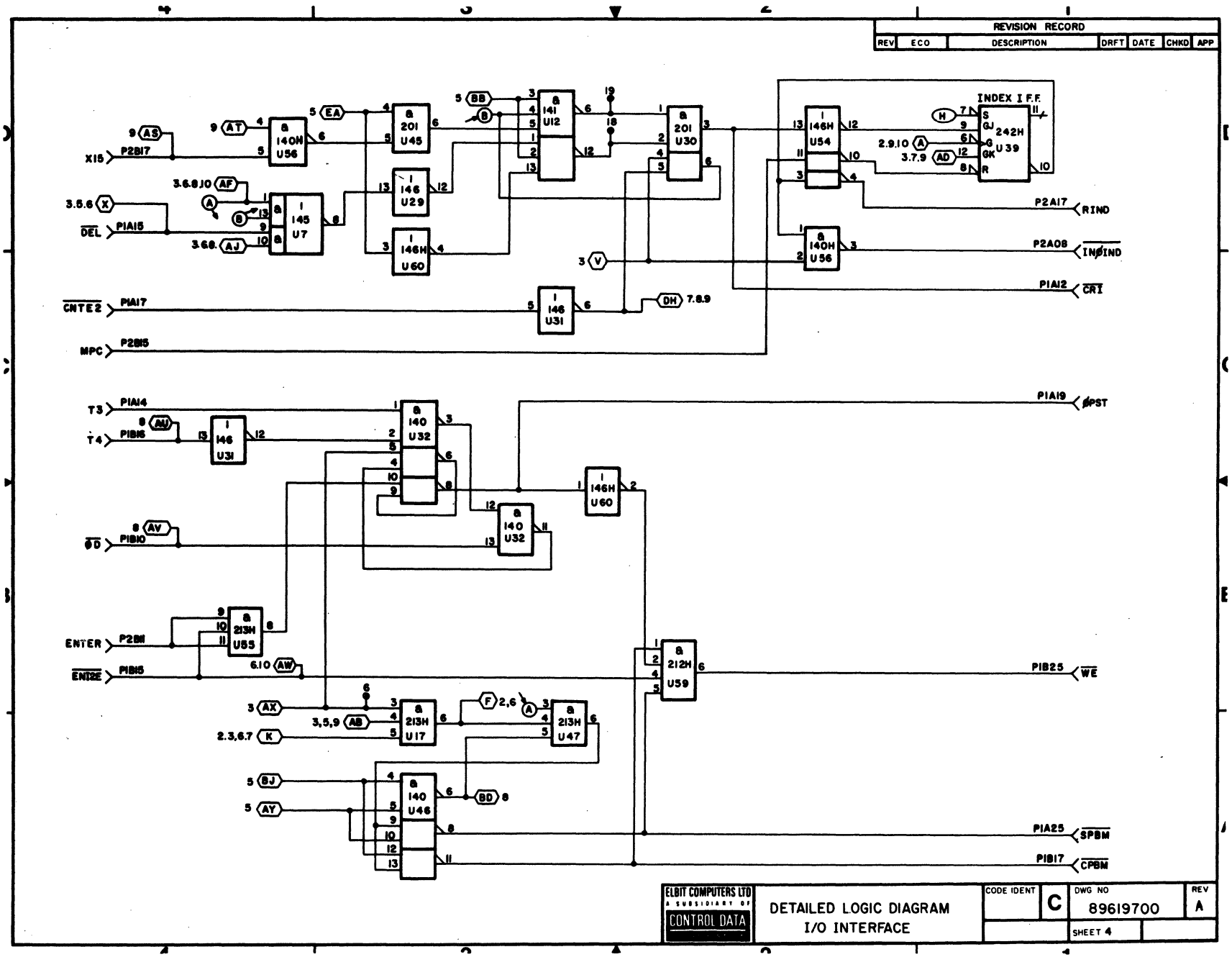
The signals $\overline{\text{SPBM}}$ and $\overline{\text{CPBM}}$ indicate that the computer is executing a "set protect bit" or "clear protect bit" instruction respectively. These signals are used on the memory address card to determine the polarity of the protect bit written back in the specified location. Their equations are as follows:

$$\overline{\text{SPBM}} = \text{ØP} \cdot \text{GØCS} \cdot \overline{\text{ØDD}} \cdot \text{FEO} \cdot \text{DEL} \cdot (\text{F1} = 6)$$

$$\overline{\text{CPBM}} = \text{ØP} \cdot \text{GØCS} \cdot \overline{\text{ØDD}} \cdot \text{FEO} \cdot \text{DEL} \cdot (\text{F1} = 7)$$

The signal ØPST is used by the breakpoint stop logic on the Programmer's Console to allow the computer to be stopped when executing a memory write cycle to a specified location. Its equation is:

$$\text{ØPST} = \text{ENTER} + \text{ENI2E} + \text{ØP} \cdot (\text{F} = 4,5,6,7,\text{D})$$


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
INDEX I F.F.
X15 P2BI7
DEL PIAI5
CNTE2 PIAI7
MPC P2BI5
P2AI7 RIND
P2A08 IN∅IND
PIAI2 CRI
DH 7.8.9
T3 PIAI4
T4 PIBI6
∅D PIBI0
PIAI9 ∅PST
ENTER P2BI
ENDE PIBI5
PIB25 WE
PIA25 SPBM
PIBI7 CPBM
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CONTROL DATA
DETAILED LOGIC DIAGRAM
I/O INTERFACE
CODE IDENT C
DWG NO 89619700
REV A
SHEET 4

INPUT/OUTPUT (I/O) INTERFACE (drawing number 89619700, sheet 5)

DECODER FOR F1 FIELD

Function

This circuit decodes the F1 field of the instruction register on the Decoder assembly (R1, R2, R3, R4), and generates control signals using these decoded signals.

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
R4	H	P1B22	F1 field	5	D4
R3	H	P1B19			D4
R2	H	P1A23			D4
R1	H	P1A24			D4
$\overline{\text{ENI4}}$	L	P1A10	Enter Interrupt indicator	5	B4

Outputs

IE	H	P1A22		5	D1
INR	H	P1B23			D1
IN0	H	P1B27			C1
IN32	H	P1B29			C1
IN41	H	P1A30			B1
SLS	H	P1B24	Selective Stop		B1
SHADR	H	P2A16	Short Address		A1
$\overline{\text{AQC}}$	L	P1A21	Q channel control (see sheet 7)	5	C1

(I/O) INTERFACE (drawing number 89619700, sheet 5, cont'd.)

Description

The decoder's (U58) 16 active-low outputs correspond to the instruction register F1 field codes (R1, R2, R3, R4). The following signals are generated with their aid and are transmitted to other boards:

The signal SHADR is active during memory reference instructions in which one CPU cycle (RNI•0) is enough to calculate the effective address (and therefore the ADR timing is not needed). It is used on this assembly as well as the Timing assembly to produce the control signals for the RNI and ADR flip-flops. Its equation is:

$$SHADR = (F1 = 0) + \overline{DEL} \cdot (F1 = 2,8)$$

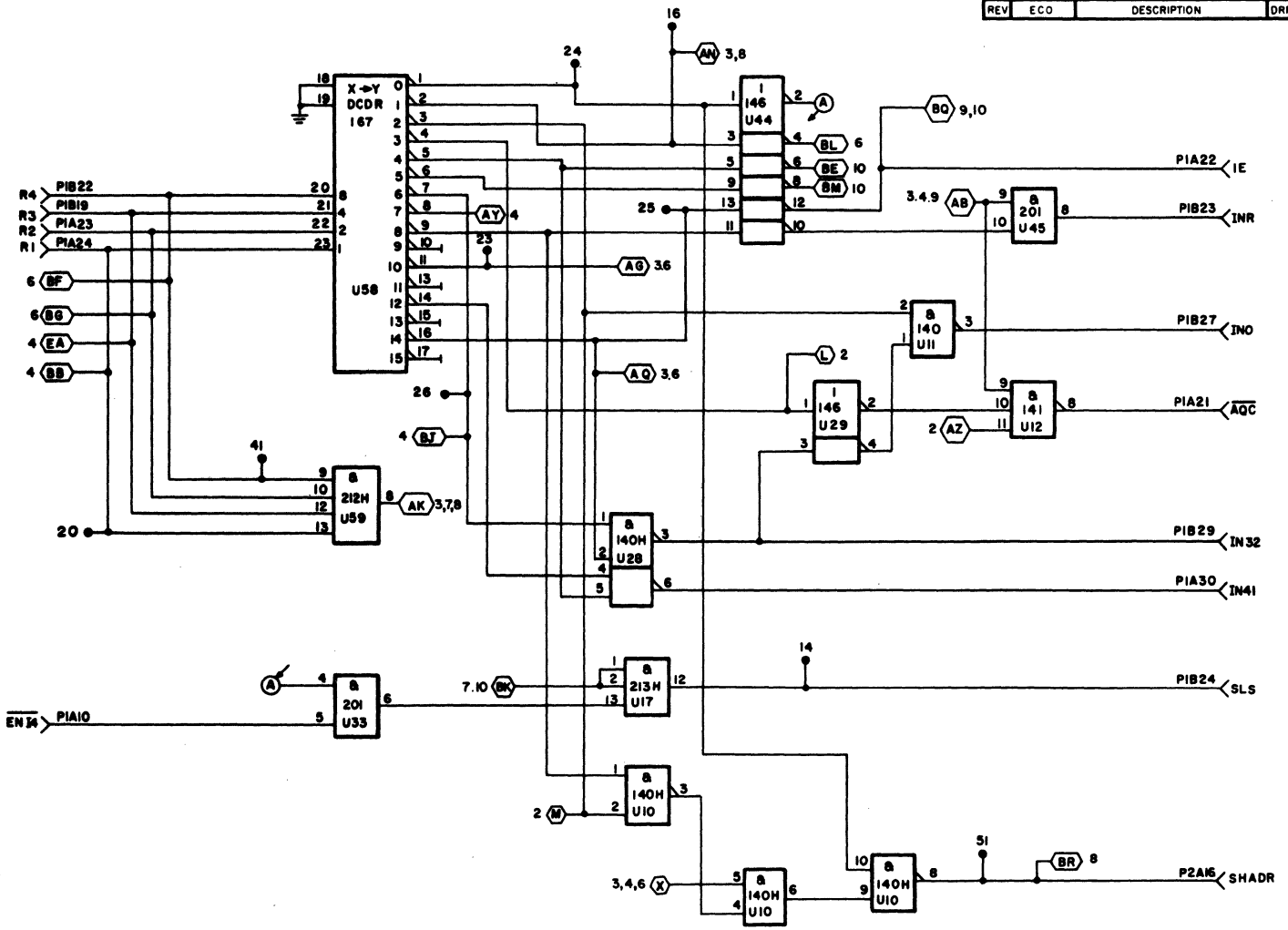
The signal SLS is sent to the programmer's console and stops the computer if the SELECTIVE STOP switch is set. Its equation is:

$$SLS = RNI \cdot EVEN \cdot (F = 0) \cdot (F1 = 0) \cdot \overline{EN14}$$

The signal $\overline{EN14}$ is produced on the Console Interface and is used to prevent the first cycle after an enter-interrupt from being interpreted as a selective stop. It is used here to generate SLS.
Other signals are:

$$IE = (F1 = E)$$
$$INR = FE0 \cdot (F1 = 8)$$
$$IN0 = (F1 = 2,6,E)$$
$$IN32 = (F1 = 6,E)$$
$$IN41 = (F1 = 4,C)$$

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM I/O INTERFACE	CODE IDENT	C	DWG NO 89619700	REV A
				SHEET 5	

INPUT/OUTPUT (I/O) INTERFACE (drawing number 89619700, sheet 6)

AUGEND CONTROLS AND X REGISTER CLOCK CONTROL

Function

This circuit generates:

a. augend controls not included on the Decoder assembly ($\overline{\text{DELTAUG}}$, SE, IM, SFL)

b. X register clock controls (WXL, WXM)

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
WRQ	H	P2A10		6	D4
F1E1	H	P1A27	F1 = 1		C4
SKT	H	P2A30	Skip condition		C4
$\overline{\text{CSX}}$	L	P1A31			B3
$\overline{\text{WXLT}}$	L	P1B28			B3
MDS2	H	P1B13		6	D2

Outputs

XEZ	H	P2A05	(X = 0)	6	C3
$\overline{\text{DELTAUG}}$	L	P2B30			C3
$\overline{\text{CLRQ}}$	L	P1B07	Clear Q register		D1
WXM	H	P2A07	X Register clock controls		C1
WXL	H	P2A15			C1
SE	H	P2A04			B1
SIM	H	P2A09			B1
SFL	H	P2B05		6	A1

(I/O) INTERFACE (drawing number 89619700, sheet 6, cont'd.)

Description

The augend gate controls are described together with the augend gates (ALU circuit, sheets 4,5). Their equations are as follows:

$$\overline{DELTAUG} = \overline{RNI \cdot \emptyset DD \cdot \emptyset DD2 \cdot (F = 0) \cdot (FI = 1) \cdot SKT}$$

This function is active during skip instructions when the skip condition (SKT) is met.

$$SE = ENI2 \cdot EVEN + RNI \cdot \emptyset DD \cdot (F = 0) \cdot FIE23$$
$$+ RNI \cdot \emptyset DD \cdot (F \neq 0) \cdot \overline{DEL} \cdot R4$$
$$IM = I7 + ENI2 \cdot EVEN$$
$$\overline{SFL} = ENI2 \cdot EVEN \cdot \overline{FE0} \cdot DEL$$

The X register clock control signals are used on the Timing assembly to produce clocks for the two ALU boards (WXL is associated with the ALU LSB, WXM with the ALU MSB). Their equations are as follows:

$$WXL = CSX + WXLI + EAD + ENI3$$

$$WXM = WXL + RNI \cdot \emptyset DD \cdot (F = 0) \cdot [(FI = E) + R4 \cdot I7]$$

where

WXLI comes from decoder (sheet 7)
EAD is produced on the timing card (see Timing, sheet 4)
and is active during the last cycle of the address calculation.

The signal XEZ is transmitted to the ALU circuit and controls the X register selector. When this signal is high, the X register receives memory data from the Memory Control board; when it is low, the X register receives data from the shifter. The equation is as follows:

$$XEZ = WRQ + RNI \cdot \emptyset DD \cdot (F = 0) \cdot (FI = 0,1,4,5,8,9,A,C,D)$$

(I/O) INTERFACE (drawing number 89619700, sheet 6, cont'd.)

The following signals are decoded from the F1 field of the instruction register:

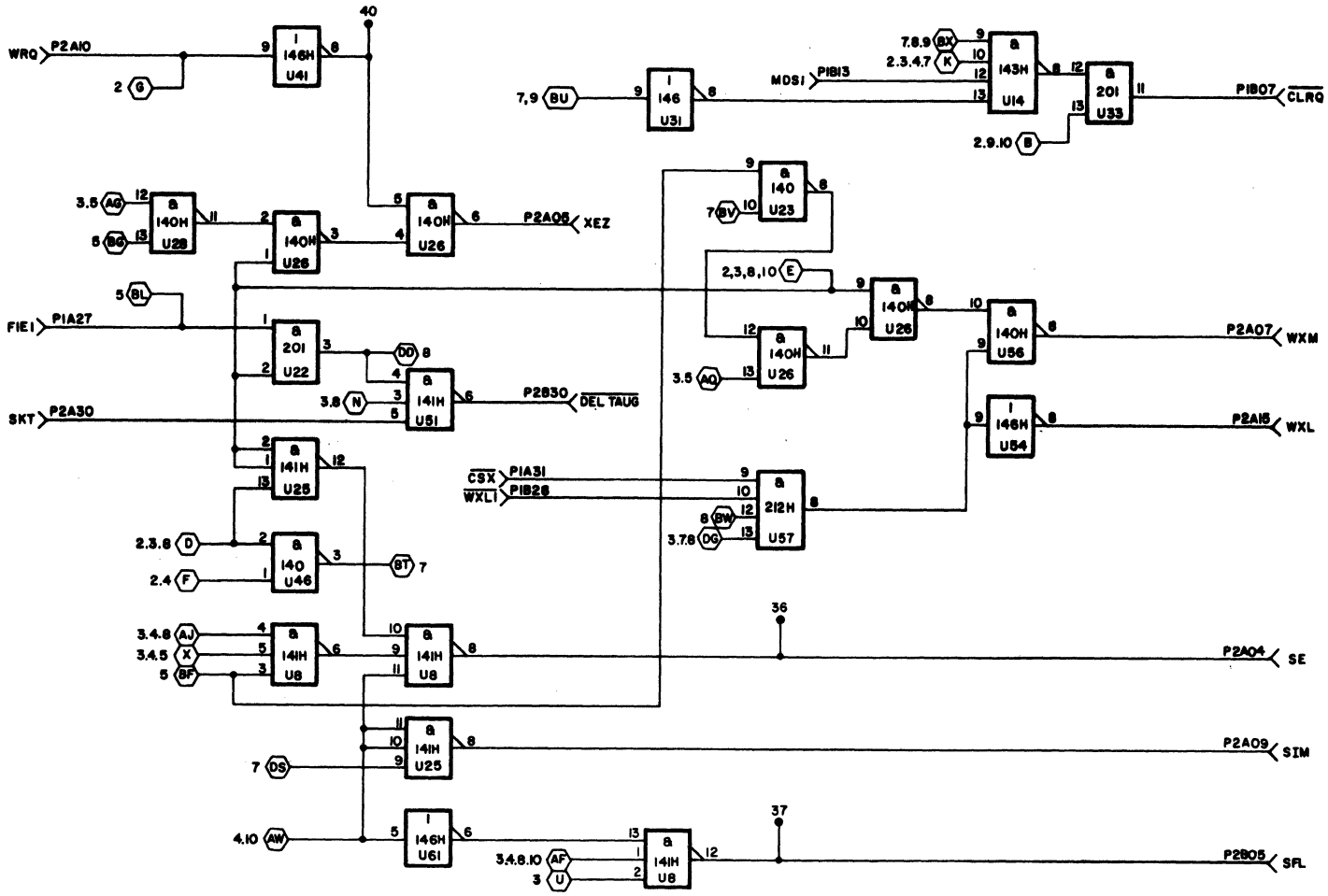
F1E1 = (F1 = 1), used in Console Interface circuit
F1EF = R1•R2•R3•R4, used in timing circuit

The signal $\overline{CLRQ}$ is transmitted to the ALU assemblies to clear the Q register. Its equation is:

$$CLRQ = MC + MDS2 \cdot \overline{MDS} \cdot EVEN \cdot \overline{03}$$

It is active during Master Clear and when the computer is running; it clears the Q register at the beginning of the multiply instruction execution.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM I/O INTERFACE	CODE IDENT C	DWG NO 89619700	REV A
			SHEET 6	

INPUT/OUTPUT (I/O) INTERFACE (drawing number 89619700, sheet 7)

CONTROLS FOR SHIFTER AND A/Q CHANNEL DIRECTION

Function

This circuit generates:

a. control signals for the shifter circuit (C0,C1,C2,C3,ZITSH)
b. signal AQC to control the direction of data flow on the A/Q channel.

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Location Square
I65	H	P1B02		7	D4
$\overline{I7}$	L	P1A01		|	C4
ITR	H	P1A02		|	C4
MDS	H	P1A03		7	B4

Outputs

ZITSH	H	P2B23		7	B3
$\overline{AQC}$	L	P1A21	A/Q channel Control	5	C1
C0	H	P1A04	Shifter Controls	7	C1
C1	H	P1B09		|	B1
C2	H	P1B01		|	B1
C3	H	P1B04		7	C1

(I/O) INTERFACE (drawing number 89619700, sheet 7, cont'd.)

Description

The shifter control signals are described with the ALU circuits (sheets 6,7). Their equations are as follows:

$$
\begin{aligned}
C0 &= MBS \cdot (F \neq 2) \cdot EVEN \cdot \overline{CNTE2} \\
&+ \overline{G\emptyset CS} \\
&+ MDS \cdot \emptyset DD \cdot (F \neq 2) \\
&+ ITR \cdot I7 \cdot I6 \cdot I5 \\
&+ EN I3 \cdot \overline{\emptyset DD2} \\
&+ \emptyset P \cdot EVEN \cdot FE0 \cdot F1E23 \\
&+ RN I \cdot \emptyset DD \cdot \overline{\emptyset DD2} \cdot (F = 0) \cdot (F1 = E) \\
&+ RN I \cdot EVEN \cdot (F = 0) \cdot (F1 = F) \cdot I7 \cdot I6 \cdot I5
\end{aligned}
$$

$$
\begin{aligned}
C1 &= \overline{G\emptyset CS} + EN I3 \cdot \overline{\emptyset DD2} \\
&+ MDS \cdot (F \neq 3) + ITR \cdot I7 \\
&+ RN I \cdot \emptyset DD \cdot \overline{\emptyset DD2} \cdot (F=0) \cdot (F1=E) \\
&+ RN I \cdot EVEN \cdot (F=0) \cdot (F1=F) \cdot I7
\end{aligned}
$$

$$
\begin{aligned}
C2 &= RN I \cdot EVEN \cdot (F=0) \cdot (F1EF) \cdot \overline{(I6\ I5)} \cdot \overline{I7} \\
&+ ITR \cdot \overline{I7} \cdot \overline{\emptyset DD \cdot I5 \cdot I6} \\
&+ \overline{[ITR + MDS \cdot \emptyset DD + MDS \cdot EVEN \cdot (F \neq 2) \cdot \overline{CNTE2} + EN I3 \cdot \overline{\emptyset DD2}} \\
&\quad \overline{+ RN I \cdot EVEN \cdot (F=0) \cdot (F1EF) + RN I \cdot \emptyset DD \cdot (F=0)\ (F1=E)\ \overline{\emptyset DD2}]}
\end{aligned}
$$

$$
\begin{aligned}
C3 &= \overline{G\emptyset CS} + ITR \cdot EVEN \cdot I7 \cdot I6 \cdot I5 \\
&+ \emptyset P \cdot EVEN \cdot (F=0) \cdot (F1E23) \\
&+ EN I3 \cdot \overline{\emptyset DD2} \\
&+ RN I \cdot \emptyset DD \cdot (F=0) \cdot (F1=E) \cdot \overline{\emptyset DD2}
\end{aligned}
$$

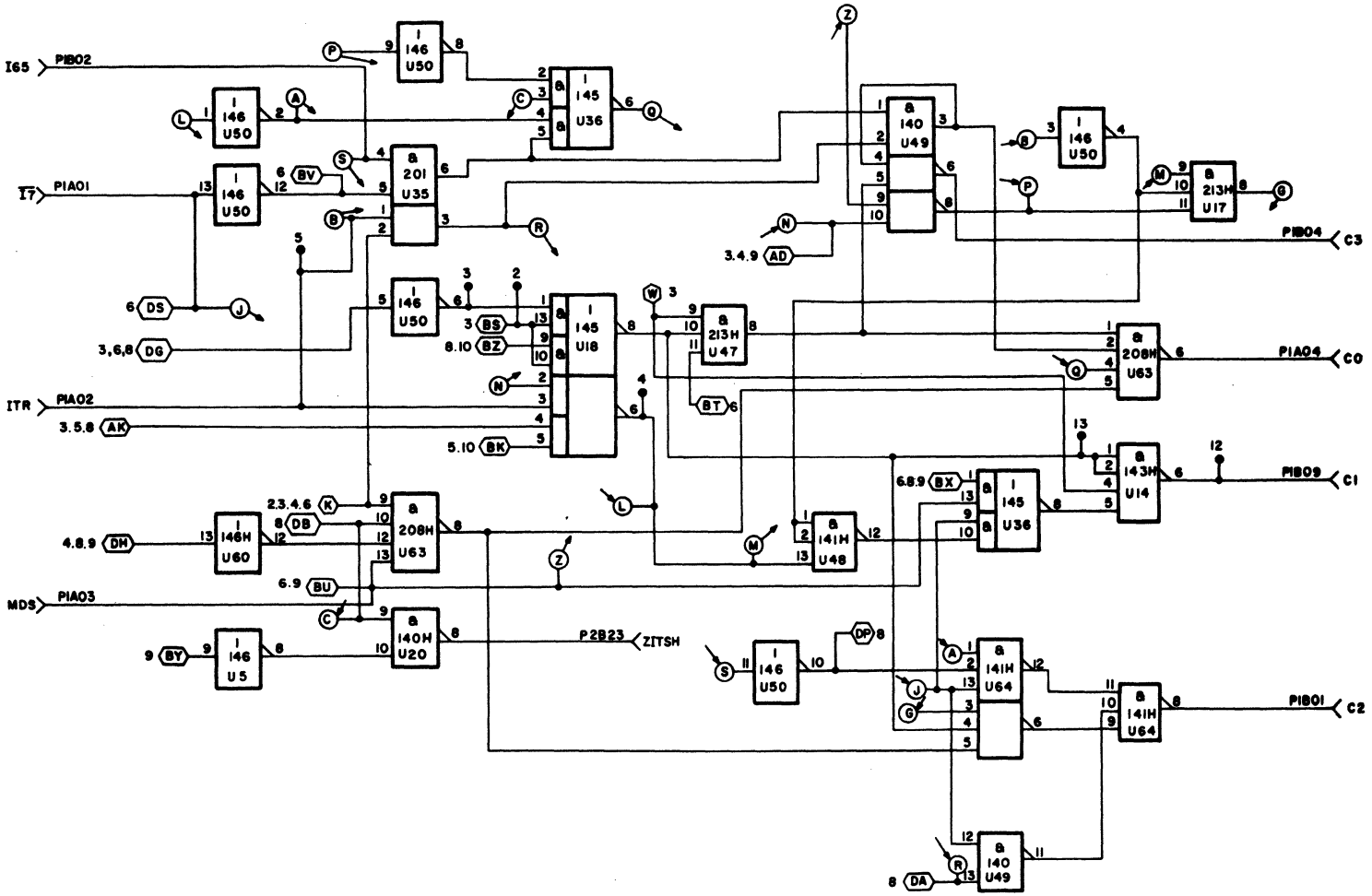
$$
\begin{aligned}
ZITSH &= ALU7M + (F=2) \\
&= ALU15 + (F=2)
\end{aligned}
$$

(I/O) INTERFACE (drawing number 89619700, sheet 7, cont'd.)

The signal AQC controls the direction of data flow from the ALU to the A/Q data bus or from the A/Q data bus to the ALU. Its equation is:

$$AQC = \emptyset P \cdot FE0 \cdot (F1 = 3)$$

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM I/O INTERFACE	CODE IDENT C	DWG NO 89619700	REV A
			SHEET 7	

INPUT/OUTPUT (I/O) INTERFACE (drawing number 89619700, sheet 8)

MAIN SEQUENCE FLIP-FLOP CONTROLS

Function

This circuit generates control signals for the main sequence flip-flops of the Timing circuit.

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Location Square
$\overline{02}$	L	P1B03		8	D4
$\overline{01}$	L	P2B16			C4
$\overline{EAD}$	L	P1A26			B4
$\overline{MDI}$	L	P2A11			D2
SHI	H	P1B06		8	C3

Outputs

JOP2	H	P2A18	Main Sequence flip-flop control	8	B2
KITR	H	P2B13			D1
JOP	H	P2B12			D1
KRNII	H	P2B14			C1
$\overline{JITR}$	L	P2A13			C1
$\overline{JRNI}$	L	P2B10			B1
EXT	H	P1B08			B1
F23	H	P2B08	(F=2)+(F=3)	8	D3

(I/O) INTERFACE (drawing number 89619700, sheet 8, cont'd.)

Description

The control signals for the main sequence flip-flops determine the state of the computer. They are described with the Timing circuits (sheets 5,6).

Other main sequence flip-flop controls are generated on the Timing and the Console Interface assemblies. The equations of the signals generated on this board follow:

$$\overline{JRNI} = \overline{\emptyset P \cdot \emptyset DD + EAD \cdot (F = 1) + EN12 \cdot \emptyset DD}$$

$$J\emptyset P = RNI \cdot \emptyset DD \cdot (F = 0) \cdot [(F1 = 2,3) + \emptyset DD2 \cdot (F1 = E)]$$
$$+ EAD \cdot (F \neq 1) \cdot (F \neq 0) + \emptyset P2 \cdot \emptyset DD$$
$$+ KITR + MD1$$

$$J\emptyset P2 = RNI \cdot \emptyset DD \cdot (F = 0) \cdot (F1 = 6,7) + EAD \cdot (F = D)$$

$$\overline{JITR} = \overline{RNI \cdot \emptyset DD \cdot (F = 0) \cdot (F1 = F) \cdot \overline{SHT}}$$

$$KITR = ITR \cdot EVEN \cdot [CNTE2 \cdot (16 \cdot 15) + N41]$$

The signal KRNI1 is transmitted to the Console Interface to produce the final RNI flip-flop signal, KRNI (refer to Console Interface sheet 5). Its equation is as follows:

$$KRNI1 = RNI \cdot \emptyset DD \cdot (F = 0) \cdot [(F1 = 2,3,6,7) + \emptyset DD2 \cdot (F1=E)] + JITR +$$
$$+ RNI \cdot \emptyset DD \cdot (F \neq 0) \cdot \overline{SHADR \cdot (F=1)}$$
$$+ EN13$$

The signal EXT is high when the ØDD state is to be extended for double cycle operation (ØDD·ØDD2, refer to Timing sheet 2). It is also employed during instructions which use an immediate operand for a memory reference. In this case the ØDD state is extended while the ØP state goes high, thus avoiding the ØP·EVEN state when this is not needed as the CPU does not have to wait for the operand from memory.

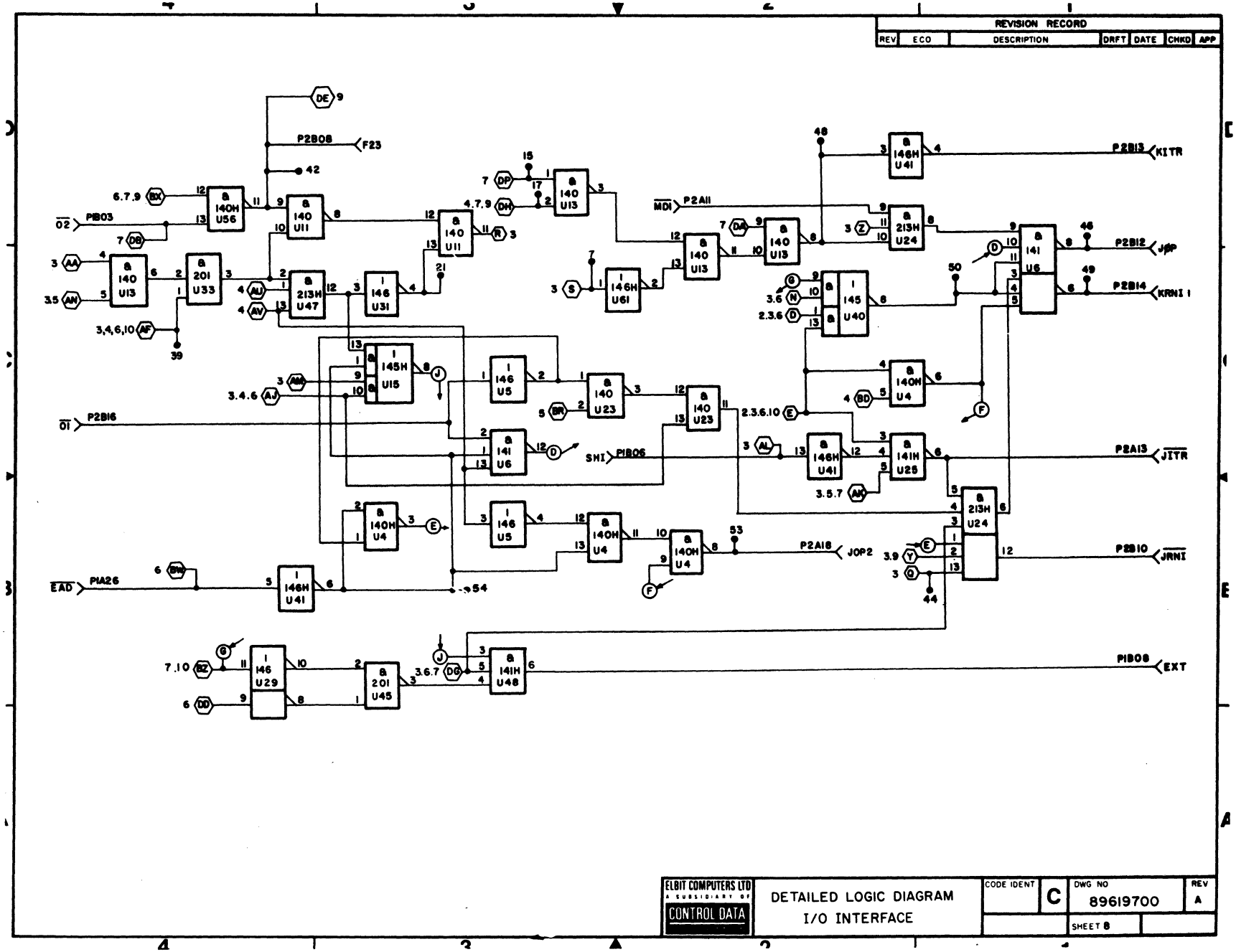
(I/O) INTERFACE (drawing number 89619700, sheet 8, cont'd.)

The equation of EXT is:

$$\begin{aligned} EXT = {} & EN13 + RNI \cdot \emptyset DD \cdot (F = 0) \cdot (FI = 1, E) \\ & + RNI \cdot \emptyset DD \cdot (F \neq 0) \cdot (FI = A) \cdot \overline{DEL} \\ & + EAD \cdot DEL \cdot (FI = 1,2,3) \cdot (F = 8,9,A,B,C,E,F) \end{aligned}$$

The signal F23 is transmitted to the timing board. Its equation is:

$$F23 = (F = 2) + (F = 3)$$


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
P2B08 F23
PIB03
P2A11 MDI
P2B13 KITR
P2B12 JPP
P2B14 KRNI
P2B16
P2A13 JITR
P2A18 JOP2
P2B10 JRNI
PIB06 SHI
PIA26 EAD
PIB08 EXT
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CONTROL DATA
DETAILED LOGIC DIAGRAM
I/O INTERFACE
CODE IDENT C
DWG NO 89619700
REV A
SHEET 8

INPUT/OUTPUT (I/O) INTERFACE (drawing number 89619700, sheet 9)

OVERFLOW LOGIC

Function

This circuit generates the overflow signal (ØVFL), for arithmetic operations in the computer.

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
KØVF	H	P2B19	Overflow flip-flop, K input	9	C4
BB	H	P2A27			B4
A7M	H	P2A20			B4
$\overline{03}$	L	P2B07			B4
32KW	H	P2A02			A4
SO	H	P2B26	Addition/Subtraction control		B3
ADD7M	H	P2B28			B3
AUG7M	H	P2A28			B3
ALU7AM	H	P2A29			A3
M	H	P2B03			C2
PTADD	H	P2B24		9	D3

Outputs

BX15	H	P2B27		9	C3
$\overline{ØVFL}$	H	P2A12			D1

(I/O) INTERFACE (drawing number 89619700, sheet 9, cont'd.)

Description

The state of the overflow flip-flop (U39/15) determines the overflow signal. Its output ($\overline{\text{ØVFL}}$: U41/2) is transmitted to the Programmer's Console (OVERFLOW indicator) and to the Console Interface.

The J input to the flip-flop is connected to the signal JØVFL (U38/8):

$$\text{JØVFL} = \overline{\text{MMRQ}\cdot\text{ØDD}\cdot\text{ADR}}\cdot\overline{(\text{F} = 2)}\cdot\overline{(\text{F} = 3)}\cdot\overline{\text{PTADD}}\cdot\overline{\text{M}}$$

$$\cdot(\text{AUG7M} \oplus \text{ALU7M})\cdot(\text{SO} \oplus \text{AUG7M} \oplus \text{ADD7M})$$

This restricts overflow to instructions in which arithmetic sums occur ADD, SUB, RAQ, ADQ, INQ and INR. The signal SO controls addition (high) and subtract (low) in the ALU. Thus during addition an overflow will occur according to the function:

$$(\text{AUG7M} \oplus \text{ALU7M})\cdot\overline{(\text{AUG7M} \oplus \text{ADD7M})}$$

Thus on overflow the two numbers being added have the same sign while the sum has the opposite sign.

During subtraction an overflow will occur according to the function:

$$(\text{AUG7M} \oplus \text{ALU7M})\cdot(\text{AUG7M} \oplus \text{ADD7M})$$

Thus the two numbers being subtracted have opposite signs; the subtrahend and difference also have opposite signs.

The K input, KØVF, is produced on the console interface card and is active during skip-on-overflow and skip-on-no-overflow instructions. The preset is connected to the signal (U40/6):

$$\text{ØP}\cdot\text{ØDD}\cdot\text{FEO}\cdot(\text{FI} = \text{E})\cdot\text{32KW}\cdot\text{X15} + [\text{ØP}\cdot\text{ØDD} + \text{MDS}\cdot\text{CNTE2}]\cdot(\text{F} = 3)\cdot\text{A7M}\cdot\text{JKCK}$$

(I/O) INTERFACE (drawing number 89619700, sheet 9, cont'd.)

Thus the overflow flip-flop is set during an exit-from-interrupt instruction when the computer is in 32K mode (Operator's Console switch 32K/65K) and the sign bit of the X register is set. The flip-flop is also set during a divide instruction if the quotient is too large for the A register.

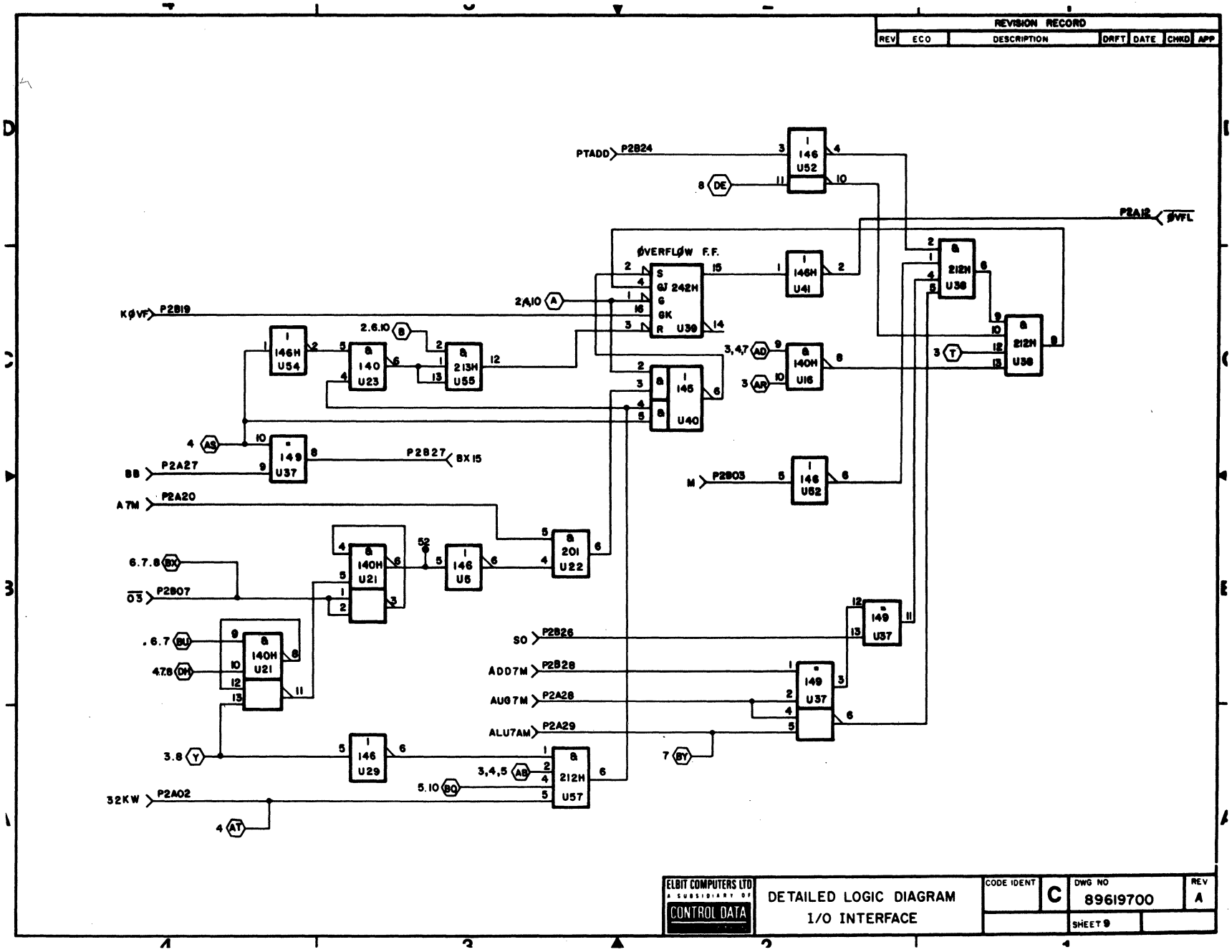
The overflow flip-flop is cleared by the signal (U55/12):

$$MC + \emptyset P \cdot \emptyset DD \cdot FE0 \cdot (F1 = E) \cdot 32KW \cdot \overline{X15}$$

Thus the flip-flop is cleared under the conditions for setting it, except that the sign bit of the X register is not set. It is also cleared by Master Clear (MC).

The signal BX15 is also generated in this circuit. It is transmitted to the decoder and is used during multiply/divide instructions. Its function is:

$$BX15 = BB \oplus X15$$


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
PTADD P2B24
8 DE
P2A12 ØVFL
ØVERFLØW F.F.
KØVF P2B19
2A,10 A
2.6.10 B
3,4,7 AD
3 AR
3 T
4 AS
BB P2A27
P2B27 BX15
M P2B03
A7M P2A20
6.7.8 BX
03 P2B07
.6.7 BU
4.7.8 BH
S0 P2B26
ADD7M P2B28
AUG7M P2A28
ALU7AM P2A29
7 BY
3.8 Y
3,4,5 AB
5.10 BQ
32KW P2A02
4 AT
U52
U41
U38
U39
U54
U23
U55
U40
U16
U37
U21
U6
U22
U29
U57
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CONTROL DATA
DETAILED LOGIC DIAGRAM
I/O INTERFACE
CODE IDENT C
DWG NO 89619700
REV A
SHEET 9

INPUT/OUTPUT (I/O) INTERFACE (drawing number 89619700, sheet 10)

ENABLE-INTERRUPT LOGIC

Function

This circuit generates the Enter-Interrupt signal (EINT).

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
$\overline{\text{RNI21}}$	L	P1B26		10	C4
PH3	H	P2B20		10	C2
PH2	H	P2B29		10	C3

Outputs

EINT	H	P2B18		10	B1

Description

When signal EINT is active high it indicates that the interrupt system is enabled. It is transmitted to the Console Interface assembly and to the Programmer's Console (INTRPT ENABLE indicator). The signal is generated by the two EINT flip-flops (U53) and associated gates. The EINT1 flip-flop (U53/15) is set after the RNI•EVEN cycle of the EIN instruction. It is controlled by the signal of its J-input:

$$JEINT1 = RNI \cdot EVEN \cdot (F = 0) \cdot DEL \cdot (F1 = 4)$$

The equation for its K input is:

$$KEINT1 = RNI \cdot WRQ$$

The EINT2 flip-flop (U53/10) is set by EINT1•RNI•WRQ•PH2. Thus EINT becomes active during the last CPU cycle of the instruction that follows the EIN instruction.

The J input of the EINT2 flip-flop is connected to the signal

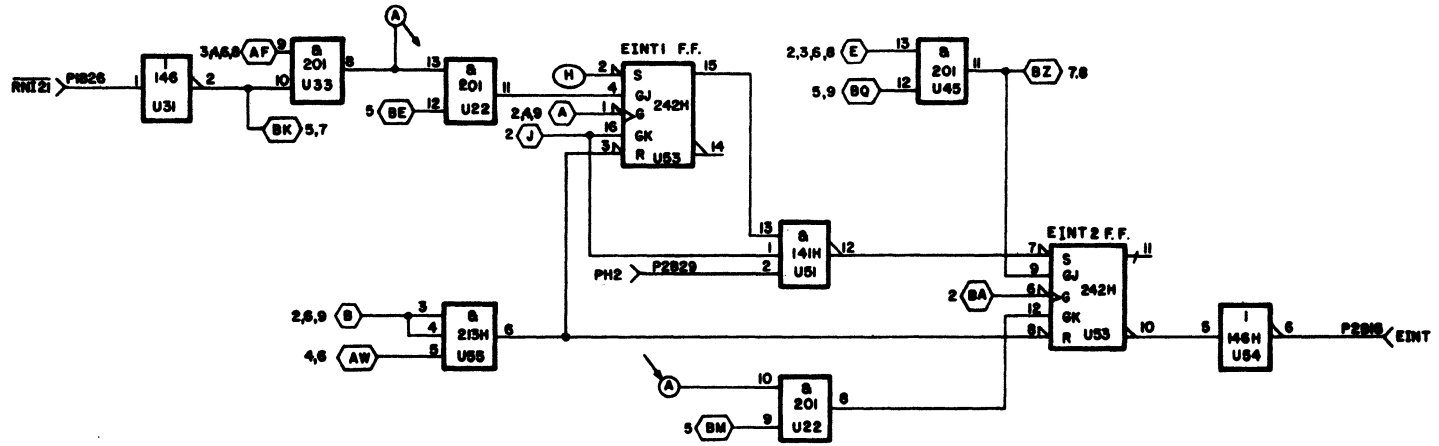
$$RNI \cdot \emptyset DD \cdot (F = 0) \cdot (F1 = E)$$

Thus the interrupt system is enabled immediately after an exit interrupt instruction. The K input is connected to:

$$RNI \cdot EVEN \cdot DEL \cdot (F = 0) \cdot (F1 = 5)$$

Thus the interrupts are disabled immediately after an EIN instruction. The EINT flip-flops are clocked by PH3 and cleared by Master Clear and EN12•EVEN. This inhibits the interrupt system when the computer enters the interrupt state.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM I/O INTERFACE	CODE IDENT C	DWG NO 89619700	REV A
			SHEET 10	

"Pages 5-330 to 5-336 are unassigned."

CONSOLE INTERFACE

The Console Interface circuits are accommodated on a single 50-PAK printed wiring board. The logic circuit diagram of the unit is given in drawing number 89618800, sheets 1 to 7.

The Console Interface accommodates the circuits which interface the Programmer's Console and the CPU. It also generates some of the auxiliary controls for the CPU. This page lists the functional blocks accommodated on this board. The circuits and signals are described in detail on pages facing the corresponding sheets of the circuit diagram.

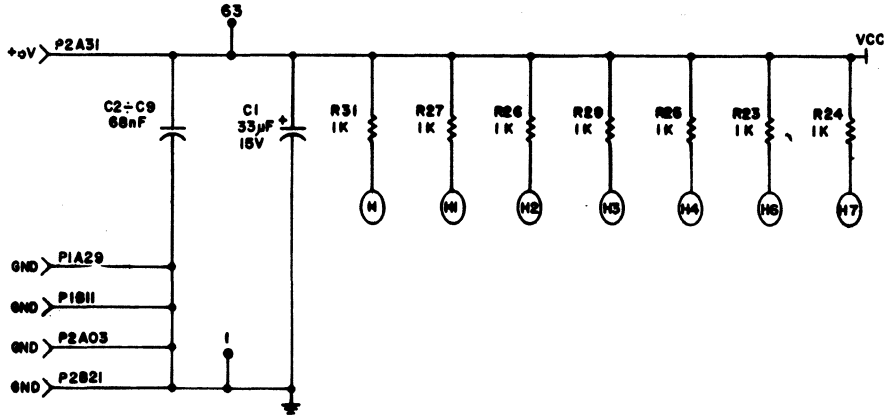
MAIN FUNCTIONAL BLOCKS

Designation	Shown on sheet
Start/Stop sequence flip-flops	2
Program protect logic	3
Test mode and autorestart	4
ALU logic	5
Enter interrupt logic	6
Skip logic	7

5-338

ØFF — SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SHEET LOCATION 2	3	4	5	6	7
A				D-2		B-3
B				D-2		B-3
D		C-2				C-3
E					C-3	D-2
F	C-2	D-4				C-2
G					D-3	C-4
K	B-1	C-4	D-4		D-3	C-3
L		A-1			A-2	C-3
M	D-3		D-4		B-3	D-4
N		B-2				D-3
P		C-3				D-4
Q	D-3	A-				
R	B-3	C-3				
S	A-2	D-3				
T	C-2				C-3	
U	C-4				B-2	
V	D-2				C-3	
W	B-4	A-2				
X	D-2		C-4			
Y		C-3			A-3	
Z	D-4	C-4			A-3	
AA	C-4		C-4			
AB	D-4		B-1			
AC	C-4		C-4			
AD	A-4		C-1			
AE		D-4			A-3	
AF		A-4			C-3	
AG		C-4			B-3	
AH		A-2			C-3	
AK		D-2			A-3	
AL		B-3			A-3	
AM		D-4			D-2	



NOTE : ALL RESISTORS ARE 0.25 WATT, 5%

SHEET REVISION STATUS

1	2	3	4	5	6	7	
06	06	06	06	06	06	06	
01	07	07	07	07	07	07	
08	08	08	08	08	08	08	
09	09	09	09	08	09	09	
10	10	10	09	10	10	10	
A	A	A	A	A	A	A	
B	B	A	A	A	A	A	

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
06	CK 344	REDRAWN PER CDC STD	Dyan & Nomi	Dec. 9-13 Jan. 6-74		
07	CK 421	ADDITION OF TAGS TO PUNCT.				
08	CK 640	CORRECTION OF LOGIC ERRORS: SH3 : U24-1, P2A23 SH 5 : P2B20, P2A20 SH 6 : P2A28, U21-13, U21-2	Dyan	May, 23 74		
09	CK 783	FITS ASSY 89836700 REV 01 FITS PWB 89836600 REV 01 U9-3 CUT FROM U25-4 GATE U33-1,2,4,5,6 ADDED AT U25-4 AY WAS 89618900; AY WAS 89618600	01,02 Dyan	19 July 74		
10	CK 785	CORR DWG ERRORS	Dyan	AUG 19 74		
A	CK1178	RELEASED CLASS A All +5V Regd. by VCC	MLP	3 April 75	Kenel	
B	CK 1328	ADD C10, INF FROM P2A04 TO GND	MLP	25 JUN		

AY 89836700
AW 89836600
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL N/A

FINISH N/A

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DWN	Dyan S.	NOV-10
CHKD	Aubrey Kagan	Dec. 9
ENGR	DAVID WEISS	DEC. 9, 73
MFG	O.Q ADELA	MAY 75
APPR	HAIM T.	MAY 75
D.A.	T Kalmann	5 May 75

FIRST USED ON
AB 107-A
AB 108-A

TITLE
DETAILED LOGIC DIAGRAM
CONSOLE INTERFACE

CODE IDENT C

DRAWING NO 89618900

SCALE

SHEET 1 OF 7

8963300 D

CONSOLE INTERFACE (drawing 89618800, sheet 2)

START/STOP SEQUENCE FLIP-FLOPS

Function

This circuit works in conjunction with the Timing board. It produces the signals for starting and stopping timing sequences under control of signals from the Programmer's Console and from other computer control circuits.

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Location Square
RNI	H	P1A17	Read Next Instruction	2	D4
$\overline{\text{INT•SW}}$	L	P1B16			D4
$\overline{\text{STØPCS}}$	L	P1A16			D4
PRGST	H	P1A18			D4
$\overline{\text{MCCS}}$	L	P2B27			C4
GØCS	H	P2A05			C4
NØRMAL	H	P2A11	Normal/Power fail indicator		C4
$\overline{\text{PCL}}$	L	P2A22			C4
$\overline{\text{ØDD}}$	L	P1B13	Odd cycle		B4
JKCK	H	P2B18	Last phase of clock		B4
$\overline{\text{CRQ}}$	L	P1B25			A4
MPRY	H	P2A12	Parity signal		A4
$\overline{\text{GØCSW}}$	L	P2A04		2	A4

CONSOLE INTERFACE (Drawing 89618800, sheet 2, cont'd.)

Outputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
$\overline{MC}$	L	P2A27	Master Clear	2	D1
MC	H	P2B29	Master Clear		D1
SSI	H	P1B15			D1
$\overline{SGI}$	L	P2A13	Start timing chain		C1
$\overline{FS}$	L	P1A27			C1
MPC	H	P2B22			C1
TP	H	P2B28			B1
WRQ	H	P1A11	Memory Request		B1
PRY	H	P2B25		2	A1

Description

The Timing chain is started by the signal SGI (see Timing sheet 2). SGI is generated in the GØ flip-flop (U22/5). This is set by the positive edge of its clock input. This signal may be produced by $\overline{GØCSW}$ from the Programmer's Console or by the test mode logic (sheet 4). Two clock pulses after the $\overline{SGI}$ signal is received by the Timing assembly, the GØCS signal becomes active. This resets the GØ flip-flop. Alternatively the GØ flip-flop can also be reset by MPC = MC + PCL.

The timing chain, and therefore the computer, is stopped by the signal SSI produced by the stop flip-flop (U23/8). The stop flip-flop is set by the following signals:

$$WRQ\ (RNI \cdot INST + STOP \cdot CS + PRGST \cdot \overline{FS}) + MCCS + MCT$$

where

- WRQ is active during the second CPU memory cycle (see below). This flip-flop is clocked by the signal PH3 from the Timing assembly phase-generator.

According to this equation the flip-flop is set (and the computer stops)

- at the beginning (Phase I of RNI•ØDD) of the next instruction with the instruction stop switch set
- at phase I of the ØDD that follows the first WRQ with the CYCLE step or the STOP pushbutton set
- when the PRGST signal from the Programmer's Console is active
- at phase I of the first ØDD cycle after the master clear is pressed
- or when a signal is received from the test mode logic.

The stop flip-flop is cleared by MPC and preset by the NORMAL signal from the Memory Control assembly.

The First Step signal (FS: U23/5) is active high during

- the first memory cycle after a master clear or P register clear
- after P clear
- after an aborted enter-interrupt sequence, (see sheet 5).

The signal is preset by MPC + KEN11•JKCK and clocked by EVEN•PH3. This signal causes the CPU to request the memory according to the address P (instead of P + 1) in the following cases:

- while reading first instruction when starting to operate program
- when first enter/sweep is executed
- when the ENI sequence is aborted and the CPU has to call again on the instruction located in address P.

The Master Clear signal MC (U30/6). Its equation is:

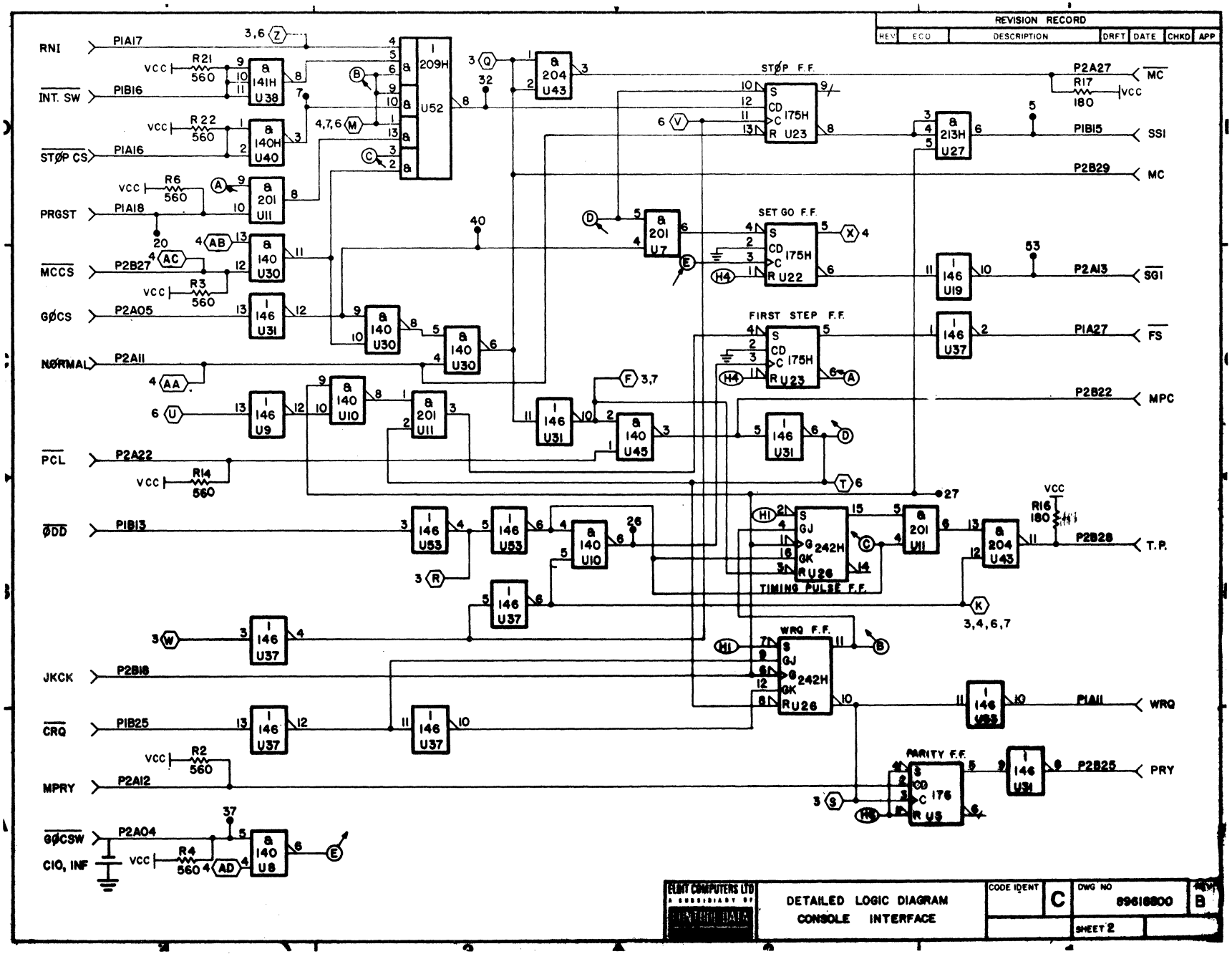
$$MC = \overline{NØRMAL} + (MCCS + MCT)\cdot\overline{GØCS}$$

The Master Clear is active when
- the NØRMAL signal from Memory Control is low
- the computer is not running and the master clear button on the Programmer's Console is pressed
- Master Clear signal is received from the test mode logic
- when the computer is running and the Master Clear button is pressed, the computer is first stopped by the stop flip-flop and then cleared. The signal NØRMAL is active high unless the computer is in power fail mode.

The signal WRQ (U26/11) shows an EVEN cycle occurring after an ØDD cycle in which a request to memory was made. Its data input is CRQ which is produced on the Timing assembly. It is clocked by JKCK and is cleared by MPC.

The WRQ2 flip-flop (U26/15) is active during the odd cycle that follows the

The parity flip-flop, PRY (U5/5) is clocked by $\overline{WRQ}$. It stores the parity of each 16 bit word written into the memory by any store-type instruction being executed in the CPU. PRY (Parity) is high when the number of 1 bits in the 16 bit word is even. The output of the flip-flop, PRY is transmitted to the Decoder assembly and used in the execution of the SPA instruction. The parity of the word written into memory is generated in the Memory Address assembly.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
RNI
PIAI7
INT. SW
PIBI6
STØP CS
PIAI6
PRGST
PIAI8
MCCS
P2B27
GØCS
P2A05
NØRMAL
P2AII
PCL
P2A22
ØDD
PIBI3
JKCK
P2BI8
CRQ
PIB25
MPRY
P2AI2
GØCSW
P2A04
CIO, INF
VCC
R21 560
R22 560
R6 560
R3 560
R14 560
R2 560
R4 560
R16 180
R17 180
U38
U40
U52
U43
U11
U30
U31
U9
U10
U45
U53
U37
U8
U23
U22
U7
U27
U19
U26
U34
U35
STØP F.F.
SET GO F.F.
FIRST STEP F.F.
TIMING PULSE F.F.
WRQ F.F.
PARITY F.F.
P2A27 MC
P2B29 MC
PIBI5 SSI
P2AI3 SGI
PIA27 FS
P2B22 MPC
P2B28 T.P.
PIAII WRQ
P2B25 PRY
ELBIT COMPUTERS LTD
DETAILED LOGIC DIAGRAM
CONSOLE INTERFACE
CODE IDENT C
DWG NO 89618800
REV B
SHEET 2

CONSOLE INTERFACE (drawing number 89618800, sheet 3)

PROGRAM PROTECT LOGIC

Function

This circuit includes most of the logic used by the program protect system of the computer. It detects two of the four types of program protect violations:

a. An attempt to execute a protected instruction after a non-protected one.
b. An attempt to execute an unprotected instruction which can affect the protect system.

The other two types of violation are detected in the Memory Control. They are transmitted to the Console Interface by means of a single signal (CV101).

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
PRTSW	H	P2A14	Protect switch	3	D4
MX17	H	P2A19			C4
IRCK	H	P1A20			C4
$\overline{\text{FE0}}$	L	P2A10			C4
$\overline{\text{ØDD2}}$	L	P2B11			B4
INR	H	P2A29			B4
IO	H	P2B23			B4
IF	H	P2B19			B4
R3	H	P2B06			B4
R4	H	P1A30		3	B4

CONSOLE INTERFACE (Drawing number 89618800, sheet 3, cont'd.)

Inputs (cont'd.)

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
RGPWR	H	P1B22		3	B4
$\overline{\text{SWEEP}}$	L	P1B17			A4
$\overline{\text{ENTER}}$	L	P1B18			A4
$\overline{\text{PEL}}$	L	P1B06			C3
$\overline{\text{CVIOI}}$	L	P2B04			B3
PH3	H	P2B05	Clock phases		A3
PH1	H	P1A14		3	A3

Outputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
PRT BIT	H	P1A25	Parity Bit	3	D1
$\overline{\text{PRTAQ}}$	L	P2A28			D1
$\overline{\text{PRTM}}$	L	P2B24			C1
$\overline{\text{INTOO}}$	L	P2B07			C1
$\overline{\text{PEF}}$	L	P2A09			C1
$\overline{\text{VIØ}}$	L	P2B15			B1
PFIND	H	P2B13	Protect Fault Indicator (PRFA)		B1
CLREQ	H	P2B12	Clear RQ flip-flop		A1
CLRXM	H	P2A29		3	D1

CONSOLE INTERFACE (Drawing number 89618800, sheet 3, cont'd.)

Description

An illegal instruction sequence is detected by the flip-flops MX17 (U48/5,8). The MX17A flip-flop (U48/5) is clocked by IRCK. Its data input is MX17. The first half of the flip-flop (MX17A) stores the protect status of the current instruction. Its output clocks MX17B (U48/9). When a protected instruction follows a non-protected one, the output of MX17A goes high causing the $\overline{Q}$ output of MX17B to go high.

The MX17A flip-flop is set by the signal $\overline{MCI}$ +ENI + $\overline{PRTSW}$. Thus the first instruction after a master clear or after an enter-interrupt sequence may be protected without causing a protect violation. When the protect switch is NOT set, every instruction is considered protected. The MX17A flip-flop is cleared by $\overline{ENTER}$ + $\overline{SWEEP}$ + $\overline{PRFB}$. PRFB is active when a protect violation caused by an illegal instruction is sensed. Such an instruction is executed as a non-protected selective stop. The enter and sweep modes are also non-protected. The output of MX17A is also used on the Memory Control assembly and by the A/Q and DSA busses.

The flip-flop MX17B is preset by:

$$\overline{MCI} + ENI + \overline{PRTSW} + ENTER + SWEEP + \overline{PRFB}$$

This blocks a protect violation when the protect switch is not set and allows a protect violation to be cleared by the master clear signal or by the enter interrupt sequence. It also causes the flip-flop to be preset after a protect fault is detected. The MX17B is cleared by $\overline{PRFB}$ to ensure correct timing.

The protect bit flip-flop (U24/6) stores the protect bit of every word read from the memory. The data input is MX17 and it is clocked by $\overline{WRQ}$ (see sheet 2). The output, PROTECT-BIT is displayed on the Programmer's Console.

CONSOLE INTERFACE (Drawing number 89618800, sheet 3, cont'd.)

The flip-flops PRFA (U35/15) and PRFB (U35/11), are set when a protect fault is detected on the console interface card. The clock is PH3 and data input to both flip-flops is the following function:

$$VI\emptyset = PRTSW \cdot \overline{MX17B} + PRTSW \cdot \overline{MX17A} \cdot RNI \cdot \emptyset DD \cdot (F=0) \cdot (INR \cdot IO + IE + R3 \cdot \overline{R4})$$

This signal is active when the protect switch is set and an illegal sequence is detected; or when the switch is set, the current instruction is not protected, and one of the following instructions has been read: EIN, IIN, SPB, CPB, EXIT, or INR (Inter Register). Here the M register is a destination register. The flip-flop J-input is $\overline{VIO}$. It is also used by the Timing assembly to block the memory request signal CRQ and to avoid the clock JKCK when one of these violations occurs (see Timing, sheet 2).

The PRFA flip-flop may also be set, through its preset input, by the signal $\overline{CVIOI}$ from the Memory Control assembly. This signal becomes active when the memory control detects protect violations during a memory cycle, caused by the CPU.

$\overline{CVIOI}$ also sets a latch made up of two NAND gates (U8/8,11). This latch is reset by the signal:

$$\overline{\emptyset DD} + \emptyset DD2 + PH3 + ENTER + SWEEP + \overline{RNI}$$

The signal $\overline{PEF}$ is active when the latch is set or when the signal $PEL \cdot \overline{MX17A}$ is active. $\overline{PEF}$ is sent to the decoder and is used to avoid changing the A register during the SPA instruction in case the memory write cycle was aborted due to protect fault or parity error.

The PRFA flip-flop is cleared by the signal $MC \cdot \overline{PRTSW}$. It may also be reset by KPF which is produced on the Console Interface (sheet 7). It is active during skip-on-protect-fault or skip-on-no-protect-fault instructions.

CONSOLE INTERFACE (Drawing number 89618800, sheet 3, cont'd.)

The output of the PRFA flip-flop (PFIND) is connected to the PROTECT FAULT indicator on the Programmer's Console.

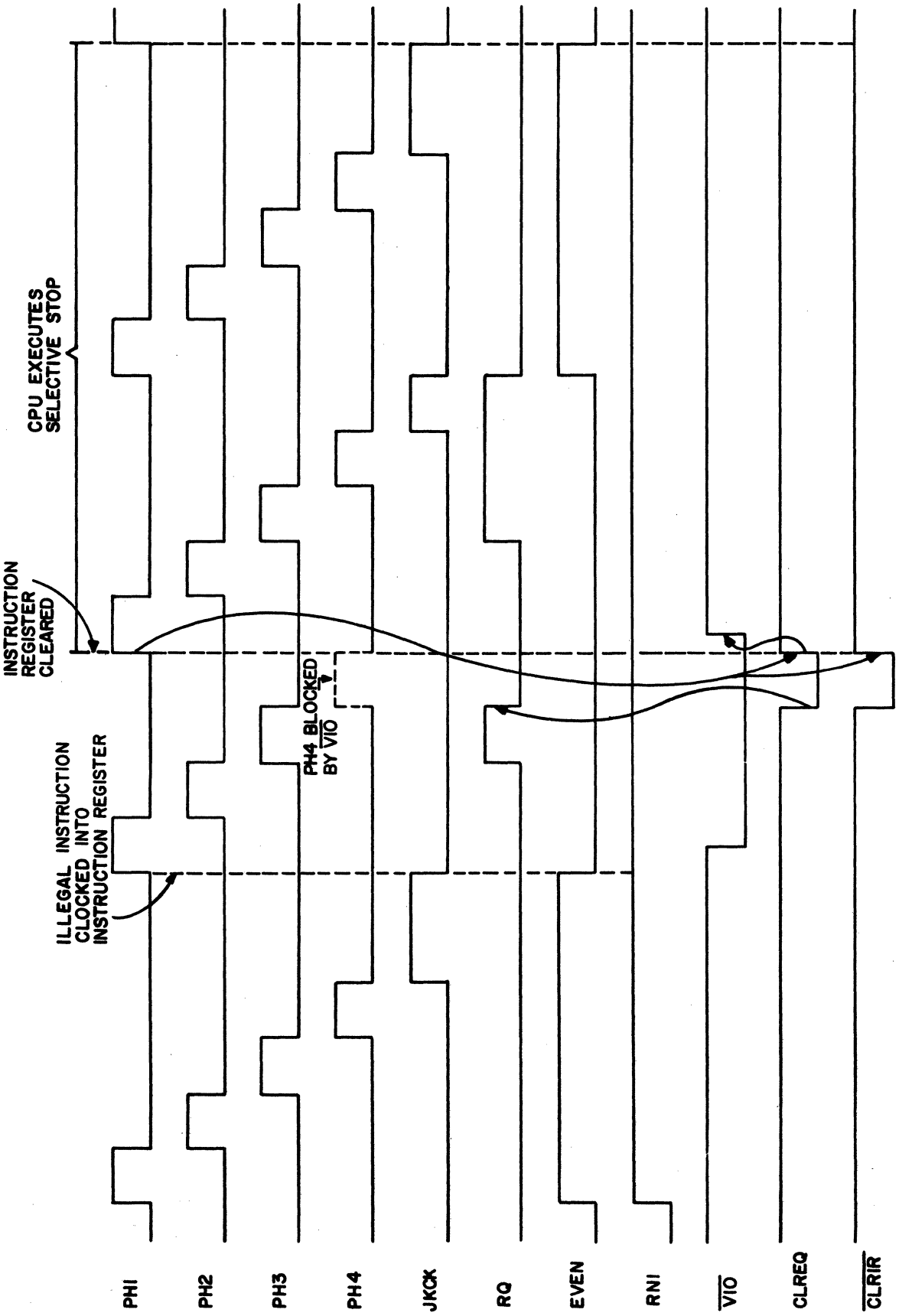
It is also wire-ORed through open collector inverter (U47/8) to be part of the signal $\overline{\text{INT00}}$ which is hard-wired to the zero level interrupt on the ALU least significant board (LSB). The equation of INT00 is:

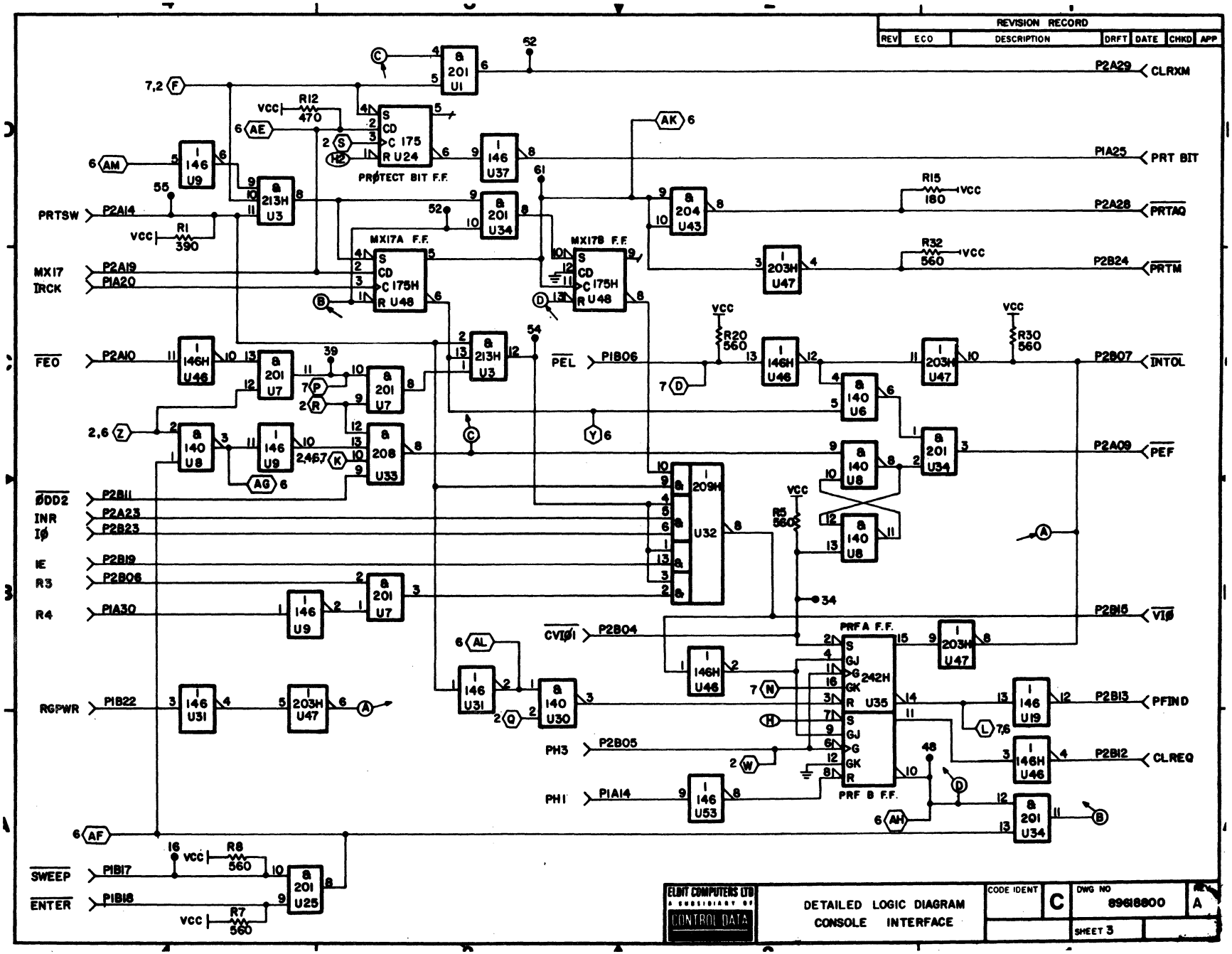
$$\text{INT00} = \overline{\text{PEL}} \cdot \text{RGPWR} \cdot \overline{\text{PFIND}}$$

The PRFB flip-flop is cleared by PH1. It produces the signal CLREQ which is sent to the Timing assembly to clear the RQ flip-flop. This prevents any memory request signal even after the $\overline{\text{VIO}}$ signal has become inactive. The CLREQ signal also clears the instruction register so that the instruction is executed as a non-protected selective stop (see Console Interface, sheet 5).

The timing diagram for the protect fault detect sequence is shown below.

Timing Sequence During Protect Fault Caused By Illegal Instruction




REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
PROTECT BIT F.F.
MX17A F.F.
MX17B F.F.
PRF A F.F.
PRF B F.F.
P2A29 CLRXM
P1A25 PRT BIT
P2A28 PRTAQ
P2B24 PRTM
P2B07 INTOL
P2A09 PEF
P2B15 VIØ
P2B13 PFIND
P2B12 CLREQ
PRTSW P2AI4
MX17 IRCK P2AI9 P1A20
FEO P2AI0
PEL P1B06
ØDD2 P2B11
INR P2A23
IØ P2B23
IE P2B19
R3 P2B06
R4 P1A30
CVIØI P2B04
RGPWR P1B22
PH3 P2B05
PH1 P1AI4
SWEEP P1BI7
ENTER P1BI8
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
CONSOLE INTERFACE
CODE IDENT C
DWG NO 89618800
REV A
SHEET 3

CONSOLE INTERFACE (drawing number 89618800, sheet 4)

TEST MODE AND AUTORESTART

Function

This is the circuit which executes the commands from the TEST MODE and the AUTORESTART positions of toggle switches on the Programmer's Console. Both features cause the computer to start running after a master clear.

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Location Square
OPST	H	P2B09		4	D4
BEA	H	P2B31	Breakpoint signal		D4
$\overline{\text{AUTRSW}}$	L	P2A08	Autorestart switch		B4
$\overline{\text{TMSW}}$	L	P2A24	Test Mode switch		B4
32M	H	P2B26		4	B4
Outputs					
BEAC	H	P2A30	BEA controlled	4	C1

CONSOLE INTERFACE (Drawing number 89618800, sheet 4, cont'd.)

Description

The test mode feature is activated either by the TEST MODE switch or the AUTORESTART switch, both on the Programmer's Console. These switches produce the signals TMSW and AUTRSW respectively, which clock the test mode flip-flop (TM1, TM2: U17) with the signal

$$\overline{32M \cdot (TMSW + AUTRSW \cdot \overline{AUTØRS})}$$

where

- 32M is a clock of about 32 μsec period generated on the memory control board.
- AUTØRS is the output of flip-flop U5/8 (see below).

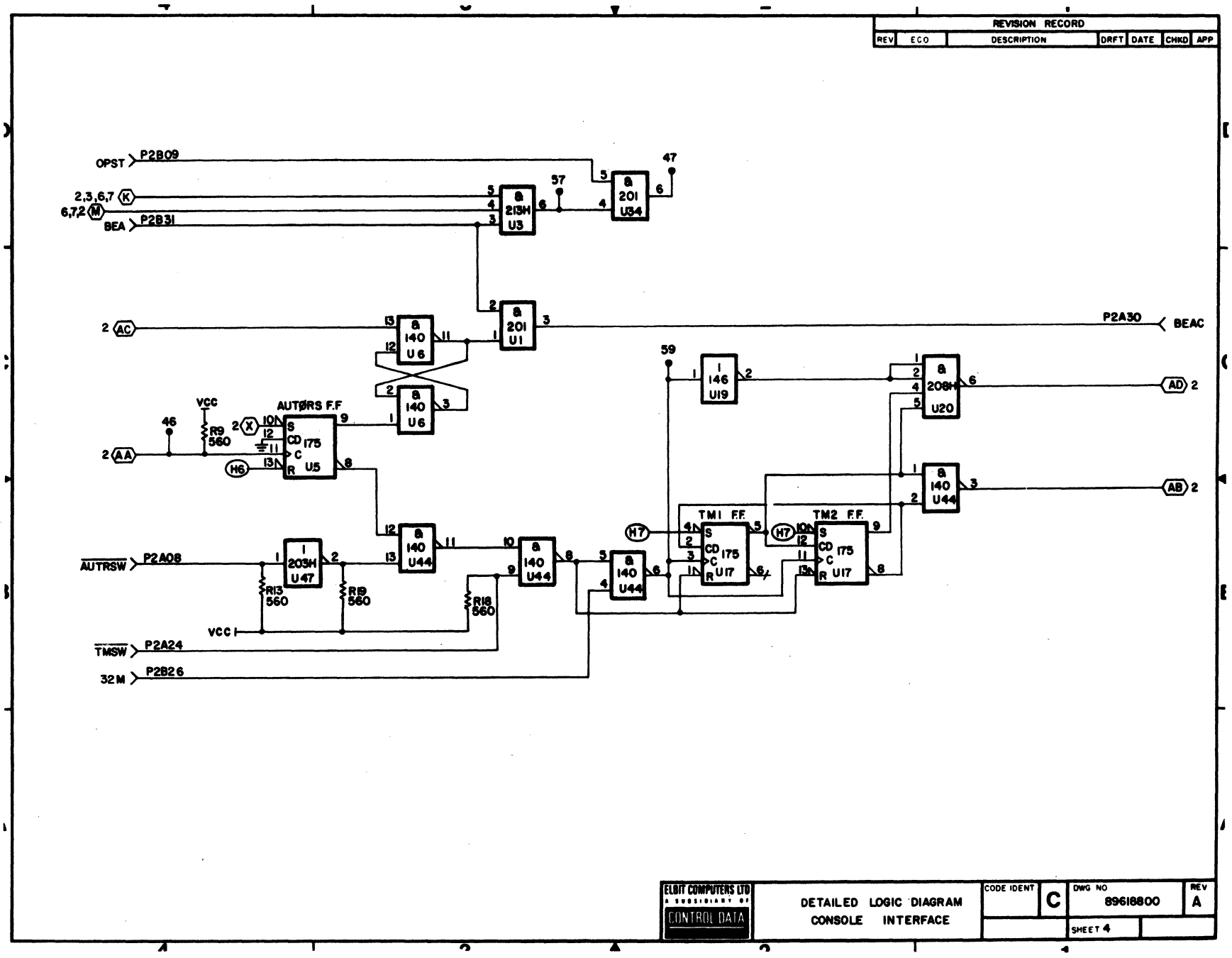
The outputs of two-stage counter formed by TM1 and TM2 are decoded as $\overline{MCT}$ (U44/3) and $\overline{GØT}$ (U20/6). These signals generate a Master Clear ($\overline{MC}$) and then a clock pulse to the GØ flip-flop. The latter starts the computer running (see sheet 2).

With the AUTORESTART switch set the computer is master cleared and starts running on restoration of line power after a power failure.

When a power failure occurs, the signal NØRMAL from the Memory Control assembly goes low. When power is restored, NØRMAL goes high, clocking the AUTØRS flip-flop (U5/8). If the AUTORESTART switch is set, the test mode flip-flops are activated, causing Master Clear (MC), and clocking the GØ flip-flop. The GØ flip-flop produces the signal $\overline{SGT}$ (see console interface sheet 2) which resets AUTØRS thus clearing the test mode flip-flops and allowing the computer to run.

The $\overline{\text{AUTØRS}}$ flip-flop also resets a latch (U6/3, 11) which blocks the breakpoint signal (BEA). This latch is cleared by Master Clear.

The gates U3/6 and U34/6 produce sync pulses when the contents of the breakpoint register and that of the memory address register are equal. These pulses may be used for hardware debugging.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
OPST P2B09
2,3,6,7 K
6,7,2 M
BEA P2B31
8 213H U3
8 201 U34
57
47
8 201 U1
2 AC
8 140 U6
P2A30 BEAC
59
1 146 U19
8 208H U20
AD 2
AB 2
8 140 U44
VCC
R9 560
46
2 AA
AUTØRS F.F
2 X
S CD 175 C R U5
H6
TM1 F.F
TM2 F.F
H7
S CD 175 C R U17
AUTRSW P2A08
1 203H U47
R13 560
R19 560
R18 560
VCC
TMSW P2A24
32M P2B26
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
CONSOLE INTERFACE
CODE IDENT C
DWG NO 89618800
REV A
SHEET 4

CONSOLE INTERFACE (drawing number 89618800, sheet 5)

ALU LOGIC

Function

This circuit performs arithmetic and logic functions in conjunction with the two ALU boards of the CPU.

These functions are:

- carry generation
- calculation of the trap address
- QSX: (contents of Q register) < (contents of X register)
- DBB: that bit of the bit bucket register which is used to generate the sign bit for the result of multiply/divide operations.

NOTE

Two ALU assemblies are used to accommodate the 16 bits of the computer word (without parity or protect bits). One assembly designated LSB, operates on the least significant bits (bits 00 through 07), the other assembly (MSB) operates on the most significant bits (08 through 15). Signals associated with the LSB are labelled L, those associated with the MSB are labelled M, these letters being appended to the signal name.

CONSOLE INTERFACE (Drawing number 89618800, sheet 5, cont'd.)

Inputs

Signal	Active	Connector/Pin	Function	Location sheet	Location square
TA2M	H	P2A21		5	D4
TA2L	H	P2B26	Trap address generators		D4
TA1M	H	P2A17			D4
TA1L	H	P2B17			D4
TA0M	H	P2B16			D4
TA0L	H	P2A15			D4
GMM	H	P2B03	ALU Carry generate (bits 12 ÷ 15)		C4
PMM	H	P2A02	ALU Carry propagate (bits 12 ÷ 15)		C4
GLM	H	P1B20	ALU Carry generate (bits 8 ÷ 11)		C4
PLM	H	P1A21	ALU Carry propagate (bits 8 ÷ 11)		C4
GML	H	P1B31	ALU Carry generate (bits 4 ÷ 7)		C4
PML	H	P2B01	ALU Carry propagate (bits 4 ÷ 7)		C4
GLL	H	P2B02	ALU Carry generate (bits 0 ÷ 3)		C4
PLL	H	P2A01	ALU Carry propagate (bits 0 ÷ 3)		C4
A7M	H	P1B08			D2
X15	H	P1A08			D2
Q7M	H	P1B09			D2
$\overline{03}$	L	P1B07	$\overline{F = 3}$		C2
XGQL	H	P1A03	{X} > {Q} on LSB		C2
XSQM	H	P1B02	{X} < {Q} on MSB		C2
XGQM	H	P1A02	{X} > {Q} on MSB	5	C2

CONSOLE INTERFACE (Drawing number 89618800, sheet 5, cont'd.)

Outputs

Signal	Active	Connector/Pin	Function	Location sheet	Location square
$\overline{\text{ITA4L}}$	L	P2A26	Trap Address	5	D3
$\overline{\text{ITA3L}}$	L	P2A18			D3
$\overline{\text{ITA2L}}$	L	P2A16			D3
MCNM	H	P1B30	Carry output to MSB		C3
LCNM	H	P1B29	- " -		C3
MCNL	H	P1A31	Carry output to LSB		C3
LCNL	H	P1A23	- " -		B3
DBB	H	P1A06	Bit bucket sign bit		C1
QSX	H	P1B03	{Q} < {X}, over 16 bits	5	C1

CONSOLE INTERFACE (Drawing number 89618800, sheet 5, cont'd.)

Description

NOTE

The two ALU boards will be refered to as follows:
MSB: Board dealing with eight most significant bits;
LSB: Board dealing with eight least significant bits.

The carry generator of the ALU is the look-ahead microcircuit, U49. It accepts the carry propagate (P) and carry generate (G) outputs of the ALU microcircuits (74181) from the ALU circuit (sheets 2,3), and returns four carry inputs. Each group of four bits of the ALU produces a G and a P signal, the suffixes specify the group of bits. The following table is a key to these suffixes.

Board	Group of bits	Bit Nos.	Suffix
LSB	lower	0 ÷ 3	LL
LSB	higher	4 ÷ 7	ML
MSB	lower	8 ÷ 11	LM
MSB	higher	11 ÷ 15	MM

CONSOLE INTERFACE (Drawing number 89618800, sheet 5, cont'd.)

The logic equations for the output signals are:

$$\overline{LCNL} = GMM \cdot GML \cdot GLM \cdot (GLL \cdot PLL + PML) + GMM \cdot (PLM \cdot GLM + PMM)$$
$$\overline{MCNL} = LCNL \cdot GLL + GLL \cdot PLL$$
$$\overline{LCNM} = LCNL \cdot GML \cdot GLL + GML \cdot GLL \cdot PLL + GML \cdot PML$$
$$\overline{MCNM} = LCNL \cdot GML \cdot GML \cdot GLL + GLM \cdot GML \cdot GLL \cdot PLL + GLM \cdot GML \cdot PML + GLM \cdot PLM$$

The signal LCNL is generated in the super-high speed AND-OR-INVERT gates U50, U36/6. The output signals are returned to the ALU board designated in the last letter of the signal name: LNCL and MCNL to the LSB, LCNM and MCNM to the MSB.

The trap address is calculated from the TA0, TA1, TA2 signals of the two ALU boards, the corresponding signals from the two boards being ANDed together to form the trap address signals ($\overline{ITA2L}$, $\overline{ITA3L}$, $\overline{ITA4L}$) which are returned to the LSB.

Comparison of the contents of the X and Q registers is performed on each ALU board for the bits on that board. The following signals are generated and sent to this circuit as inputs:

Signal	Origin	Significance
XGQL	LSB	{X} > {Q}
XGQM	MSB	{X} > {Q}
XSQM	MSB	{X} < {Q}

Note: {X} signifies "content of register X over the eight bits of the board".

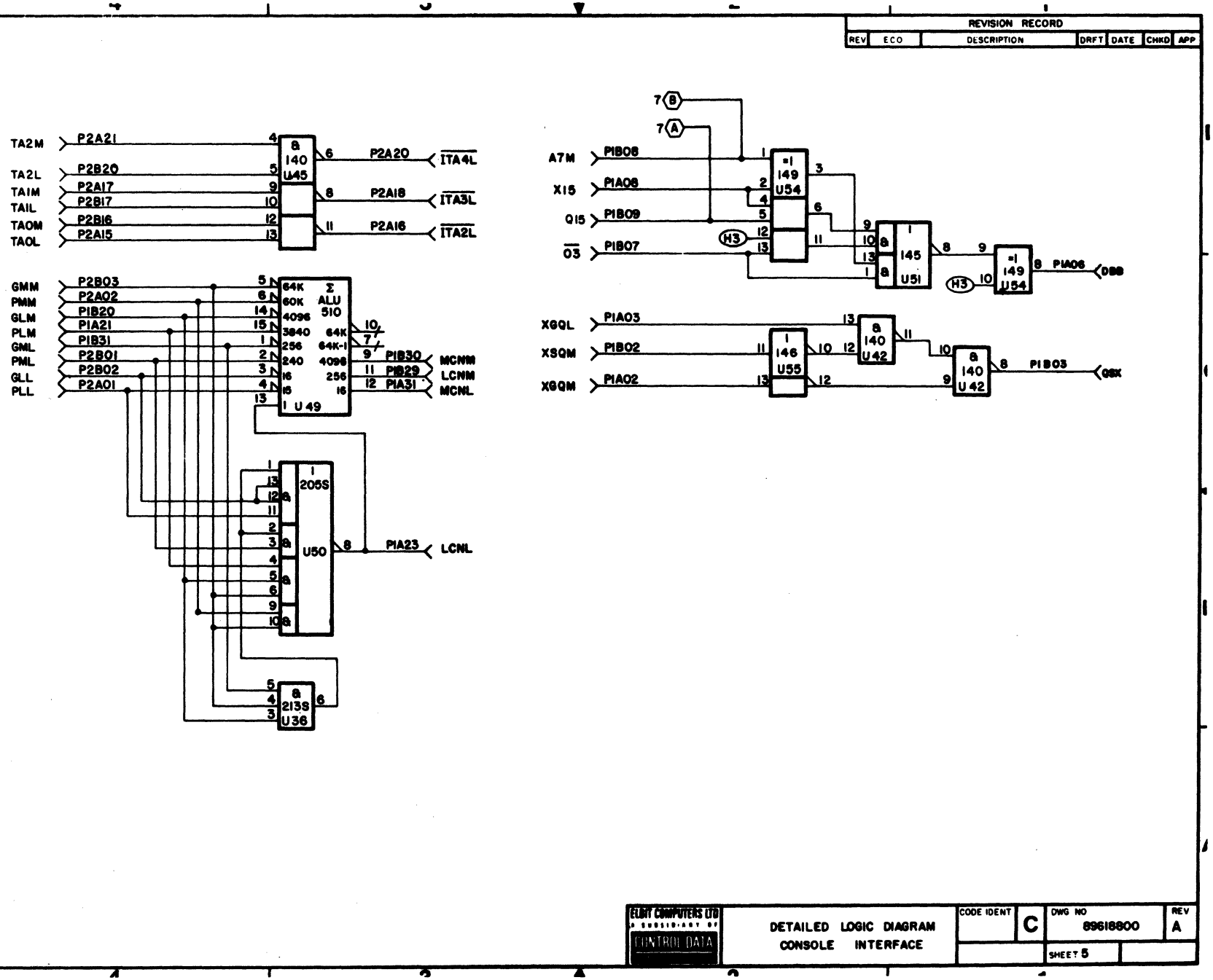
The output of this circuit is QSX which is active when the content of register Q is smaller than the content of register X, over all 16 bits. Its equation is:

$$QSX = XGQM + XGQL \cdot \overline{XSQM}$$

The bit bucket, located on the decoder card, is used to store a bit at the beginning of multiply and divide instructions. In multiply instructions the bit stored is A7M $\oplus$ X15 where A7M is the sign bit of the A register and X15 is the sign bit of the X register.

In division the bit stored is Q7M $\oplus$ X15 where Q7M is the sign bit of the Q register. Thus the bit will be set if numbers of different signs are multiplied or divided. The bit bucket is set by the signal DBB generated at U54/8, from signals of the A, Q and X registers on the MSB:

$$DBB = (A15 \oplus X15) \cdot \overline{03} + (Q15 \oplus X15) \cdot 03$$


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
TA2M P2A21
TA2L P2B20
TAIM P2A17
TAIL P2B17
TAOM P2B16
TAOL P2A15
8 140 U45
P2A20 ITA4L
P2A18 ITA3L
P2A16 ITA2L
GMM P2B03
PMM P2A02
GLM P1B20
PLM P1A21
GML P1B31
PML P2B01
GLL P2B02
PLL P2A01
64K 60K 4096 3840 256 240 16 16
Σ ALU 510
64K 64K-1 4096 256 16
P1B30 MCNM
P1B29 LCNM
P1A31 MCNL
1 U 49
1 205S U50
P1A23 LCNL
8 213S U36
A7M P1B08
X15 P1A08
Q15 P1B09
03 P1B07
=1 149 U54
H3
1 145 U51
=1 149 U54
P1A06 DSB
XGQL P1A03
XSQM P1B02
XGQM P1A02
1 146 U55
8 140 U42
8 140 U42
P1B03 QSX
7 B
7 A
CDC CONTROL DATA
DETAILED LOGIC DIAGRAM
CONSOLE INTERFACE
CODE IDENT C
DWG NO 89618800
REV A
SHEET 5

CONSOLE INTERFACE (drawing number 89618800, sheet 6)

ENTER INTERRUPT LOGIC

Function

This logic circuit controls the initiation of the enter interrupt sequence. (see Timing, sheet 4).

Inputs

Signal	Active	Connector/ Pin	Function	Location Sheet	Square
ENI	H	P1A15		6	D3
$\overline{\text{ENI20}}$	L	P1B24			C3
KRNII	H	P1B28			C3
$\overline{\text{GSL}}$	L	P1A22	Masked Interrupt detected		B3
$\overline{\text{GSM}}$	L	P1A24			B3
$\overline{\text{INDIND}}$		P1B23	Indirect Address indicator		B3
EINT	H	P1A19	Interrupt System Enabled		B3
DEL2	H	P2A20			B3
DFE0	H	P2B08		6	A3

Outputs

$\overline{\text{ØVFW}}$	L	P1B12	ENI·ØVFL	6	D1
$\overline{\text{ENI4}}$	L	P2B14			C1
CLRIR	H	P2B10	Clear Instruction Register		C1
KRNI	H	P2A06			B1
$\overline{\text{KENII}}$	H	P1A28			B1
JENI	H	P2A25		6	A1

CONSOLE INTERFACE (Drawing number 89618800, sheet 6, cont'd.)

Description

The ENI flip-flop on the timing card is set by the signal JENI. This signal is:

$$JENI = [(RNI \cdot \overline{EPS} + INDIND) \cdot (GSM + GSL) \cdot WRQ \cdot EINT] \cdot \overline{[RNI \cdot \overline{MX17A} \cdot MX17 \cdot \overline{PRFA}]} \cdot \overline{[RNI \cdot MX17A \cdot MX17 \cdot DFE0 \cdot DEL2]} \cdot \overline{[RNI \cdot \overline{PRTSW} \cdot DFE0 \cdot DEL2]}$$

where

- EPS is active during enter of sweep mode EPS = ENTER + SWEEP
- GSM and GSL are generated by the ALU boards and are active when any interrupt line is active and its corresponding bit in the M register is set
- INDIND is generated by the I/O interface and is active when the computer is doing indirect addressing
- EINT is produced by the I/O interface and is active when the interrupt system is enabled.

The JENI signal becomes active during RNI or in indirect addressing in the CPU cycle following a memory request if the interrupts are enabled and a masked interrupt is detected. However the JENI signal will be blocked if one of the following conditions exists:

a. The next instruction is IIN and the protect switch is OFF.
b. The next instruction is a protected IIN and the present instruction is protected.
c. The next instruction will cause an illegal instruction sequence (because of a protected instruction following a non-protected one) and a protect fault does not already exist.

CONSOLE INTERFACE (Drawing number 89618800, sheet 6, cont'd.)

The signal KENI1 is used to abort the enter interrupt sequence when the M register is changed just before the sequence has begun and the interrupt is therefore no longer masked. The equation of KENI1 is:

$$\overline{KENI1} = \overline{GSM} \cdot \overline{GSL} \cdot RNI \cdot ENI$$

$\overline{KENI1}$ is used to block the KRNI signal which allows the RNI state to remain active. It is also used to preset the FS flip-flop (see Console Interface sheet 2).

The signal CLRIR is used to clear the instruction register. It is active during:

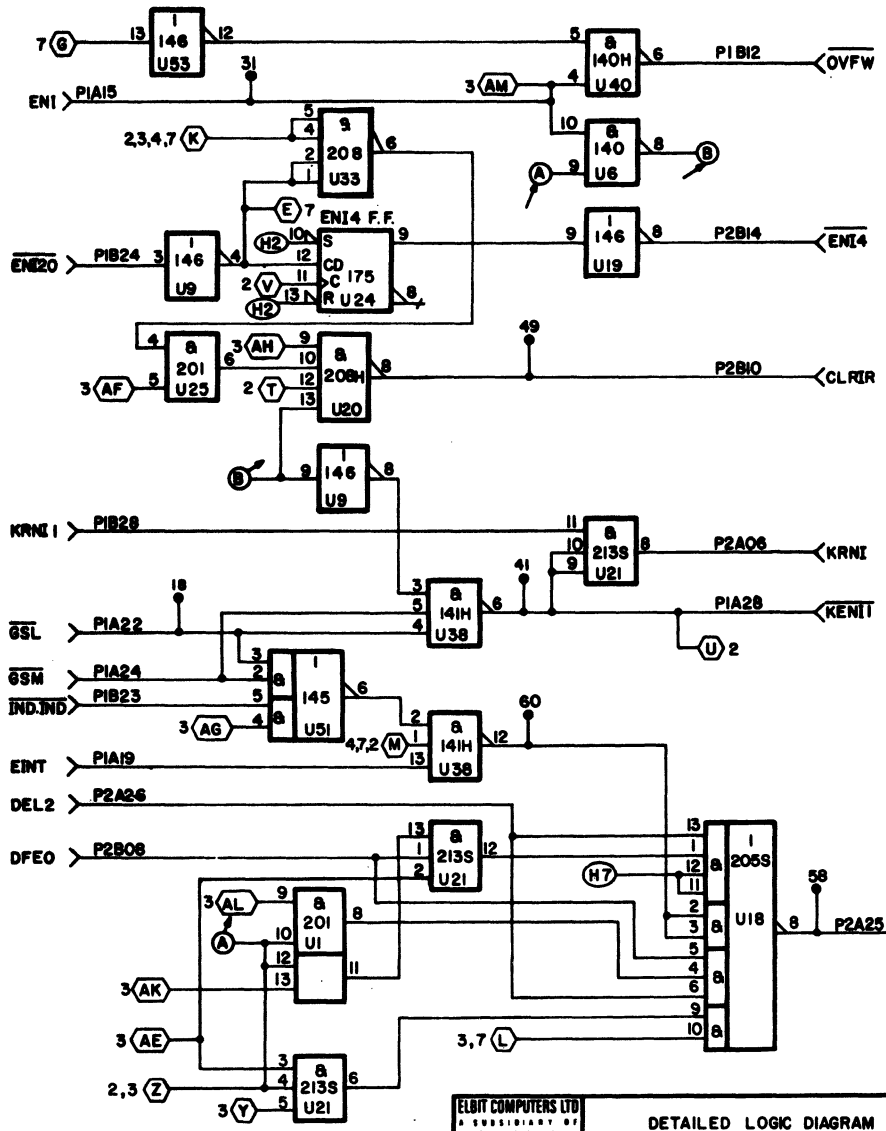
- RNI•ENI which is the first CPU cycle of the enter interrupt sequence (at U20/13);
- ENI2•ØDD (timed by PH3 during sweep or enter) at the end of the sequence;
- CLREQ (see Console Interface sheet 3) at U20/9 and Master Clear at U20/12.

The signal ENI2•ØDD sets the ENI4 flip-flop (U24/9). The output of this flip-flop prevents the first RNI cycle after the enter interrupt sequence from being interpreted as a selective stop. This is necessary as the instruction register is cleared at the time of that sequence.

The signal ØVFW = ENI•ØVFL is used to set bit 15 of the P register with the status of the everflow bit during enter-interrupt when the computer is in 32K mode (32K/65K mode switch on Programmer's Console).

89633300 A

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM CONSOLE INTERFACE	CODE IDENT C	DWG NO 89618800	REV A
			SHEET 6	

5-367/5-368

CONSOLE INTERFACE (drawing number 89618800, sheet 7)

SKIP LOGIC

Function

This circuit carries the logic used in executing the skip instruction.

Inputs

Signal	Active	Computer/ Pin	Function	Location Sheet	Square
32KW	H	P1A12		7	D4
15	H	P1A01	Bit 5 of Instruction Register		D4
FIEI	H	P1A09			D4
$\overline{\text{ØVFL}}$	L	P1B10			C4
14	H	P1B01	Bit 4 of Instruction Register		C4
$\overline{\text{SLK}}$	L	P1A07			C4
AM	H	P1A26	Contents of A register 200		C4
AL	H	P1B26			C4
$\overline{\text{WEZM}}$	L	P1A13	W field of Q-register equals zero		B4
QEZI	H	P1B27			B4
$\overline{\text{WEZL}}$	L	P2A07			B4
16	H	P1B05	Bit 6 of Instruction Register		B4
$\overline{17}$	L	P1A05	Bit 7 of Instruction Register	7	B4

Outputs

KØVF	H	P1A10		7	D1
$\overline{\text{CGPE}}$	L	P1B21			C1
SKT	H	P1B04	Skip Condition		C1
$\overline{\text{WEZ}}$	L	P2B30	WEZ = WEZM (logically)	7	A1

CONSOLE INTERFACE (Drawing number 89618800, sheet 7, cont'd.)
Description

The signal SKT is active when the conditions for a skip exist. Its equation is:

$$SKT = \overline{15}\cdot\overline{16}\cdot\overline{17}\cdot(\overline{14} \oplus \overline{AL\ AM}) + \overline{17}\cdot\overline{16}\cdot 15\cdot(\overline{14} \oplus A7M)$$
$$+\overline{17}\cdot 16\cdot\overline{15}\cdot(\overline{14} \oplus \overline{WEZM\cdot WEZL\cdot QEZ}) + \overline{17}\cdot 16\cdot 15\cdot(\overline{14} \oplus Q7M)$$
$$+17\cdot\overline{16}\cdot\overline{15}\cdot(\overline{14} \oplus \overline{SLK}) + 17\cdot\overline{16}\cdot 15\cdot(\overline{14} \oplus \overline{\emptyset VFL})$$
$$+17\cdot 16\cdot\overline{15}\cdot(\overline{14} \oplus \overline{PEL}) + 17\cdot 16\cdot 15\cdot(\overline{14} \oplus \overline{PFIND})$$

where

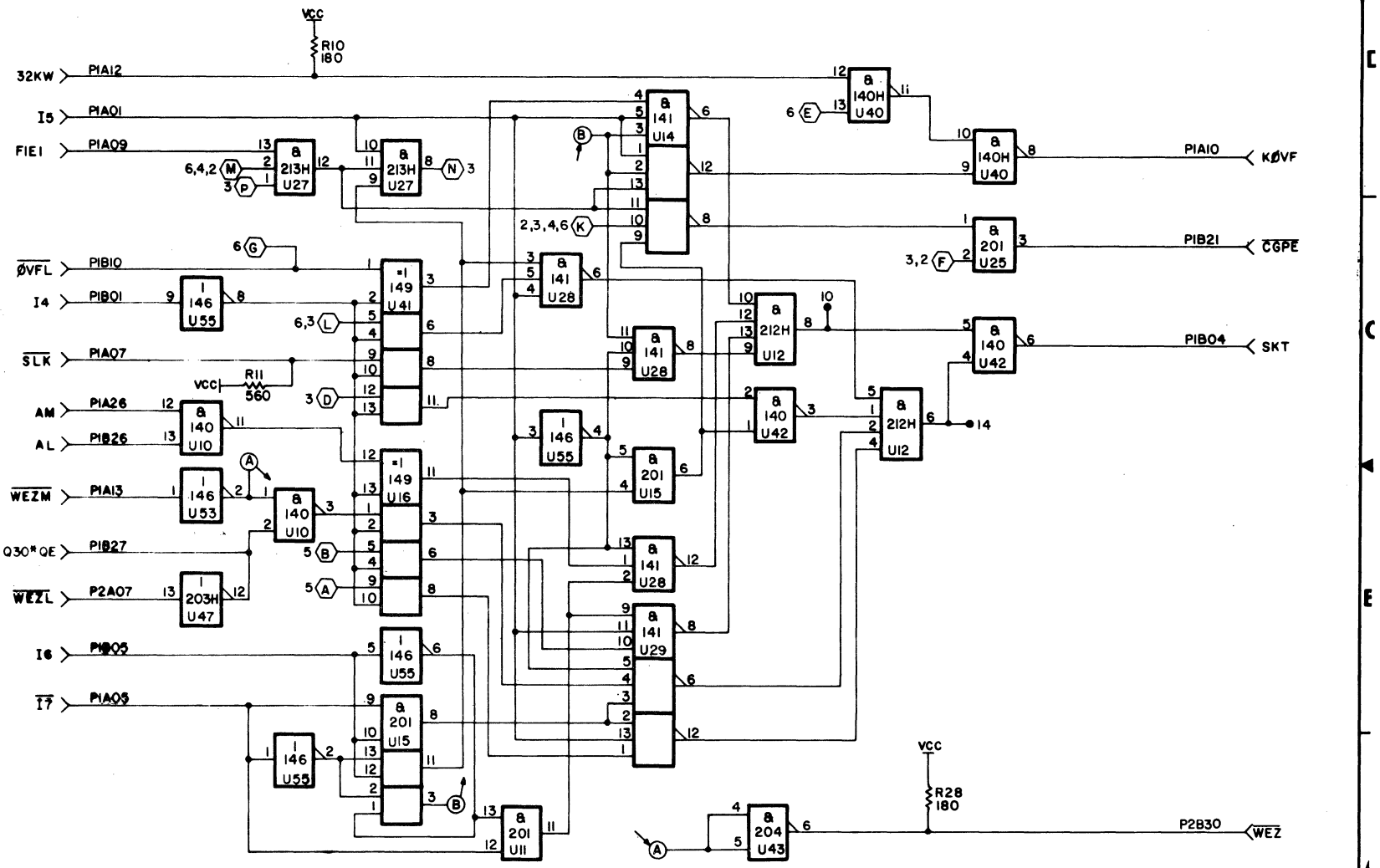
- 14, 15, 16, 17 are bits 4 ÷ 7 of the instruction register,
- AL and AM are produced by the ALU boards and are active when the contents of the A register is zero
- A7M and Q7M are the sign bits of the A and Q registers
- the signal WEZM•WEZL•QEZl is high when the Q register is zero
- SLK is low when the selective skip switch is set
- the signals ØVFL, PEL and PFIND are active during overflow, parity error, and protect fault, respectively.

The signal CGPE is used by the Memory Control assembly to clear the general parity error flip-flop. It is active during skip-on-parity-error and skip-on-no-parity error instructions and also during master clear.

The signal KØVF is used by the I/O Interface assembly to clear the overflow. flip-flop. It is active during skip-on-overflow and skip-on-no-overflow instructions and also when the computer enters an interrupt while in 32K mode (programmer's console switch 32K/65K).

The skip logic also produces a signal (U27/8) which clears the protect fault indicator during a skip-on-protect-fault or skip-on-no-protect-fault instruction.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM CONSOLE INTERFACE	CODE IDENT C	DWG NO 89618800	A
			SHEET 7	

TELETYPEWRITER (TTY) CONTROLLER

The Teletypewriter (TTY) Controller circuits are accommodated on a single 50-PAK wiring board. The logic circuit diagrams and descriptions cover four different printed wiring assemblies (PWA) in the field. The relevant pages are indexed in the lower table on this page.

The TTY Controller interfaces the computer CPU with a Teletypewriter Terminal or with a Console Display Terminal (CDT). It provides for communication at 9600, 1200, 300 or 110 bauds. The baud rate is selected by inserting a jumper plug in the appropriate location on the board (see circuit description, sheet 4. This page lists the functional blocks accommodated on this board. The circuits and signals are described in detail on pages facing the corresponding sheets of the circuit diagram.

This board also carries the Breakpoint Logic.

MAIN FUNCTIONAL BLOCKS

Designation	Shown on sheet
A/Q channel data path	2
Controller/Teletype interface	3
Oscillator - Baud rate selector	4
Address decoding - Reply/Reject logic	5
Control and interrupt logic	6
Breakpoint logic	7, 8

PWA PART NO.	PAGE
89967400	5-374
89947600	5-402
89984700	5-410
89976400	5-416

TTY CONTROLLER (PWA 89967400, Logic Diagram 89616400, Rev. J)

A/Q CHANNEL DATA PATH (sheet 2)

Function:

This circuit receives parallel data from the CPU and converts it into serial form for transmission to the teletypewriter. It also receives serial data from the teletypewriter, converts it into parallel form, and transmits it to the CPU.

Inputs

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
$\overline{A08}$	P2B23	A register bus bits	2	D-4
$\overline{A13}$	P2A11	A register bus bits		D-4
$\overline{RDA}$	[U22/18]	Reset Data Available		D-4
SDIN	[U22/20]	Serial Data Input		B-4
CP	[U22/17]	Clock Pulse		C-4
EPS	P2A28	Even Parity Select		D-2
PARITYSEL	P2A22	Parity Select		D-2
-12V	P2A23	Supply voltage	2	B-4

Bi-directional Signals

$\overline{A00}$	P2A20		2	A-1
$\overline{A01}$	P2B20	Busy Status		A-1
$\overline{A02}$	P2B19	Interrupt Status		A-1
$\overline{A03}$	P2A17	Data		B-1
$\overline{A04}$	P2A21	End-of-Operation Status		B-1
$\overline{A05}$	P2B22	Alarm Status		B-1
$\overline{A06}$	P2B18	Lost Data Status		B-1
$\overline{A07}$	P2A19	Parity Error Status		B-1
$\overline{A09}$	P2B24			A-1
A10	P2B26		2	A-1

(or data bits to/from A-register)

Outputs

$\overline{A11}$	P2B28		2	D-4
$\overline{SP\emptyset UT}$	[U22/25]	Serial Data Output		C-1
TBMT	[U22/22]			C-1
EØC	[U22/24]	End-of-Operation Status		C-1
ØR	[U22/15]			A-4
DA	[U22/19]	Data Available		A-4
PE	[U22/13]		2	A-4

TTY CONTROLLER (drawing 89616400, sheet 2, cont'd)

Description

Lines A00 through A07, A09 and A10 communicate with the CPU and serve both as input and output lines. Lines A08 and A13 are served as inputs to the controller. Signal A11 is an output from the controller. The input signals are buffered and converted. They are used as director function bits and are input to the Universal Asynchronous Receiver/Transmitter (UAR/T) U22, and other parts of the controller.

The circuit is built around the Universal Asynchronous Receiver/Transmitter (UAR/T). In its receive portion, this accepts serial data from the teletypewriter (SDIN) and converts it to data on eight parallel lines (terminals 5 through 12) timed by the clock pulses (CP) from the oscillator baud rate selector (sheet 4). In its transmit portion, the UAR/T accepts parallel data on eight lines (terminals 26 through 33) and transmits it to the teletypewriter as SDØUT under the action of the same clock (CP).

The control inputs to the UAR/T are XR, $\overline{DS}$, CP, $\overline{RDA}$, $\overline{PARITYSEL}$, and even parity:

- XR resets the internal registers of the UAR/T
- $\overline{DS}$ is a strobe for parallel input (transmitter)
- CP is the clock input
- $\overline{RDA}$ resets the data available signal DA (receiver)
- $\overline{PARITYSEL}$ is used to select the parity option,
- EPS: selects whether even or odd parity is used.

The following table summarizes the action of the parity selector signals:

SIGNAL	LOGIC LEVEL	FUNCTION
EPS	High	Even parity generated in UAR/T
EPS	Low	Odd parity generated in UAR/T
$\overline{PARITYSEL}$	Low	Enables parity in UAR/T (7 data + parity bit)
$\overline{PARITYSEL}$	High	No parity generation (8 bits from CPU)

TTY CONTROLLER (drawing 89616400, sheet 2, cont'd)

The control outputs are PE, ØR, DA, TBMT and EØC signals.

- PE is active when the parity option is selected and a parity error is detected in the serial data input.
- ØR is active when a new character is received on the SDIN input, and the DA output has not yet been reset.
- DA is active when a character has been received on the SDIN input and is stable on the parallel data outputs.
- TBMT is active when a new character is transmitted in the SDØUT and remains active until the start of transmission of the next character.

The data flow from the CPU to the teletypewriter is thus from the common input/output lines of the controller (A00 through A07, A09, A10) with parallel data, to the single line serial data (SDØUT), according to the baud-rate clock and according to the control signals.

The data flow to the CPU is selected by multiplexers U23, U37. The outputs of these multiplexers are either the eight data bits from U22 or the eight status bits: Busy, Interrupt, Data EOP, Alarm, Lost Data and Parity Error. One status bit is always "1". The data selectors are controlled by signal DSEN which comes from the address decoding and reply/reject logic. Bits $\overline{A00}$ to $\overline{A07}$ are strobed by the signal (DSEN+RDA+READ) which comes from the receiver/transmitter control logic. This signal is active when the controller sends data or status to the CPU. The status bits are strobed by signal DSEN. They are used as follows: $\overline{A09}$: read mode $\overline{A11}$: manual interrupt

NOTE

Sheet 2 on page 5-378 differs from some older revisions in the following areas:

* zone B-4: U22/20 is not connected to U22/21(zone C-1)
* zone C-3: AND-gate type 140 is U7/9,10-8
* zone A-2: AND-gate U68/1,2,13-12 is type 213S

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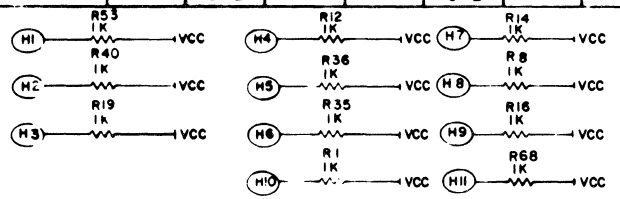
ØFF SHEET REFERENCE

OFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4	5	6	7	8
A	B-4		B-1				
B	B-4				A-3		
D	B-4			B-1			
F	B-4	C-3					
G	A-4				A-4		
J	C-1				B-3		
K	A-4				B-4		
L	C-3			C-1	A-4		
M	C-4			C-3			
N	C-3				C-4		
P	B-3				A-3		
Q	B-3				C-3		
R	B-3			C-2	B-1		
S	B-3				D-1		
T	A-3				D-1		
U	A-3				B-1		
V	C-3			C-3			
W	C-3				C-4		
X	C-3	C-3			B-4		
Y	D-2	B-4		C-2			
Z	C-2	B-4		C-2			
AA	C-2			C-2	D-4		
AB	C-2			C-2	D-3		
AC	C-1			B-2			
AD	C-1			B-2			
AF	B-1			B-2			
AG	B-1	C-2		D-2			
AJ	B-1			C-2			
AK	B-1			C-2	D-4		
AL	C-1				C-1		
AM	C-1	D-3					
AN	C-1				B-2		
AP	A-4				B-4		
AQ		B-4		B-2			
AR		B-3		B-1	A-2		
AS		C-3			A-4		
AT		C-3			C-1		
AU		D-2			C-2		



SHEET REVISION STATUS

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C	B	A	B	B	A	B	A		
D	D	D	B	B	D	B	A		
E	E	D	B	B	E	B	A	E	
F	F	D	F	B	E	F	A	F	
G	F	D	G	B	E	F	A	G	
H	H	D	H	B	E	H	A	H	
J	J	J	J	J	J	H	A	J	

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
J		SEE PAGE 9				

	2	3	4	5	6	7	8
AV			D-1	D-3	C-1		
AX				C-3	B-4		
AY				C-3	C-1		
AZ				B-2	D-4		
BA				D-2	B-2		
BB				C-3	B-2		
BD				C-2	D-3		
BF				C-1	C-1		
BG				B-1	D-3		
BH	A-4				B-3		
BK				B-1	D-4		
BL				B-1	D-3		
BM						C-4	B-3
BN						B-4	B-3
BP						D-3	D-2
BQ						B-2	C-1
BR						A-2	C-1
BS						A-2	C-1
BT						A-4	A-3
BU			A-3	A-2			
BV	A-4			D-3			
BW	A-3				B-3		

NØTE ALL UNMARKED RESISTØRS ARE 025 WATT 5%

AW 89616300
AY 89967400
DETACHED LISTS

DO NOT SCALE DRAWING

MATERIA

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CONTROL DATA
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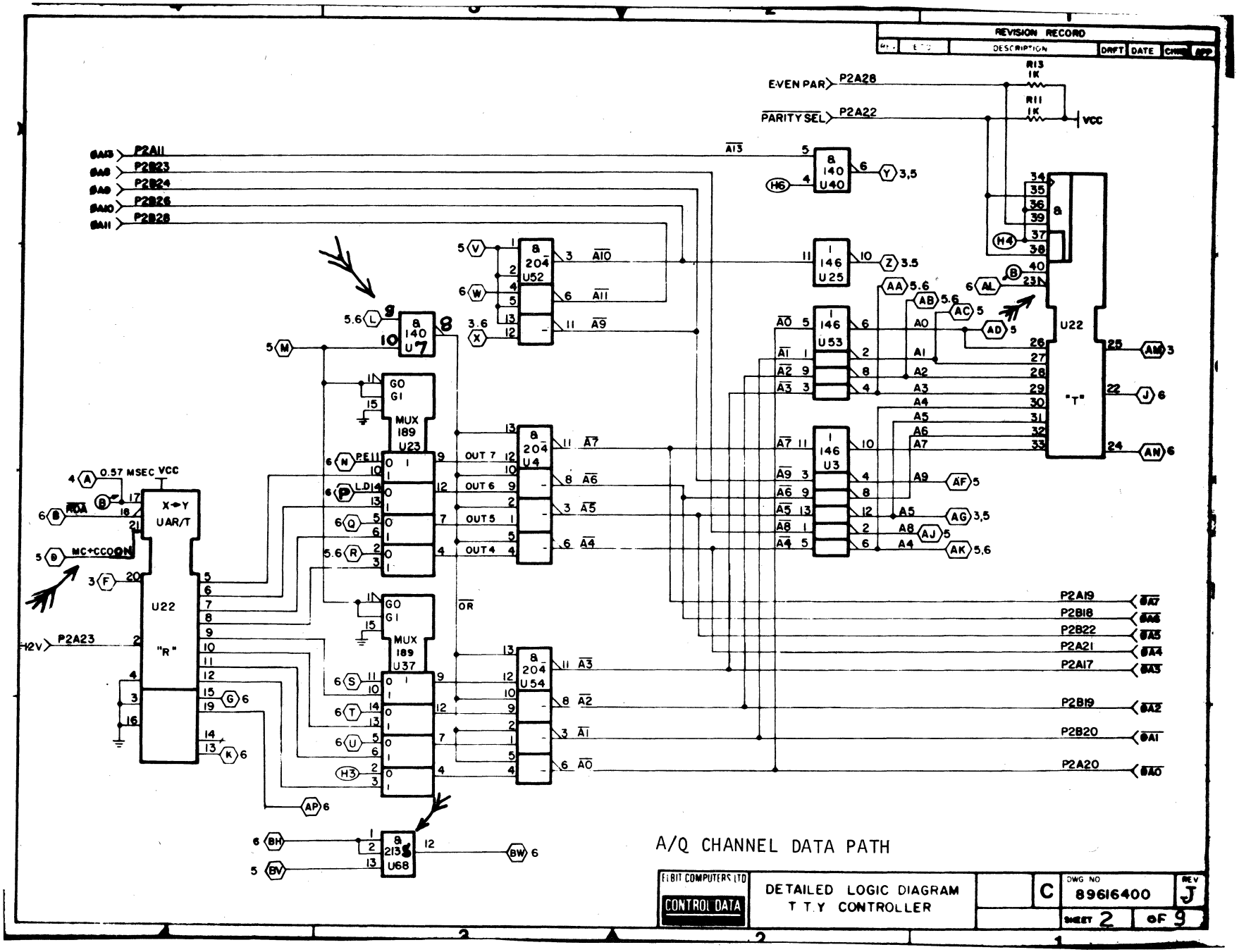
CHKD HAIM J.
APP'D
QA
May 78

TITLE
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
P/N 89967400

DRAWING NO. 89616400
REV C
SHEET 1 OF 9

89633300 E

5-377


REVISION RECORD
DESCRIPTION
DRFT
DATE
CHK
APP
EVEN PAR P2A26
PARITY SEL P2A22
R13 1K
R11 1K
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P2B23
P2B24
P2B26
P2B28
U40
U25
U53
U3
U52
U4
U54
U7
U23
U37
U68
U22 "R"
U22 "T"
X←Y UAR/T
MUX 189
OUT 7
OUT 6
OUT 5
OUT 4
0.57 MSEC
MC+CCOON
P2A23
P2A19
P2B18
P2B22
P2A21
P2A17
P2B19
P2B20
P2A20
A/Q CHANNEL DATA PATH
FEBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
T T Y CONTROLLER
C
DWG NO 89616400
REV J
SHEET 2 OF 9

TTY CONTROLLER (Drawing number 89616400, sheet 3)

CONTROLLER/TELETYPE INTERFACE

Function:

This circuit acts as an interface for serial data input and output (SDIN, SPØUT) between the controller and the teletypewriter or the Console Display Terminal (CDT).

Inputs

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
TTY-KB	P2A25	Signal from Teletypewriter	3	C-4
CDT TRANS	P2A27	Signal from CDT		C-4
V_{CC}	P2A31	Supplies		A-4
+19V	P2B27			B-2
-12V	P2A24		3	A-2

Outputs

TTY PR	P2B30	Teletypewriter signal indicator	3	D-1
	P2A26	Signal to Teletypewriter (driver output)		C-1
MØTØR ØN	P2B29			C-1
$\overline{\text{MØTØR ØN}}$	P2A29			C-1
CDT-REC	P2A30	Signal to CDT	3	C-1

NOTE

Sheet 3 on page 5-381 differs from some older revisions in the following areas:

* zone B-3: the TTS flip-flop is U5-14, type 242H.
* zone C-4: the signal at P2A10 is identified as TEST IN.

TTY CONTROLLER (Drawing number 89616400, sheet 3, cont'd)

Description

The controller input signal from the teletypewriter keyboard (TTYTB) enters the controller through the optical coupler U20 and is passed to the A/Q channel data path circuit (sheet 2) as signal SDIN. Alternatively when the CDT peripheral is connected, its output (CDTTRANS) is taken to the coupler through transistors Q1, Q2. The optical coupler provides isolation between the controller logic circuits and possible high voltages appearing on the peripherals. Resistors R31, R18 in the input circuit provide matching for the CDT signals; R31 and catching diode CR1 also isolate and protect the transistors.

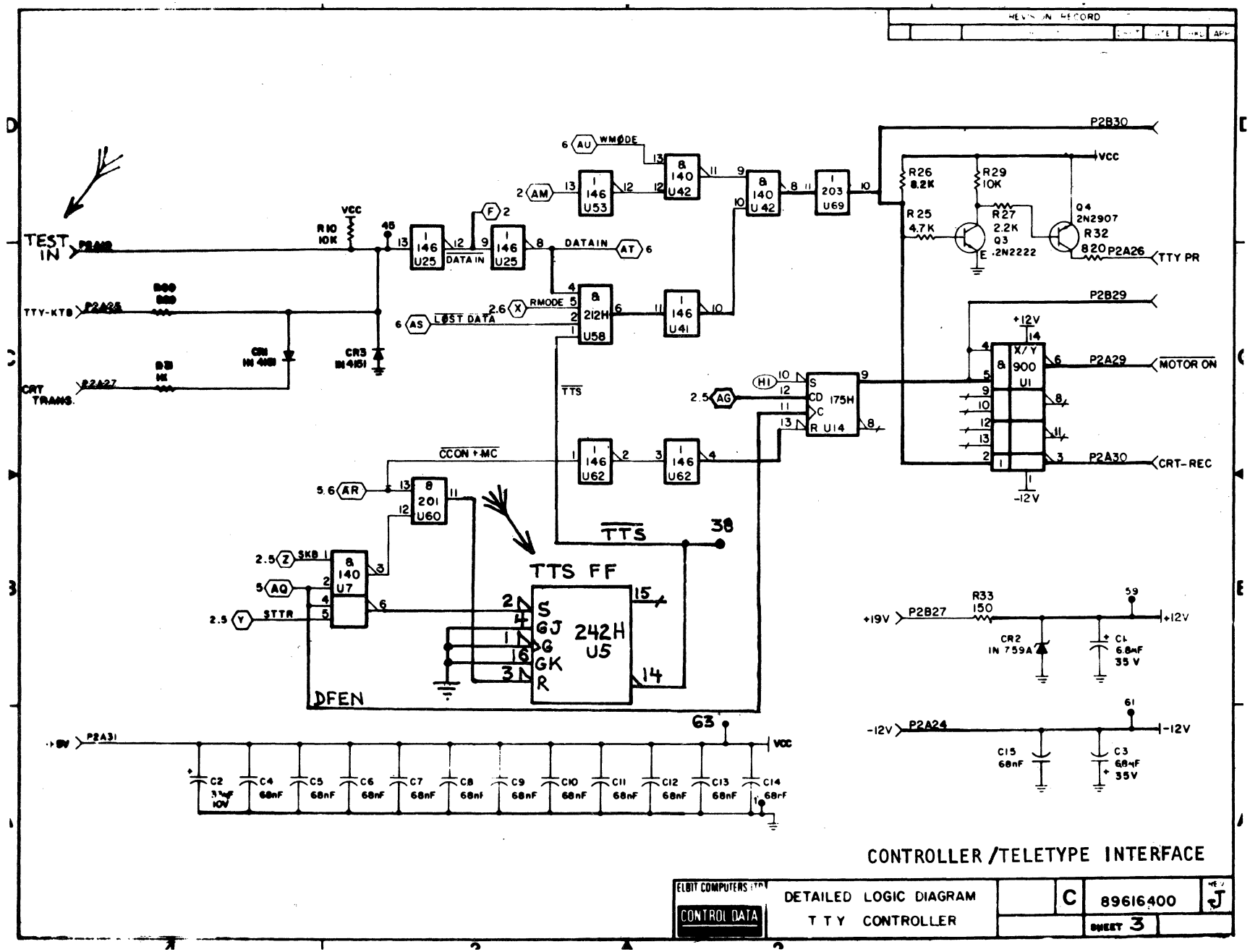
Both the controller output signal (SDØUT from the UAR/T on the A/Q channel data path circuit, sheet 2) and the controller input signal (SDIN) are passed for display (TTYPR, CDTREC) through the data output circuit. The two signals are combined at U42/8 and gated to the output circuit as follows:

Data Signal	Gating Signal	Conditions
SDØUT	WMØDE	Write mode
SDIN	RMØDE·LOST DATA·TTS	Read mode, no lost data, TTS flip-flop set

The TTS flip-flop is selected by the signal DFEN. It is set by A13 ($\overline{A13}$ active low) and cleared by either A10 (active high) or by $\overline{MC \cdot CONT}$ from the address decoding and reply/reject circuit (sheet 5).

The controller data output circuit transmits the serial data (SDIN, SDØUT) to the teletypewriter printer (TTYPR) through transistors Q3 and Q4 and to the CDT peripheral through driver U1/3 (CDTREC).

The MØTOR ØN signal is transmitted through driver output U1/6, it is set by A05 and cleared by $\overline{MC\ CONT}$. When set it is clocked by DFEN in U14. The signal is available as an indicator with opposite polarity.



CONTROLLER /TELETYPE INTERFACE

CONTROL DATA	DETAILED LOGIC DIAGRAM T T Y CONTROLLER	C	89616400 REV J SHEET 3

TTY CONTROLLER (Drawing number 89616400, sheet 4)

OSCILLATOR - BAUD RATE SELECTOR

Function:

The Oscillator-Baud Rate Selector Circuit generates the clock signals required to operate the controller at four different rates: 9600, 1200, 300 and 110 baud. The three higher rates are used only with the CDT.

The circuit consists of a clock section and a group of programmable counters forming the rate selector.

SIGNAL	SIGNAL SOURCE/ CONNECTOR PIN	FUNCTION	LOCATION SHEET	SQUARE
EXTCLK	P2A09	External Clock	4	D-4
STPCLK	P2B09	Clock Stop Enable		D-4
$\overline{\text{BAUD SEL}}$	P2A08	Programmed Selector Enable		B-4
Outputs				
CP	[U7/11]	Clock pulses	4	B-1
1.3µs	[U15/3]	1.3 µsec clock	4	D-1

TTY CONTROLLER (drawing 89616400, sheet 4, cont'd.)

The Clock Section

The main oscillator consists of U45, U68, Q5, Q6 and a 12.2222 MHz crystal. The output of this oscillator is divided by 10 (programmable counter U31 and flip-flop U14). The resulting signal of 1.2222 MHz goes to divide-by-16 counter (U15). One output of U15 (Pin 3), is a clock with a 1.3 microsecond period used in other parts of the control logic. The output at U15 (Pin 6) is a 152.8 kHz clock which goes to the Baud Rate Selection Circuit.

The Rate Selector

Baud rate selection is accomplished by changing the preset inputs to programmable counters U10 and U11. These process the 152.8 kHz clock signal according to the preset input lines coming from multiplexor U12. This chooses between two groups of four signal lines: $\overline{\text{BAUDSEL}}$ active selects four hard-wired logic levels as inputs to the selector, setting the programmable counter to the 1200 baud rate; $\overline{\text{BAUDSEL}}$ inactive selects four programmable lines from location U13 as inputs to the selector. A removable jumper plug at this location selects one of the baud rates as follows:

Baud rate	Jumper plug in position U13 terminals
110	10 - 7
300	11 - 6
1200	12 - 5
9600	13 - 4

TTY CONTROLLER (drawing 89616400, sheet 4, cont'd.)

The action of this circuit is now described.

When the 9600 baud is selected, the jumper plug at U13/10 - 7 forces U12/4 to logic low while the other outputs remain high. This clears flip-flop U9, blocking the output from counter U10, and gates the 152.8 kHz clock through U8/3 and U5/6. The resulting clock pulse (CP) goes to the clock input of U22 in the A/Q channel data path logic.

When 1200 baud is selected, pin U12/12 becomes low while the other outputs are high. This causes the data inputs of programmable counter U11 to be 1011_2 and the data inputs of programmable counter U10 to be 0000_2. The circuit composed of U9, U10 and U11 thus behaves as a divide-by-8 counter and the clock frequency signal (CP) becomes 19.1 kHz.

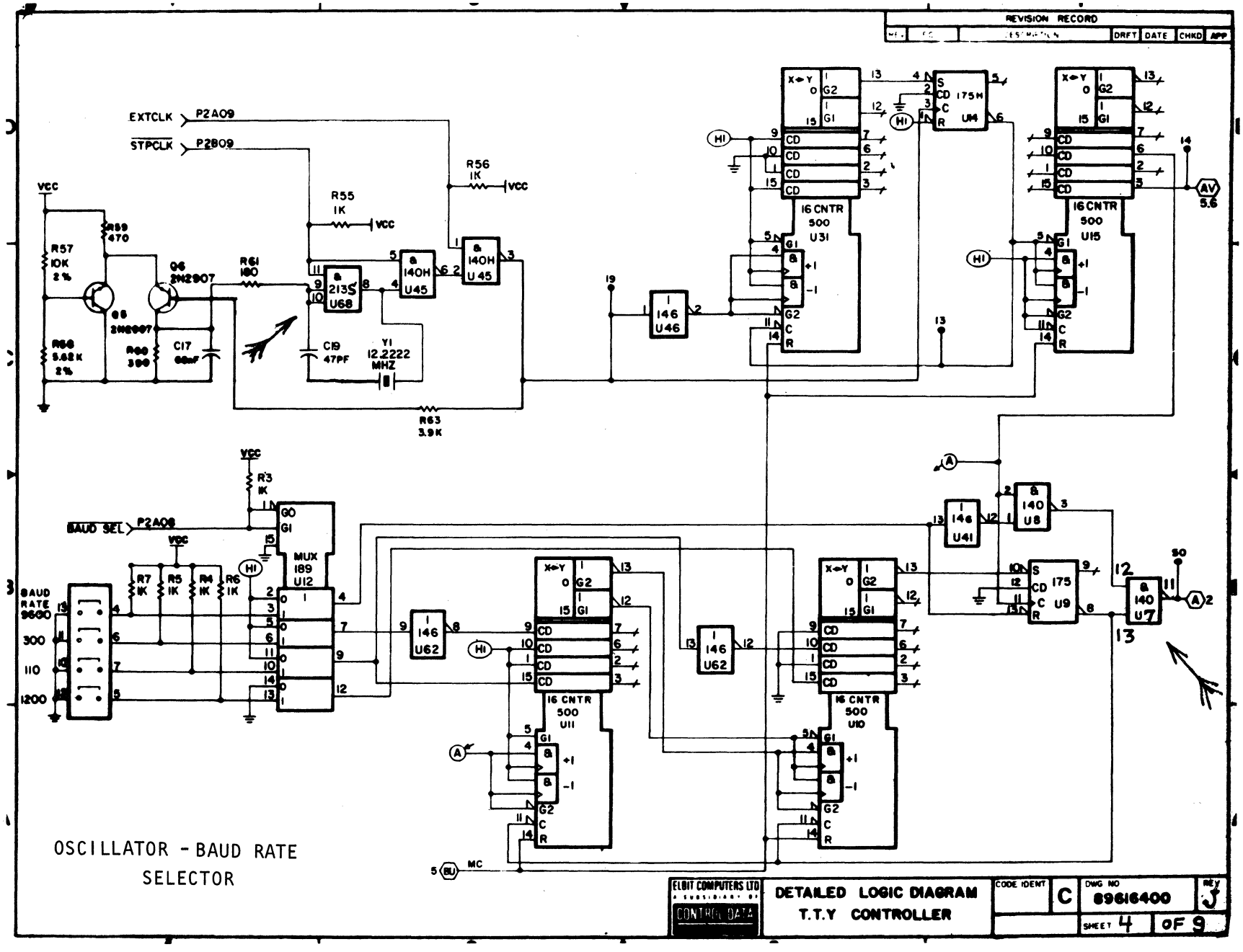
Similarly, when 300 baud is selected, the counter divides by 32 to produce a frequency of 4.77 kHz. When 110 baud is selected the counter divides by 87 to produce a frequency of 1.76 kHz.

Note that the jumper plug for baud rate selection in location U13 has to be inserted at the time of installation.

NOTE

Sheet 4 on page 5-385 differs from some older revisions in the following areas:

* zone C-4: two capacitors (C18, 0.47NF and C20, 47PF) and 180-ohm resistor R62 are not mounted in the oscillator circuit.
* zone C-3: AND-gate U68/11,9,10-8 is type 213S.
* zone B-1: AND-gate type 140 is U7/12,13-11.


REVISION RECORD
EXTCLK P2A09
STPCLK P2B09
VCC
R57 10K 2%
R59 470
R58 5.62K 2%
R60 390
Q5 2N2907
Q6 2N2907
R61 180
C17
R55 1K
R56 1K
R63 3.9K
U68 213S
U45 140H
U45 140H
C19 47PF
Y1 12.2222 MHZ
U46 146
U31 16 CNTR 500
U44 175H
U115 16 CNTR 500
AV 5.6
HI
BAUD SEL P2A08
R3 1K
R7 1K
R5 1K
R4 1K
R6 1K
MUX 189 U12
BAUD RATE 9600
300
110
1200
U62 146
U62 146
U111 16 CNTR 500
U110 16 CNTR 500
U41 146
U8 140
U9 175
U7 140
MC
OSCILLATOR - BAUD RATE SELECTOR
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
CODE IDENT C
DWG NO 89616400
REV J
SHEET 4 OF 9

TTY CONTROLLER (drawing 89616400, sheet 5)

ADDRESS DECODING - REPLY/REJECT LOGIC

Function

This circuit decodes the A/Q channel address bits from the Q register of the CPU as well as the $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ signals. It decides on the response ($\overline{\text{REPLY}}$ or $\overline{\text{REJECT}}$) to the CPU based on these signals and on the status of the controller itself. The circuit also generates control signals used in other parts of the controller.

Inputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{\text{WEZ}}$	L	P2A15		5	C-4
Q00	H	P2A05			B-4
Q04	H	P2B07			C-4
Q05	H	P2B15			C-4
Q06	H	P2A14			C-4
Q07	H	P2A06			C-4
Q08	H	P2B14			C-4
Q09	H	P2A16			C-4
Q10	H	P2B16			C-4
$\overline{\text{READ}}$	L	P2A04			B-4
$\overline{\text{WRITE}}$	L	P2B06			B-4
$\overline{\text{MC}}$	L	P2B08		5	A-4

Outputs

$\overline{\text{REJECT}}$	L	P2B13		5	D-1
$\overline{\text{REPLY}}$	L	P2B12		5	D-1

TTY CONTROLLER (drawing 89616400, sheet 5, cont'd)

Description

The CPU addresses the TTY controller through the signals WEZ, Q04 through Q10. When WEZ, Q10, Q09, Q08, Q06, Q05 are at logic low and Q04, Q07 are at logic high, the TTY controller is selected and the logic high at the output of the address decoder (U44/12: TADR) opens the decoder gates (U30, U44/6). The decoder gates produce four signals, which are active according to the information and data flow (under CPU command):

Note: TADR is active high at U44/12 when the TTY controller is addressed.

Terminal	Signal	Equation	Information/ Data Flow
U30/12	RDEN	TADR.READ.$\overline{Q00}$	Data from TTY to CPU (Read Data Enable)
U30/6	WDEN	TADR.WRITE.$\overline{Q00}$	Data from CPU to TTY (Write Data Enable)
U30/8	DSEN	TADR.READ.$\overline{Q00}$	Status of controller to CPU (Director Status)
U44/6	DFEN	TADR.WRITE.$\overline{Q00}$	Director function from CPU to controller

The strobe flip-flops provide the timing for the controller outputs (REPLY, REJECT). They are clocked by the 1.3 microsecond pulse train from the oscillator/baud selector circuit (sheet 4) and cleared (stopped) unless either the $\overline{READ}$ or $\overline{WRITE}$ command is active.

The controller gives a $\overline{REPLY}$ or $\overline{REJECT}$ output to the CPU during strobe pulses. The $\overline{REPLY}$ signal is active when the output control gate (U39/6) is high. This occurs when any one of its inputs is low. The following table summarizes the input conditions to the output control gate.

TTY CONTROLLER (drawing 89616400, sheet 5, cont'd.)

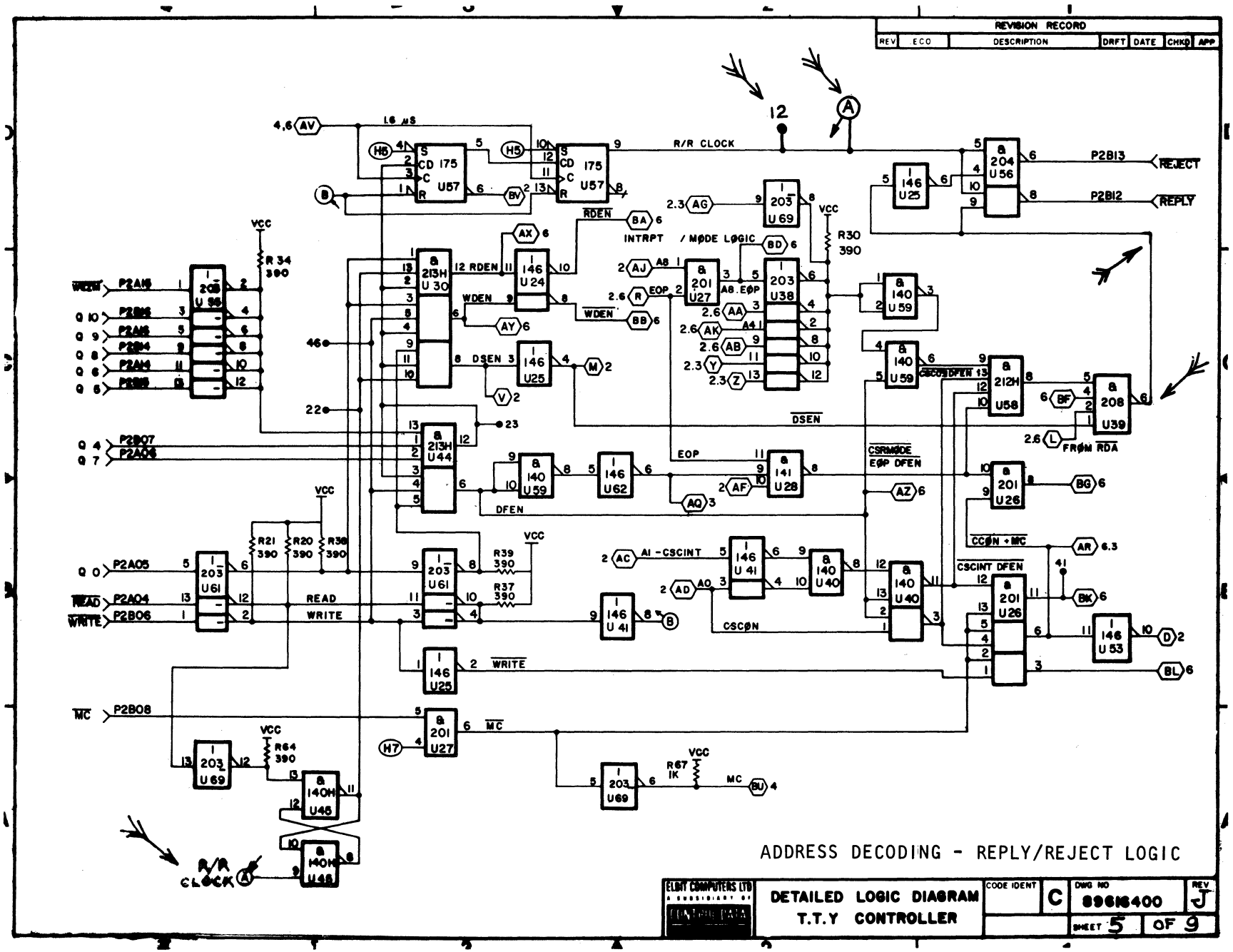
Terminal	Input Signal	$\overline{\text{REPLY}}$ Active
U39/1	$\overline{\text{DSEN}}$	Read Status, Reply always
U39/2	$\overline{\text{DS}}$•WRITE	Transmission of character from controller to TTY complete
U39/4	$\overline{\text{RDA}}$•READ	Character from TTY in controller and ready for transmission to CPU
U39/5	Decoder output (U58/8)	Director function sent from CPU to controller when expression in note is high

NOTE

Sheet 5 on page 5-389 differs from some older revisions in the following areas:

*zone D-2: U57/9, R/R CLOCK, is connected to U5/9 (zone A-4)

*zone D-2: TP12 is connected to U57/9.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
ADDRESS DECODING - REPLY/REJECT LOGIC
ELBIT COMPUTERS LTD
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
CODE IDENT C
DWG NO 89616400
REV J
SHEET 5 OF 9
R/R CLOCK
R/R CLOCK
P2B13 REJECT
P2B12 REPLY
INTRPT / MODE LOGIC
RDEN
WDEN
DSEN
DFEN
EOP
CSRMODE
EOP DFEN
CSCINT DFEN
CSCON
CCON + MC
READ
WRITE
MC
FROM RDA
VCC

TTY CONTROLLER (drawing 89616400, sheet 6)

CONTROL AND INTERRUPT LOGIC

Function

This circuit generates an interrupt signal for the End-of-Operation (EØP), ALARM, DATA and Manual interrupt conditions.

It also contains a number of control flip-flops and generates the associated signals:

Flip-flop	Signal
READ/WRITE, MØDE	WMØDE, RMØDE
DATA READ, LØST DATA	$\overline{\text{RDA}}$, LØST DATA(LD)
MECH BUSY	BUSY, EØP, DATA, $\overline{\text{MECH•BUSY}}$

Inputs

SIGNAL	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{\text{MNL•INTRPT}}$	L	P2A13	Manual Interrupt from Programmer's console	6	C-4
$\overline{\text{MNL•INTRPT}}$	L	P1A05		6	C-4

Outputs

$\overline{\text{CHI}}$	L	P2B25	Character Input	6	A-3
$\overline{\text{INTIL}}$	L	P2A12	Interrupt (EØP)	6	D-1

NOTE: Sheet 6 on page 5-395 differs from some older revisions in the following areas:

* zone C-3: the Manual Interrupt flip-flop is U5/11, type 242H
* zone C-4: 68NF capacitor C16 is not connected between signal $\overline{\text{MNL INTRPT}}$ at P2A13/P1A05 and ground.

The Interrupt Circuit

Each of the interrupt conditions (DATA, EØP, ALARM) is set by the corresponding director function (A02, A03, A04) together with the signal DFEN, and is latched in the corresponding D-type flip-flop (part of U2). The interrupt conditions are reset by the Clear Interrupt ($\overline{CLEAR}$). The latches (U2) are clocked by $\overline{DF} = \overline{WRITE \cdot MC}$. When the latch output (interrupt enable) coincides with the corresponding signal, an interrupt signal is produced at the output of U6. The Manual Interrupt signal (from the MANUAL INTERRUPT pushbutton on the Programmer's Console) sets the manual interrupt flip-flop (U5) and also sets the interrupt signal through U6. The following table summarizes the action of this circuit:

Interrupt Condition	Director Function	Gate	Latch Terminals
Data	A02	U36/6	U2/4,3
EØP	A03	U21/8	U2/12,11
ALARM	A04	U21/6	U2/5,6
Manual	---	U5/11	---

Note: ALARM INTERRUPT = PE·DATA·READ + LØST DATA
that is when a parity error is detected on input data or data is lost.

The output of gate U6 is used as the interrupt status bit in the A/Q channel data path logic circuit (sheet 2); its inverse (U56/11) is transmitted to the CPU.

Control flip-flops

The Read/Write gate (U36/8) forms a latch with U2/13, 14 to produce the clocked mode signals WMØDE and RMØDE used in the control and teletype interface circuit (sheet 3). It is set by the director function A08, ANDed with EØP and DFEN and reset by $\overline{RESET}$ from the address decoding and reply/reject circuit (sheet 5).

TTY CONTROLLER (drawing 89616400, sheet 6, cont'd.)

The Data Read flip-flop (U43) stores the information showing that a character has been received from the peripheral device. It is preset by the function

$$DA \cdot RM\emptyset DE \cdot \overline{LD} \cdot \overline{MECHBUSY}$$

Where

- RMØDE means that the controller is in Read Mode
- DA is an output of U22 in the A/Q channel data path logic
- $\overline{LØST\ DATA}$, ($\overline{LD}$) is an output from flip-flop U9 and means that a character has been received by the controller and not transferred to the CPU
- $\overline{MECHBUSY}$ (output from flip-flop U43) means that the controller is sending a character to the peripheral device.

The data read flip-flop is cleared by the rising edge of the signal from U28 and it is asynchronously cleared by $\overline{CCØN+MC}$ or $\overline{LØST\ DATA}$ at R.

The flip-flop Lost Data (U9) is clocked by the rising edge of the signal.

$$DATAREAD \cdot \overline{MECHBUSY} \cdot \emptyset R$$

(output of U29), where ØR comes from the UAR/T of the A/Q channel data path logic.

The flip-flop is cleared asynchronously by $\overline{CCØN+MC}$ or $\overline{RMØDE}$ (U60/8).

The signal LØST DATA (LD) is used as a status bit in the A/Q channel data path logic.

The MechBusy flip-flop (U43) is set while data is transmitted to the controlled peripheral and is cleared when the transmission has been completed and the $\overline{WRITE}$ signal is no longer active.

Its actuating signals are as follows:

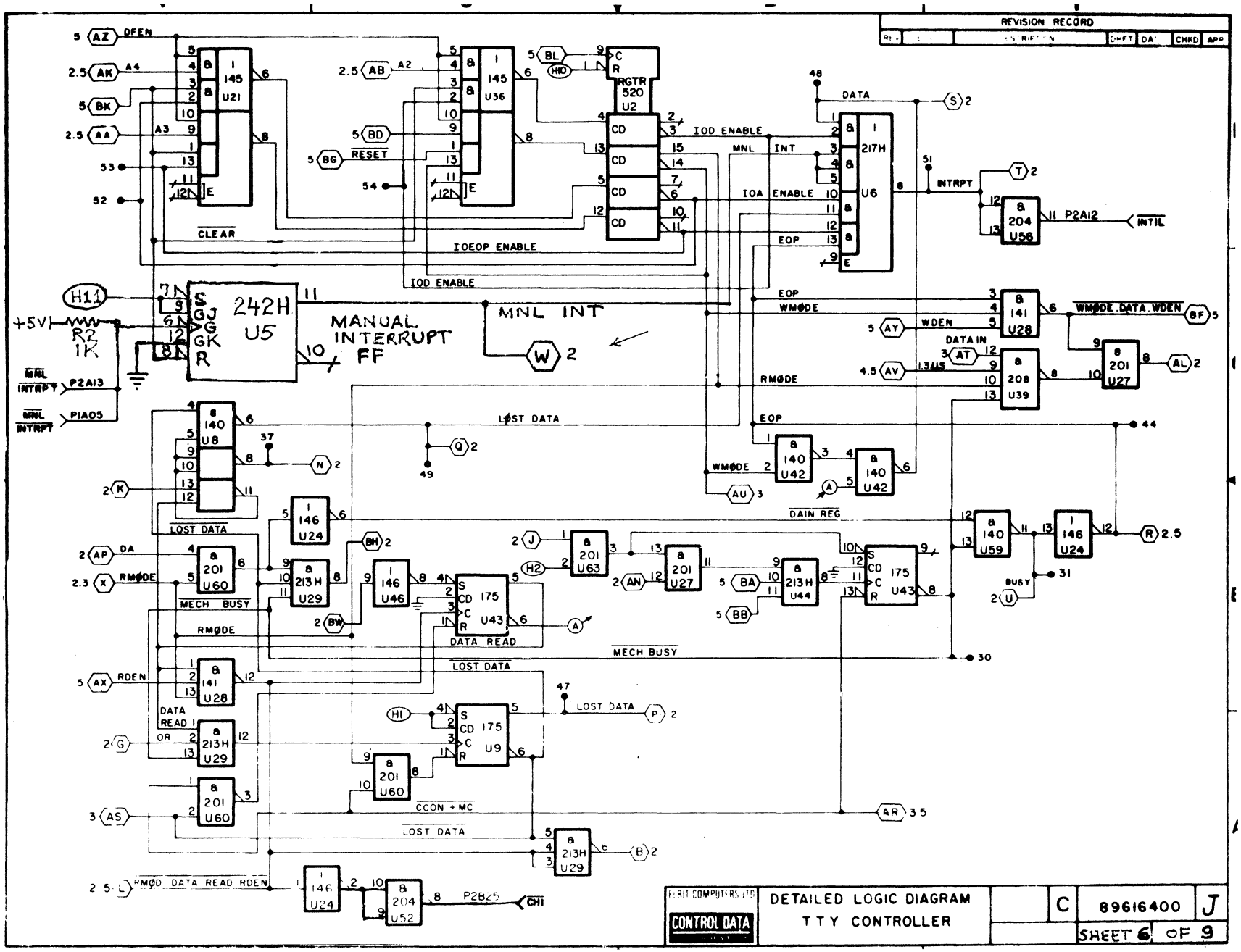
Set: by TBMT from the UAR/T to the A/Q channel data path (sheet 2)
Preset: $\overline{CCØN+MC}$
Clear: by rising edge of $E\emptyset C \cdot TBMT \cdot \overline{RDEN} \cdot \overline{WDEN}$

TTY CONTROLLER (Drawing number 89616400, sheet 6, cont'd)

Miscellaneous output signals are produced using the signals of the above flip-flops. These are:

Signal	Equation	Description/Remarks	Origin
$\overline{\text{RDA}}$	LOST DATA + CHI	to UAR/T of A/Q channel data path (sheet 2)	U29/6
$\overline{\text{CHT}}$	$\overline{\text{READ·DATAREAD}}$	Character Input prevents the most significant field of the CPU A register from being changed during a read data operation	U52/8
BUSY	MECHBUSY + DA·RMØDE	Status bit	U59/11
EØP	$\overline{\text{BUSY}}$	Status bit (End-of-Operation interrupt)	U24/12
DATA	EØP·WMODE + DATAREAD	Status bit (data interrupt)	U42/6
PARITY ERROR	$\overline{\text{PE·DATAREAD}}$	Status bit (data interrupt)	U8/11
ALARM	PARITY ERROR	Status bit (alarm interrupt)	U8/6
$\overline{\text{DS}}$·WRITE	EØP·WMØDE·WDEN	Active after transmission of character used in the UAR/T of the A/Q channel data path (sheet 2) timed by 1.3 µsec signal.	U28/6

NOTE: $\overline{\text{DS}}$ = EØP WMODE WDEN + DATAIN RMODE MECHBUSY (1.3 µsec) at U27/8.



TTY Controller Logic Diagram 89616400, Sheet 6, Controller and Interrupt Logic

TTY CONTROLLER (drawing number 89616400 sheets 7,8)

BREAKPOINT LOGIC

Function

The breakpoint logic generates the signal BEA when the data sent to the memory address register is identical to the data stored in the breakpoint register. This circuit also contains logic for buffering signals between the CPU and the Programmer's Console.

INPUTS (Sheet 7)

SIGNALS	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
$\overline{\text{CNS08}}$	L	P1A14		7	B-4
$\overline{\text{CNS09}}$	L	P1B15		7	B-4
$\overline{\text{CNS10}}$	L	P1B14		7	B-4
$\overline{\text{CNS11}}$	L	P1A15		7	B-4
$\overline{\text{CNS12}}$	L	P1B03		7	D-4
$\overline{\text{CNS13}}$	L	P1A03		7	D-4
$\overline{\text{CNS14}}$	L	P1A04		7	D-4
$\overline{\text{CNS15}}$	L	P1B05		7	D-4
CSB	H	P1B16		7	B-4
$\overline{\text{CRQ}}$	L	P2B05		7	B-4
32KW	-	P1B04		7	A-4
$\overline{\text{SGI}}$	L	P2B01		7	B-1
GØCS	H	P2B02		7	B-1
$\overline{\text{PEL}}$	L	P2A07		7	A-1
$\overline{\text{RNI}}$	L	P2B04		7	A-1

OUTPUTS (Sheet 7)

BEA	H	P1A02		7	C-1
SEN	H	P1A19		7	B-1
PEIND	H	P1A17		7	A-1
RNIB	H	P1B20		7	A-1

TTY CONTROLLER (drawing number 89616400 sheets 7,8 cont'd.)

BREAKPOINT LOGIC

Inputs (sheet 8)

SIGNALS	ACTIVE	CONNECTOR PIN	FUNCTION	LOCATION SHEET	LOCATION SQUARE
BCK	H	P1B02		8	D-4
$\overline{\text{CLRB}}$	L	P1A16			D-4
$\overline{\text{CNS00}}$	L	P1B17			B-4
$\overline{\text{CNS01}}$	L	P1B19			B-4
$\overline{\text{CNS02}}$	L	P1A18			B-4
$\overline{\text{CNS03}}$	L	P1A20			B-4
$\overline{\text{CNS04}}$	L	P1A07			D-4
$\overline{\text{CNS05}}$	L	P1A06			D-4
$\overline{\text{CNS06}}$	L	P1B13			D-4
$\overline{\text{CNS07}}$	L	P1A13			D-4
$\overline{\text{INDIND}}$	L	P2A18			B-1
$\overline{\text{ØVFL}}$	L	P2A01			A-1
EINT	H	P2B03		8	A-1

Outputs (sheet 8)

ADDR	H	P1A12		8	B-1
ØVFL	H	P1B21		8	A-1
EINTB	H	P1B18		8	A-1

TTY CONTROLLER (drawing number 89616400 sheets 7, 8 cont'd)

BREAKPOINT LOGIC

Description

The inputs CNS00 through CNS15 are passed to two registers. One is an address register (latches U34 and U35). This register is enabled by the signal CRQ. The other one is the breakpoint register. This is made up of four-bit D type flip-flops, U50, U49, U48 and U33 clocked by BCK and cleared by CLRB. The active high outputs of the breakpoint register are gated by CSB in open-collector NAND gate buffers (U67, U47, U65 and U32).

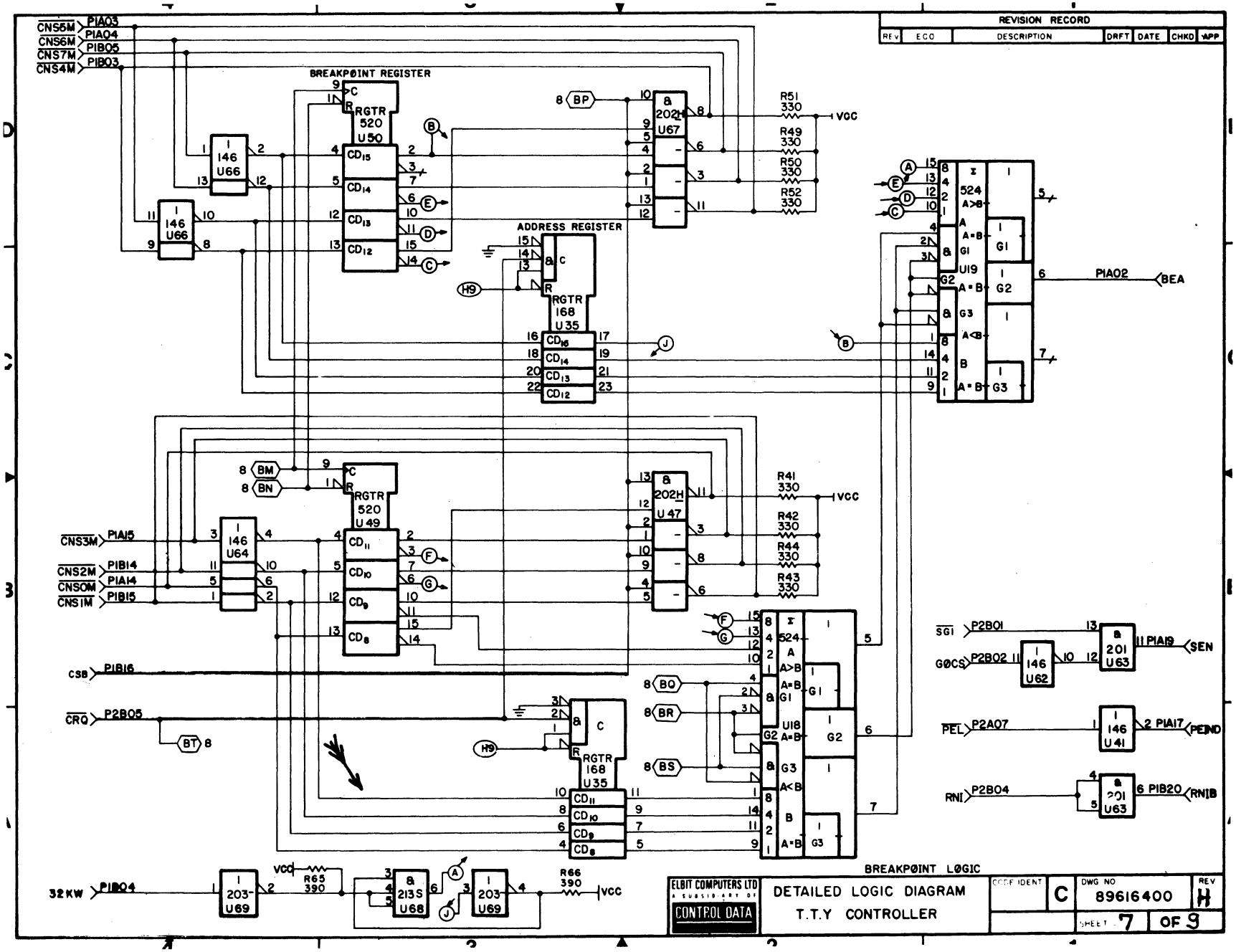
The outputs of these open-collector NAND gates are fed back to the inputs of the breakpoint register. This circuit allows the contents of the breakpoint register to be set from the front panel switches. The contents of the breakpoint register and the address latches (U35 and U34) are compared by the comparators (U16, U17, U18 and U19). If all 16 bits of the two registers are equal, the comparators generate the signal BEA.

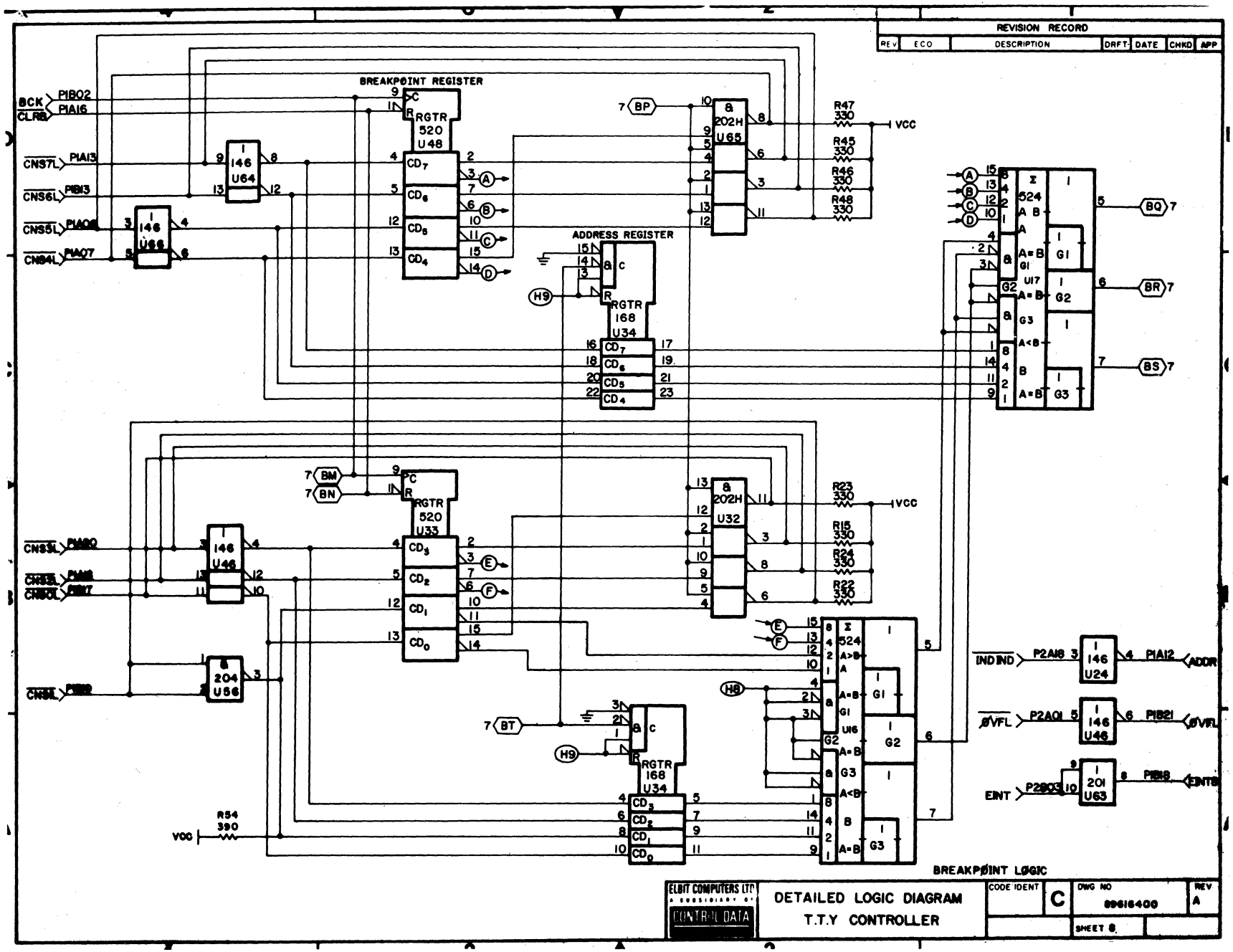
NOTE

Sheet 7 on page 5-399 differs from some older revisions in the following area:

* zone A-3: AND-gate U68/3,4,5-6 is type 213S.

Sheet 8 on page 5-400 does not differ from older revisions.


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
BREAKPOINT REGISTER
ADDRESS REGISTER
RGTR 520 U50
RGTR 168 U35
RGTR 520 U49
RGTR 168 U35
202H U67
202H U47
524 A>B
524 A<B
524 A=B
U19
U18
146 U66
146 U64
146 U62
146 U41
201 U63
203 U69
213S U68
R51 330
R49 330
R50 330
R52 330
R41 330
R42 330
R44 330
R43 330
R65 390
R66 390
VCC
CNS6M PIA03
CNS6M PIA04
CNS7M PIB05
CNS4M PIB03
CNS3M PIA15
CNS2M PIB14
CNSOM PIA14
CNS1M PIB15
CSB PIB16
CRQ P2B05
BT 8
32KW PIB04
PIA02 BEA
SGI P2B01
GØCS P2B02
PIA18 SEN
PEL P2A07
PEND
RNI P2B04
RNIB
BREAKPØINT LØGIC
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
CODE IDENT C
DWG NO 89616400
REV H
SHEET 7 OF 9


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
BREAKPOINT REGISTER
ADDRESS REGISTER
BCK PIB02
CLRB PIA16
CNS7L PIA13
CNS6L PIB13
CNS5L PIA06
CNS4L PIA07
CNS3L PIA02
CNS2L PIA12
CNS1L PIB12
CNS0L PIA17
RGTR 520 U48
RGTR 520 U33
RGTR 168 U34
146 U64
146 U66
146 U46
204 U56
202H U65
202H U32
524 U17
146 U24
146 U46
201 U63
R47 330
R45 330
R46 330
R48 330
R23 330
R15 330
R24 330
R22 330
R54 390
VCC
BQ
BR
BS
IND IND
P2A18
P1A12
ADDR
ØVFL
P2A01
P1B21
EINT
P2B05
P1B18
EINTR
BREAKPOINT LOGIC
ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
CODE IDENT C
DWG NO 89616400
REV A
SHEET 8

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
06	CK410	REDRAWN PER CDC STDS				
07 08 07 09 10 11	CK612 CK638 CK765 CK784 CK785 CK858	FACSIMILE				
A	CK1179	RELEASED CLASS A. ALL +5V REPL. BY VCC.				
B	CK1228	OFF-SHEET REF "BV" ADDED. SH2 "AP" REPL BY U68 U68 WAS 213H. FITS ASSY 89942700.				
C	CK1241	CK1228 CANCELLED. COMBINED WITH CK1241. SAME CHANGES THAT APPEAR IN CK1228 APPEAR IN CK 1241.				
D	CK828	REVERSE CHANGES TO U5 & U7 IN ECO 612.				
E	CK1268	U22-19/U60-4 REPLACES U22-19/U68-1,2; U29-8/ U68-1,2 REPLACES U29-8/U46-9; U68-12/U46-9 REPLACES U68-12/U60-4.				
F	CK1422	FITS PWA 89976400. INCORPORATES REWORK OF CK1268 & DELETES OSCILLATOR REWORK OF CK858. U68 IS 74H11.				
G	CK1446	FITS PWA 89984700. INCORPORATES REWORK OF CK1268. U68 IS 74H11.				
H	CK1447	REVISION RECORD: U68 WAS 213H. FITS PWA 89947600.				
J	CK1448	SH2, C-3: U7-8,9,10 REPLACES U5-1,2,3. SH3, B-3: U5 74H106 REPLACES U7 SH4, B-1: U7-11,12,13 REPLACES U5-4,5,6 SH5, A-4: CONN. U45-9/U39-6 REPL. BY U45-9/U56-5 SH6, C-3: U5 7400 REPL. BY U5 74H106 C-4: C16 DELETED				

S LTD
OF
TA
OF

DETAILED LOGIC DGM.
T.T.Y. CONTROLLER

CODE IDENT	DWG NO	REV
C	89616400	J
	SHEET 9	

TTY CONTROLLER (PWA 89947600, logic diagram 89616400, revision H)

The logic diagrams and logic descriptions for PWA 89947600, logic revision H, pages 5-402 through 5-409, are basically the same as for PWA 89967400, logic revision J, pages 5-374 through 5-401.

The sheets of logic revision H are located on the following pages of this manual:

sheet	1	2	3	4	5	6	7	8	9
page	5-403	5-404	5-405	5-406	5-407	5-408	5-399	5-400	5-409

PWA 89947600, logic revision H, differs from PWA 89967400, logic revision J in the following areas:

Sheet 1: Revision H matches P/N 89947600

Sheet 2: *zone B-4: U22/20 is connected to U22/21 (zone C-1)
*zone C-3: AND-gate type 140 is U5/2,1-3

Sheet 3: *zone B-3: the TTS flip-flop is U7/11, made up of two type-140 gates.
*zone C-4: the signal at P2A10 is not identified.

Sheet 4: *zone B-1: AND-gate type 140 is U5/5,4-6

Sheet 5: *zone C-4: U39/6 is connected to U5/9 (zone A-4)
*zone C-4: TP12 is connected to U39/6

Sheet 6: *zone C-3: the Manual Interrupt flip-flop is U5/11, made up of two type-140 gates
*zone C-4: 68NF capacitor C16 is connected between signal $\overline{\text{MNL INTRPT}}$ at P2A13/P1A05 and ground.

Sheet 9: revision record H

The logic descriptions for revision J also apply to revision H.

ØFF SHEET REFERENCE

OFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4	5	6	7	8
A	B-4		B-1				
B	B-4				A-3		
D	B-4			B-1			
F	B-4	C-3					
G	A-4				A-4		
J	C-1				B-3		
K	A-4				B-4		
L	C-3			C-1	A-4		
M	C-4			C-3			
N	C-3				C-4		
P	B-3				A-3		
Q	B-3				C-3		
R	B-3			C-2	B-1		
S	B-3				D-1		
T	A-3				D-1		
U	A-3				B-1		
V	C-3			C-3			
W	C-3				C-4		
X	C-3	C-3			B-4		
Y	D-2	B-4		C-2			
Z	C-2	B-4		C-2			
AA	C-2			C-2	D-4		
AB	C-2			C-2	D-3		
AC	C-1			B-2			
AD	C-1			B-2			
AF	B-1			B-2			
AG	B-1	C-2		D-2			
AJ	B-1			C-2			
AK	B-1			C-2	D-4		
AL	C-1				C-1		
AM	C-1	D-3					
AN	C-1				B-2		
AP	A-4				B-4		
AQ		B-4		B-2			
AR		B-3		B-1	A-2		
AS		C-3			A-4		
AT		C-3			C-1		
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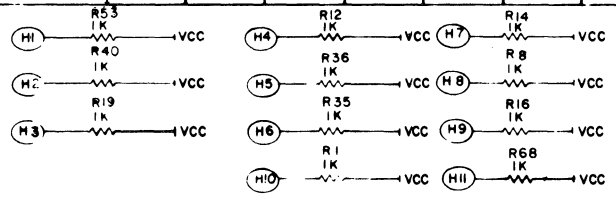

SHEET REV. STATUS

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C	B	A	B	B	A	B	A			
D	D	D	B	B	D	B	A			
E	E	D	B	B	E	B	A	E		
F	F	D	F	B	E	F	A	F		
G	F	D	G	B	E	F	A	G		
H	H	D	H	B	E	H	A	H		

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
H		SEE PAGE 9				

	2	3	4	5	6	7	8
AV			D-1	D-3	C-1		
AX				C-3	B-4		
AY				C-3	C-1		
AZ				B-2	D-4		
BA				D-2	B-2		
BB				C-3	B-2		
BD				C-2	D-3		
BF				C-1	C-1		
BG				B-1	D-3		
BH	A-4				B-3		
BK				B-1	D-4		
BL				B-1	D-3		
BM						C-4	B-3
BN						B-4	B-3
BP						D-3	D-2
BQ						B-2	C-1
BR						A-2	C-1
BS						A-2	C-1
BT						A-4	A-3
BU			A-3	A-2			
BV	A-4			D-3			
BW	A-3				B-3		

NØTE ALL UNMARKED RESISTØRS ARE 025 WATT 5%

P/N 89947600

AW 89616300
AY 89947600
DETACHED LISTS

DO NOT SCALE DRAWING

MATERIAL

FINISH

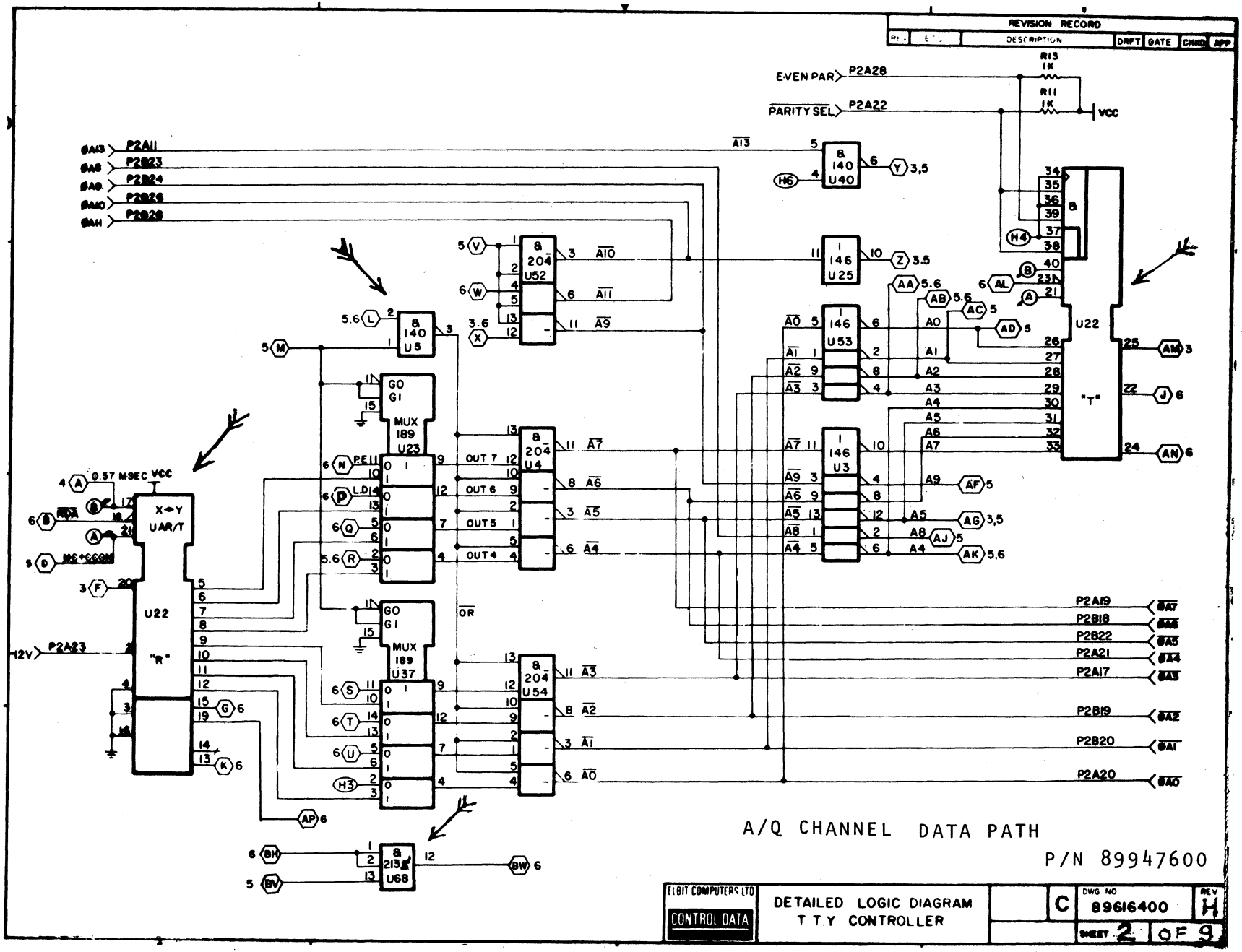
ELBIT COMPUTERS LTD
CONTROL DATA CORPORATION

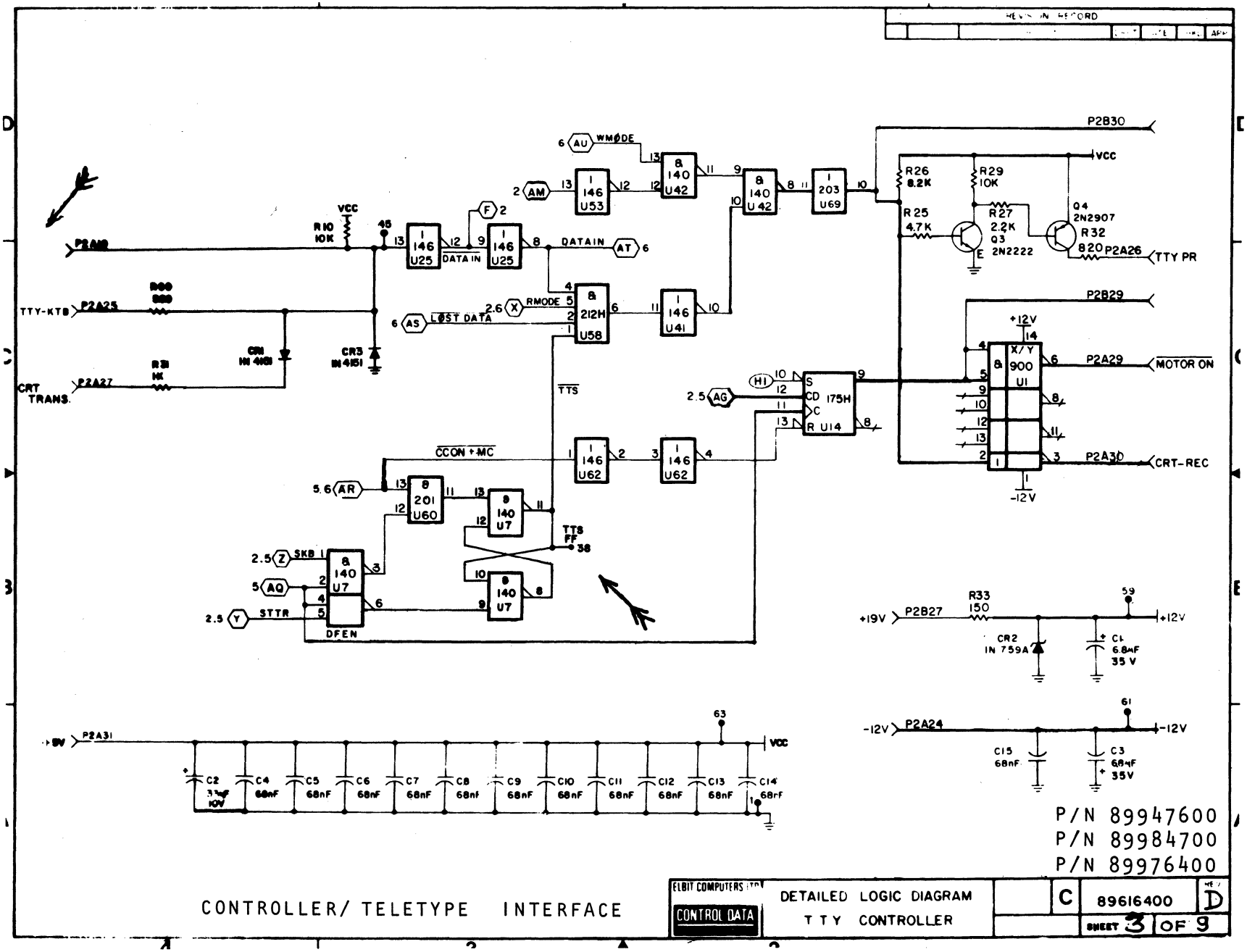
AB 107-A
AB 108-A

TITLE
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER

DRAWN H.Z.
CHKD HAIM J.
APPD
DATE May 78

SIZE C
DRAWING NO 89616400
SHEET 1 OF 9


REVISION RECORD
DESCRIPTION
DRFT
DATE
CHKD
APP
EVEN PAR P2A28
PARITY SEL P2A22
R13 1K
R11 1K
VCC
P2A11
P2B23
P2B24
P2B25
P2B26
U40
U25
U53
U22
"T"
U5
U52
U4
U3
U54
U23
U37
MUX 189
GO
G1
OUT 7
OUT 6
OUT 5
OUT 4
OR
U22
"R"
X↔Y UAR/T
0.57 MSEC VCC
12V P2A23
P2A19
P2B18
P2B22
P2A21
P2A17
P2B19
P2B20
P2A20
U68
A/Q CHANNEL DATA PATH
P/N 89947600
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
T T Y CONTROLLER
C
DWG NO 89616400
REV H
SHEET 2 OF 9



P/N 89947600
P/N 89984700
P/N 89976400

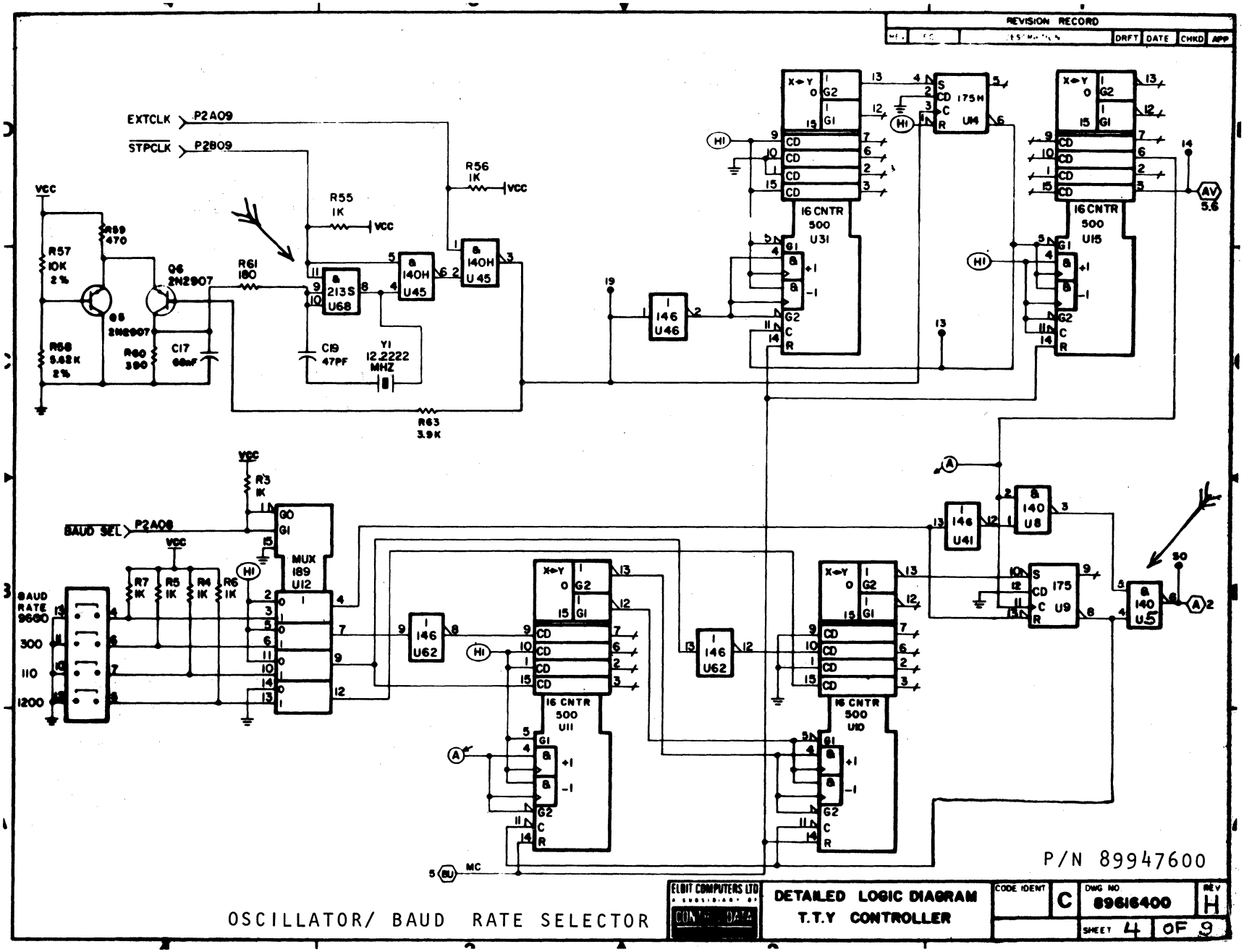
CONTROLLER/ TELETYPE INTERFACE

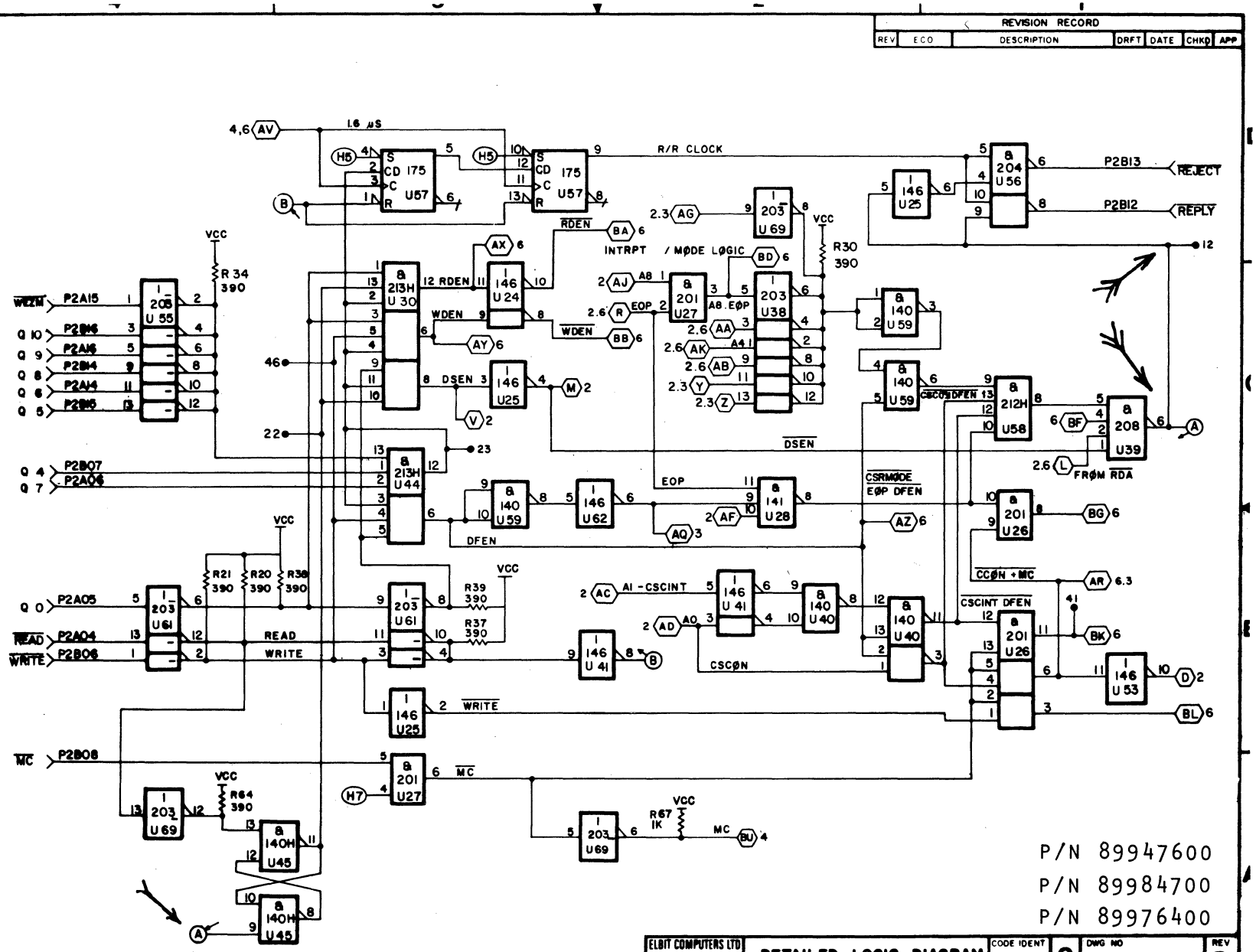
ELBIT COMPUTERS LTD
CONTROL DATA

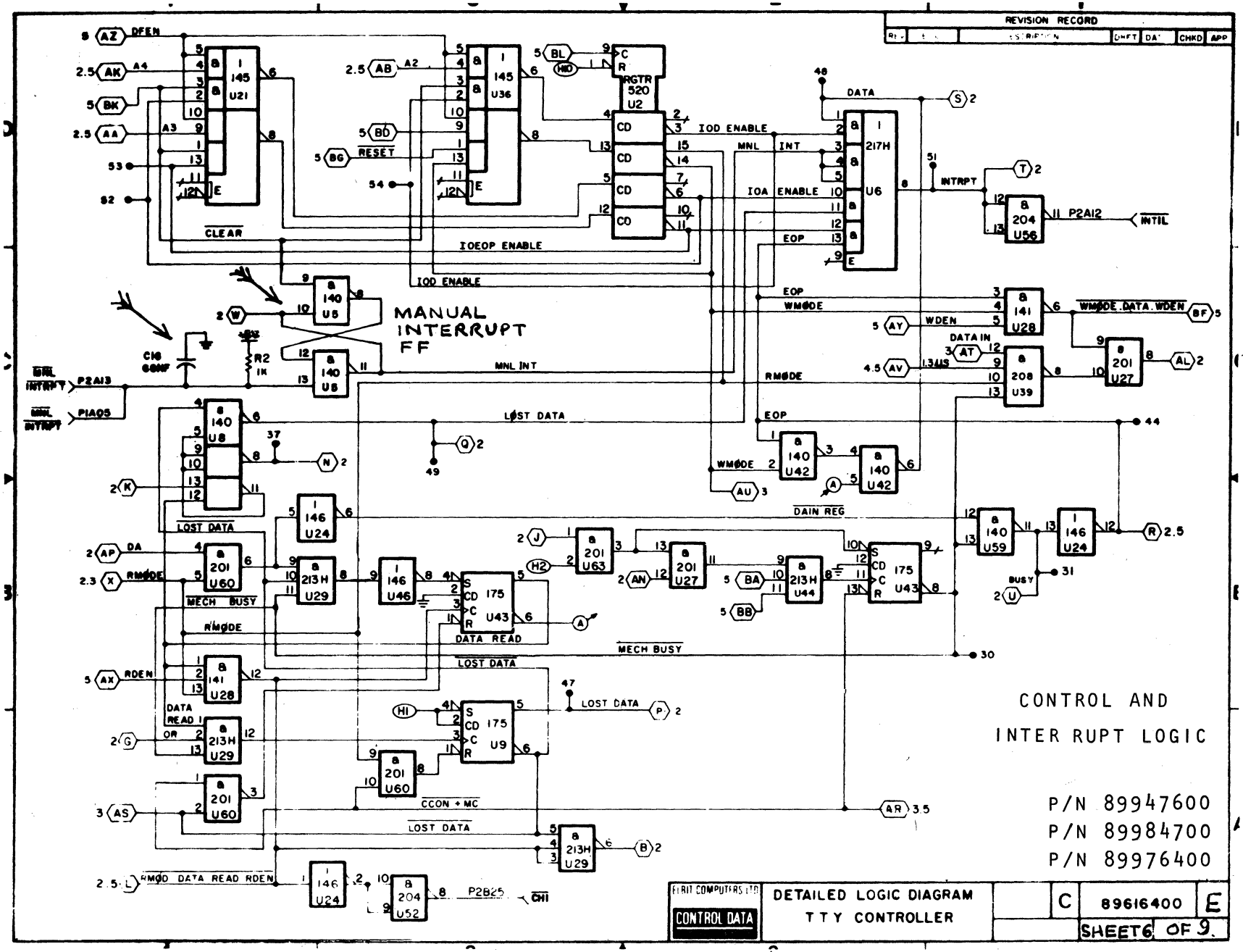
DETAILED LOGIC DIAGRAM
T T Y CONTROLLER

C 89616400 D

SHEET 3 OF 9


REVISION RECORD
EXTCLK P2A09
STPCLK P2B09
VCC
R57 10K 2%
R59 470
R58 5.62K 2%
R60 390
C17 68nF
Q6 2N2907
Q5 2N2907
R61 180
R55 1K
R56 1K
R63 3.9K
8 213S U68
8 140H U45
8 140H U 45
C19 47PF
Y1 12.2222 MHZ
1 146 U46
X=Y 0 G2 1 G1 15
S CD 175H C R U14
16 CNTR 500 U31
16 CNTR 500 U15
HI
AV 5.6
BAUD SEL P2A09
R3 1K
R7 1K
R5 1K
R4 1K
R6 1K
MUX 189 U12
BAUD RATE 9600 300 110 1200
1 146 U62
1 146 U41
8 140 U8
S CD 175 C R U9
8 140 U5
16 CNTR 500 U11
16 CNTR 500 U10
A
A2
MC
P/N 89947600
OSCILLATOR/ BAUD RATE SELECTOR
ELBIT COMPUTERS LTD
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
CODE IDENT C
DWG NO 89616400
REV H
SHEET 4 OF 9


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
1.6 µS
R/R CLOCK
P2B13 REJECT
P2B12 REPLY
INTRPT / MODE LOGIC
RDEN
WDEN
DSEN
EOP
DFEN
READ
WRITE
CSCØN
CSCINT DFEN
CSRMØDE EØP DFEN
CCØN + MC
FRØM RDA
VCC
R34 390
R30 390
R21 390
R20 390
R38 390
R39 390
R37 390
R64 390
R67 1K
P/N 89947600
P/N 89984700
P/N 89976400
ADDRESS DECODING - REPLY/ REJECT LOGIC
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
CODE IDENT C
DWG NO 89616400
REV B
SHEET 5 OF 9


REVISION RECORD
MANUAL INTERRUPT FF
CONTROL AND INTER RUPT LOGIC
P/N 89947600
P/N 89984700
P/N 89976400
CONTROL DATA
DETAILED LOGIC DIAGRAM
TTY CONTROLLER
89616400
SHEET 6 OF 9.

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
06	CK410	REDRAWN PER CDC STDS				
07 08 07 09 10 11	CK612 CK638 CK765 CK784 CK785 CK858	FACSIMILE				
A	CK1179	RELEASED CLASS A. ALL +5V REPL. BY VCC.				
B	CK1228	OFF-SHEET REF "BV" ADDED. SH2 "AP" REPL BY U68 U68 WAS 213H. FITS ASSY 89942700.				
C	CK1241	CK1228 CANCELLED. COMBINED WITH CK1241. SAME CHANGES THAT APPEAR IN CK1228 APPEAR IN CK 1241.				
D	CK828	REVERSE CHANGES TO U5 & U7 IN ECO 612.				
E	CK1268	U22-19/U60-4 REPLACES U22-19/U68-1,2; U29-8/ U68-1,2 REPLACES U29-8/U46-9; U68-12/U46-9 REPLACES U68-12/U60-4.				
F	CK1422	FITS PWA 89976400. INCORPORATES REWORK OF CK1268 & DELETES OSCILLATOR REWORK OF CK858. U68 IS 74H11.				
G	CK1446	FITS PWA 89984700. INCORPORATES REWORK OF CK1268. U68 IS 74H11.				
H	CK1447	REVISION RECORD: U68 WAS 213H. FITS PWA 89947600.				

P/N 8994 7600

LTD OF		CODE IDENT		DWG NO	REV
A	DETAILED LOGIC DGM. T.T.Y. CONTROLLER		C	89616400	H
				SHEET 9	

TTY CONTROLLER (PWA 89984700, logic diagram 89616400, revision G)

The logic diagrams and logic descriptions for PWA 89984700, logic revision G, pages 5-410 through 5-415, are basically the same as for PWA 89947600, logic revision H, pages 5-402 through 5-409.

The sheets of logic revision G are located on the following pages of this manual:

sheet	1	2	3	4	5	6	7	8	9
page	5-411	5-412	5-405	5-413	5-407	5-408	5-414	5-400	5-415

PWA 89984700, logic revision G, differs from PWA 89947600, logic revision H, in the following areas:

Sheet 1: Revision G matches PWA 89984700.
Sheet 2: *zone A-3: AND-gate U68 is type 213H
Sheet 4: *zone C-3: AND-gate U68 is type 213H
Sheet 7: *zone A-3: AND-gate U68 is type 213H
Sheet 9: revision record G

The logic descriptions for revisions J and H also apply to revision G.

89633300 E

ØFF SHEET REFERENCE

OFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4	5	6	7	8
A	B-4		B-1				
B	B-4				A-3		
D	B-4			B-1			
F	B-4	C-3					
G	A-4				A-4		
J	C-1				B-3		
K	A-4				B-4		
L	C-3			C-1	A-4		
M	C-4			C-3			
N	C-3				C-4		
P	B-3				A-3		
Q	B-3				C-3		
R	B-3			C-2	B-1		
S	B-3				D-1		
T	A-3				D-1		
U	A-3				B-1		
V	C-3			C-3			
W	C-3				C-4		
X	C-3	C-3			B-4		
Y	D-2	B-4		C-2			
Z	C-2	B-4		C-2			
AA	C-2			C-2	D-4		
AB	C-2			C-2	D-3		
AC	C-1			B-2			
AD	C-1			B-2			
AF	B-1			B-2			
AG	B-1	C-2		D-2			
AJ	B-1			C-2			
AK	B-1			C-2	D-4		
AL	C-1				C-1		
AM	C-1	D-3					
AN	C-1				B-2		
AP	A-4				B-4		
AQ		B-4		B-2			
AR		B-3		B-1	A-2		
AS		C-3			A-4		
AT		C-3			C-1		
AU		D-2			C-2		

SHEET REV. STATUS

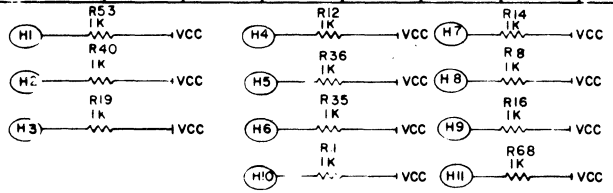
1	2	3	4	5	6	7	8	9	
A	A	A	A	A	A	A	A		
C	B	A	B	B	A	B	A		
D	D	D	B	B	D	B	A		
E	E	D	B	B	E	B	A	E	
F	F	D	F	B	E	F	A	F	
G	F	D	G	B	E	F	A	G	

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
G		SEE PAGE 9				

	2	3	4	5	6	7	8
AV			D-1	D-3	C-1		
AX				C-3	B-4		
AY				C-3	C-1		
AZ				B-2	D-4		
BA				D-2	B-2		
BB				C-3	B-2		
BD				C-2	D-3		
BF				C-1	C-1		
BG				B-1	D-3		
BH	A-4				B-3		
BK				B-1	D-4		
BL				B-1	D-3		
BM						C-4	B-3
BN						B-4	B-3
BP						D-3	D-2
BQ						B-2	C-1
BR						A-2	C-1
BS						A-2	C-1
BT						A-4	A-3
BU			A-3	A-2			
BV	A-4			D-3			
BW	A-3				B-3		

NØTE ALL UNMARKED RESISTØRS ARE 025 WATT 5%



P/N 899847 00

AW 89616300
AY 89967400
DETACHED LISTS

DO NOT SCALE DRAWING
MATERIAL

ELBIT COMPUTERS LTD
CONTROL DATA CORPORATION

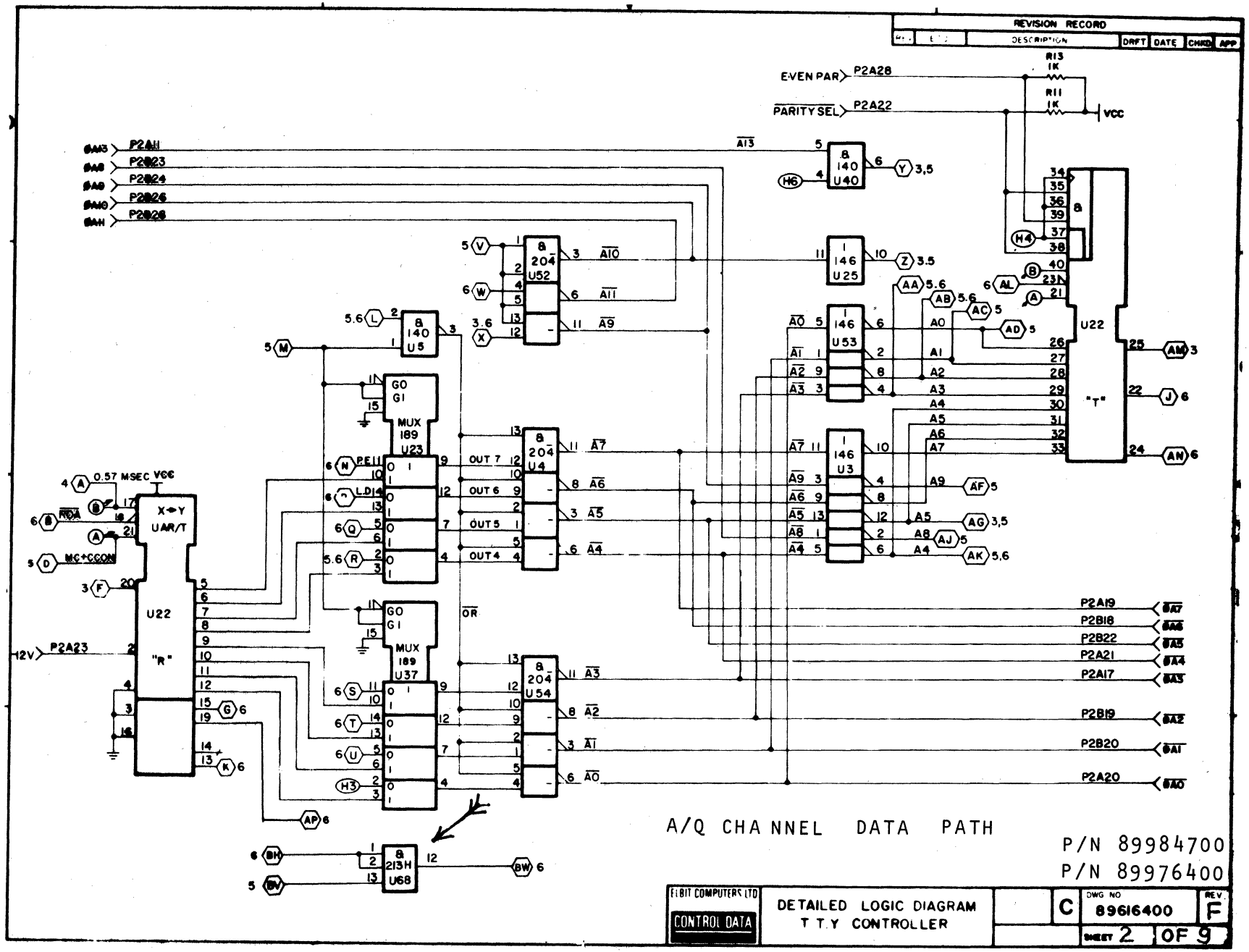
NEXT USED IN
AB 107 A
AB 108-A

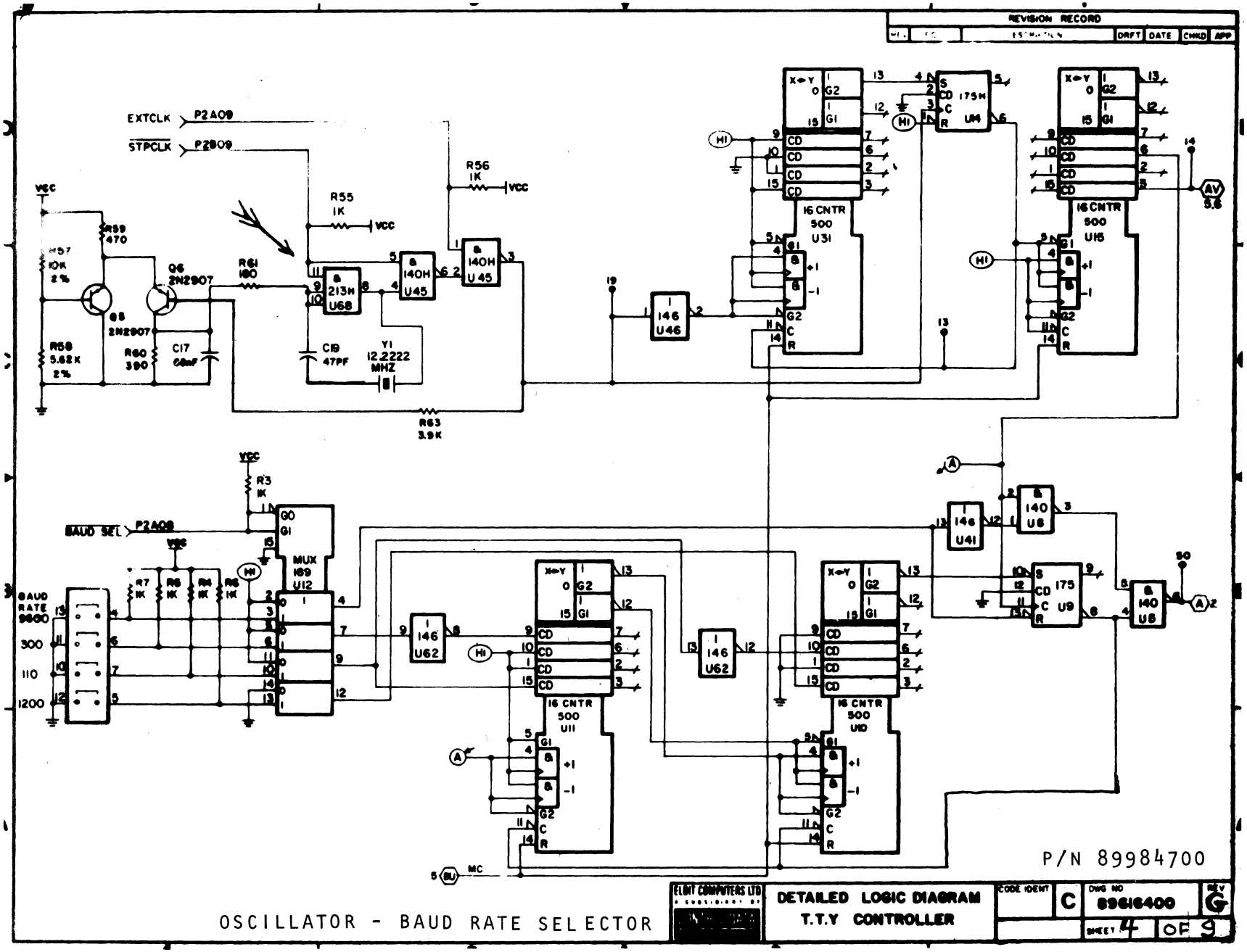
TITLE
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER

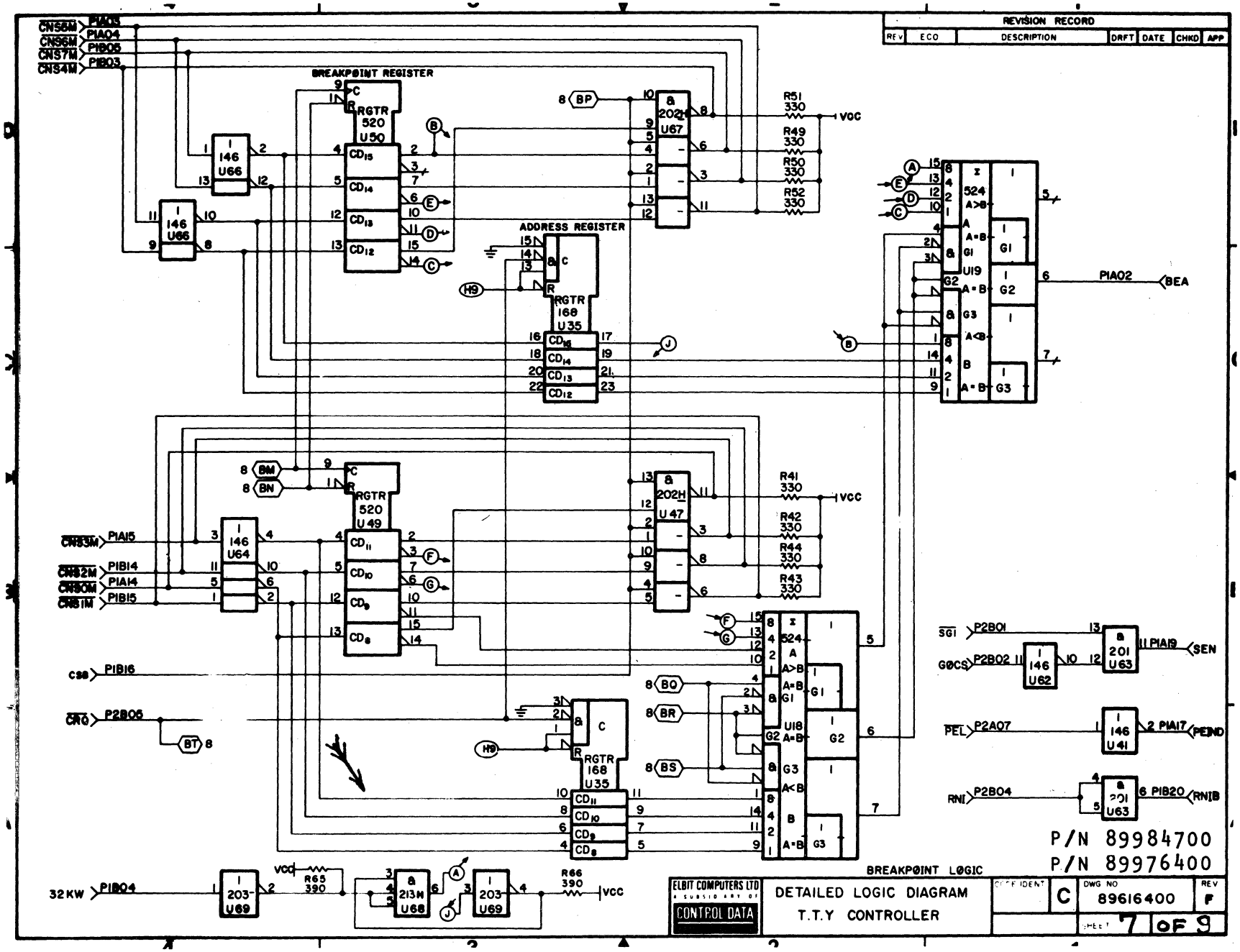
DRAWN
A. I.
CHKD
HAIM J.
May 78

SIZE C
DRAWING NO. 89616400
SHEET 1 OF 9

5-411


REVISION RECORD
DESCRIPTION
DRFT
DATE
CHKD
APP
EVEN PAR P2A28
PARITY SEL P2A22
R13 1K
R11 1K
VCC
P2A11
P2B23
P2B24
P2B26
P2B26
A13
8 140 U40
8 204 U52
8 140 U5
GO G1 MUX 189 U23
8 204 U4
GO G1 MUX 189 U37
8 204 U54
8 213H U68
1 146 U25
1 146 U53
1 146 U3
U22 "T"
U22 "R"
X↔Y UAR/T
0.57 MSEC VCC
MC+CCON
RDA
LDI
PE
OUT 7
OUT 6
OUT 5
OUT 4
OR
12V
P2A23
P2A19
P2B18
P2B22
P2A21
P2A17
P2B19
P2B20
P2A20
A/Q CHANNEL DATA PATH
P/N 89984700
P/N 89976400
FABIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
T T Y CONTROLLER
C
DWG NO 89616400
REV F
SHEET 2 OF 9


REVISION RECORD
DRFT
DATE
CHKD
APP
EXTCLK P2A09
STPCLK P2B09
VCC
R55 1K
R56 1K
R59 470
R57 10K 2%
Q6 2N2907
Q5 2N2907
R61 100
R58 5.62K 2%
R60 390
C17 68nF
C19 47PF
Y1 12.2222 MHZ
R63 3.9K
213H U68
140H U45
140H U45
146 U46
175H U4
16 CNTR 500 U31
16 CNTR 500 U15
AV 5.6
R3 1K
BAUD SEL P2A08
R7 1K
R8 1K
R4 1K
R5 1K
MUX 159 U12
BAUD RATE 9600
300
110
1200
146 U62
146 U62
16 CNTR 500 U11
16 CNTR 500 U10
146 U41
140 U8
175 U9
140 U6
A2
MC
P/N 89984700
OSCILLATOR - BAUD RATE SELECTOR
ELBIT COMPUTERS LTD
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
CODE IDENT C
DWG NO 89616400
REV G
SHEET 4 OF 9


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
BREAKPOINT REGISTER
ADDRESS REGISTER
RGTR 520 U50
RGTR 168 U35
RGTR 520 U49
RGTR 168 U35
R51 330
R49 330
R50 330
R52 330
R41 330
R42 330
R44 330
R43 330
R65 390
R66 390
VCC
PIA02
BEA
PIA19
SEN
PIA17
PEND
RNIB
P/N 89984700
P/N 89976400
BREAKPOINT LOGIC
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
DWG NO 89616400
REV F
SHEET 7 OF 9
5-414
89633300 E

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
06	CK410	REDRAWN PER CDC STDS				
07 08 07 09 10 11	CK612 CK638 CK765 CK784 CK785 CK858	FACSIMILE				
A	CK1179	RELEASED CLASS A. ALL +5V REPL. BY VCC.				
B	CK1228	OFF-SHEET REF "BV" ADDED. SH2 "AP" REPL BY U68 U68 WAS 213H. FITS ASSY 89942700.				
C	CK1241	CK1228 CANCELLED. COMBINED WITH CK1241. SAME CHANGES THAT APPEAR IN CK1228 APPEAR IN CK 1241.				
D	CK828	REVERSE CHANGES TO U5 & U7 IN ECO 612.				
E	CK1268	U22-19/U60-4 REPLACES U22-19/U68-1,2; U29-8/ U68-1,2 REPLACES U29-8/U46-9; U68-12/U46-9 REPLACES U68-12/U60-4.				
F	CK1422	FITS PWA 89976400. INCORPORATES REWORK OF CK1268 & DELETES OSCILLATOR REWORK OF CK858. U68 IS 74H11.				
G	CK1446	FITS PWA 89984700. INCORPORATES REWORK OF CK1268. U68 IS 74H11.				

P/N 89984700

LTD OF A N	DETAILED LOGIC DGM. T.T.Y. CONTROLLER	CODE IDENT	C	DWG NO 89616400	REV G
				SHEET 9	

TTY CONTROLLER (PWA 89976400, logic diagram 89616400, revision F)

The logic diagrams and logic descriptions for PWA 89976400, logic revision F, pages 5-416 through 5-419, are basically the same as for PWA 89984700, logic revision G, pages 5-410 through 5-415.

The sheets of logic revision F are located on the following pages of this manual:

sheet	1	2	3	4	5	6	7	8	9
page	5-417	5-412	5-405	5-418	5-407	5-408	5-414	5-400	5-419

PWA 89976400, logic revision F, differs from PWA 89984700, logic revision G, in the following areas:

Sheet 1: Revision F matches PWA 89976400.

Sheet 4: *zone C-4: The oscillator circuit contains 47 picofarad capacitor C20 and 180 ohm resistor R62 in the path of crystal Y1, and 0.47 nanofarad capacitor C18 to ground, on the input line to the base of transistor Q6.

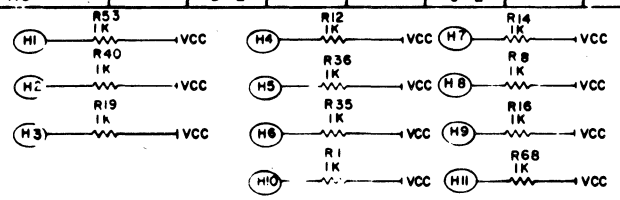
Sheet 9: revision record F.

Except for the change in the oscillator circuit on sheet 4 described above, the logic descriptions for revisions J, H, and G also apply to revision F.

89633300 E

ØFF SHEET REFERENCE

OFF SHEET REFERENCE LETTER	SHEET LØCATIØN 2	3	4	5	6	7	8
A	B-4		B-1				
B	B-4				A-3		
D	B-4			B-1			
F	B-4	C-3					
G	A-4				A-4		
J	C-1				B-3		
K	A-4				B-4		
L	C-3			C-1	A-4		
M	C-4			C-3			
N	C-3				C-4		
P	B-3				A-3		
Q	B-3				C-3		
R	B-3			C-2	B-1		
S	B-3				D-1		
T	A-3				D-1		
U	A-3				B-1		
V	C-3			C-3			
W	C-3				C-4		
X	C-3	C-3			B-4		
Y	D-2	B-4		C-2			
Z	C-2	B-4		C-2			
AA	C-2			C-2	D-4		
AB	C-2			C-2	D-3		
AC	C-1			B-2			
AD	C-1			B-2			
AF	B-1			B-2			
AG	B-1	C-2		D-2			
AJ	B-1			C-2			
AK	B-1			C-2	D-4		
AL	C-1				C-1		
AM	C-1	D-3					
AN	C-1				B-2		
AP	A-4				B-4		
AQ		B-4		B-2			
AR		B-3		B-1	A-2		
AS		C-3			A-4		
AT		C-3			C-1		
AU		D-2			C-2		



SHEET REV. STATUS

1	2	3	4	5	6	7	8	9	
A	A	A	A	A	A	A	A	A	
C	B	A	B	B	A	B	A		
D	D	D	B	B	D	B	A		
E	E	D	B	B	E	B	A	E	
F	F	D	F	B	E	F	A	F	

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
F		SEE PAGE 9				

	2	3	4	5	6	7	8
AV			D-1	D-3	C-1		
AX				C-3	B-4		
AY				C-3	C-1		
AZ				B-2	D-4		
BA				D-2	B-2		
BB				C-3	B-2		
BD				C-2	D-3		
BF				C-1	C-1		
BG				B-1	D-3		
BH	A-4				B-3		
BK				B-1	D-4		
BL				B-1	D-3		
BM						C-4	B-3
BN						B-4	B-3
BP						D-3	D-2
BQ						B-2	C-1
BR						A-2	C-1
BS						A-2	C-1
BT						A-4	A-3
BU			A-3	A-2			
BV	A-4			D-3			
BW	A-3				B-3		

NØTE ALL UNMARKED RESISTØRS ARE 025 WATT 5%

P/N 89976400

AW 89616300
AY 89976400

DETACHED LISTS

DO NOT SCALE DRAWING

MATERIAL

FINISH

ELBIT COMPUTERS LTD

CONTROL DATA

NEXT USED IN
AB 407 A
AB 108-A

DRAWN H.Z.

CHKD HAIM J.

APP'D May 78

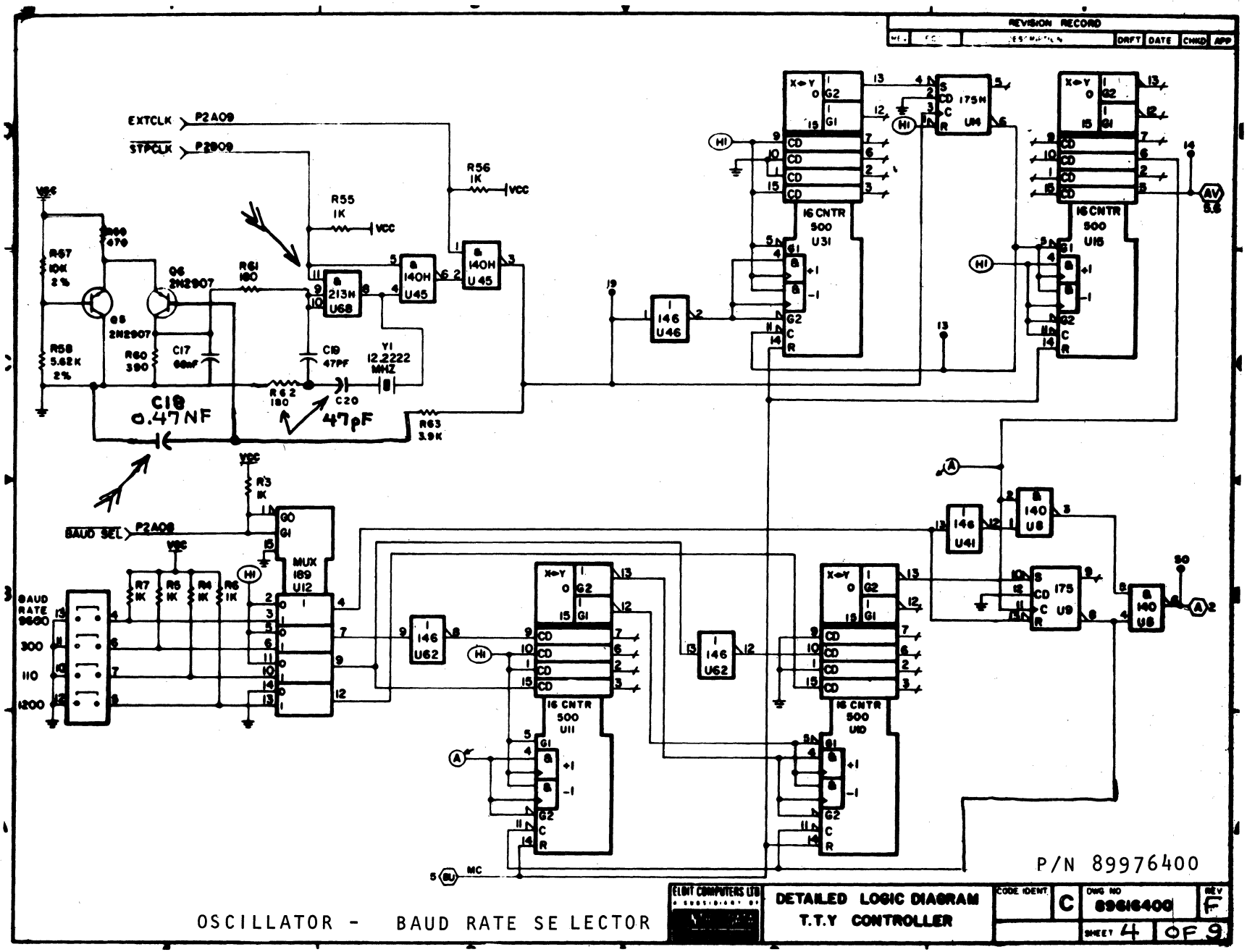
TITLE
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER

SIZE C

DRAWING NO. 89616400

SHEET 1 OF 9

5-417


REVISION RECORD
EXTCLK P2A09
STPCLK P2B09
BAUD SEL P2A08
R55 1K
R56 1K
R3 1K
R67 10K 2%
R58 5.62K 2%
R60 390
R61 180
R62 180
R63 3.9K
C17 68nF
C18 0.47NF
C19 47PF
C20 47pF
Y1 12.2222 MHZ
Q6 2N2907
Q8 2N2907
VCC
HI
MUX 189 U12
BAUD RATE 9600 300 110 1200
16 CNTR 500 U31
16 CNTR 500 U15
16 CNTR 500 U11
16 CNTR 500 U10
175H U14
175 U9
140H U45
213H U68
146 U46
146 U62
146 U41
140 U8
MC
AV
P/N 89976400
ELBIT COMPUTERS LTD
DETAILED LOGIC DIAGRAM
T.T.Y CONTROLLER
OSCILLATOR - BAUD RATE SE LECTOR
CODE IDENT. C
DWG NO 89616400
REV F
SHEET 4 OF 9

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
06	CK410	REDRAWN PER CDC STDS				
07	CK612	FACSIMILE				
08	CK638					
07	CK765					
09	CK784					
10	CK785					
11	CK858					
A	CK1179	RELEASED CLASS A. ALL +5V REPL. BY VCC				
B	CK1228	OFF-SHEET REF "BV" ADDED. SH2 "AP" REPL BY U68 U68 WAS 213H. FITS ASSY 89942700.				
C	CK1241	CK1228 CANCELLED. COMBINED WITH CK1241. SAME CHANGES THAT APPEAR IN CK1228 APPEAR IN CK 1241.				
D	CK828	REVERSE CHANGES TO U5 & U7 IN ECO 612.				
E	CK1268	U22-19/U60-4 REPLACES U22-19/U68-1,2; U29-8/ U68-1,2 REPLACES U29-8/U46-9; U68-12/U46-9 REPLACES U68-12/U60-4.				
F	CK1422	FITS PWA 89976400. INCORPORATES REWORK OF CK1268 & DELETES OSCILLATOR REWORK OF CK858. U68 IS 74H11.				

P/N 89976400

LTD OF TA ON DETAILED LOGIC DGM. T.T.Y. CONTROLLER	CODE IDENT	C	DWG NO 89616400	REV F
			SHEET 9	

ENCLOSURE POWER INPUT

The power supply and power input wiring of the main computer enclosure (equipments AB107/AB108) and that of the expansion enclosure (equipment BT148) are identical.

A Power Supply Input-Output Wiring Diagram shows the input power distribution in the equipment. The power line enters the enclosure through the line filter unit and is taken to the power supply unit (PSU) and the blowers through the PSU terminals. The PSU generates all internal supplies for the equipment.

The power supply wiring diagrams in this section apply to the following different equipments:

DRAWING NO.	PAGE NO.	EQUIPMENTS		
89762200	5-429	AB107-A04 to A12 AB108-A04 to A12	Part of BT148-A06 BT148-A05 and down	
89942600 *	5-431	AB107-A13 to A19 AB108-A13 to A19	Part of BT148-A06	
89911800 *	5-433	AB107-A10 to A15 AB108-A10 to A15	BT148-A07	
89601601	5-435	AB107-A16 and up AB107-C AB107-D	AB108-A16 and up AB108-C AB108-D	BT148-A08 up BT148-C BT148-D

The wire lists in section 9 give details on the interconnections.
The line filter unit and the power supply unit are described later in this section.

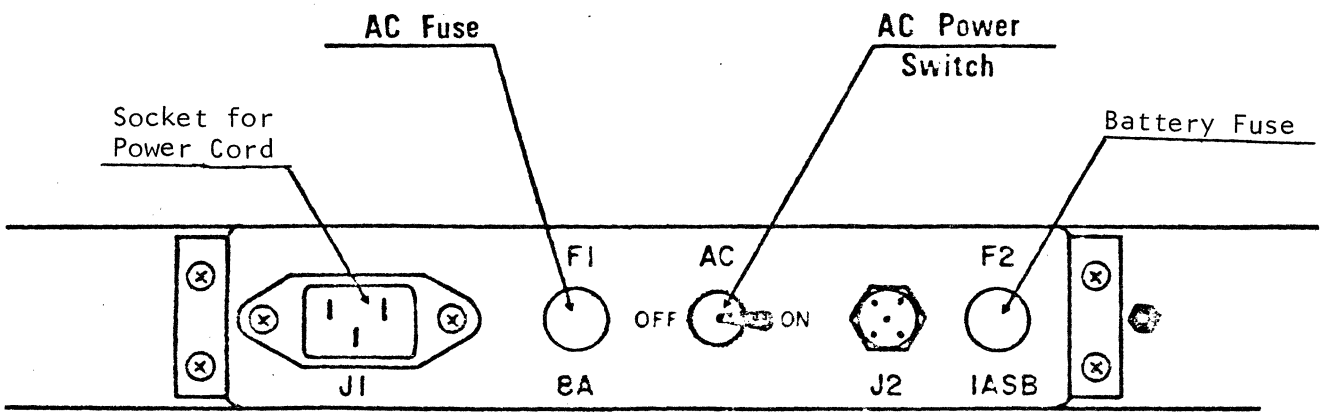
*In using wiring diagram 89911800 for the programmer's console connections in series A13, A14, A15, substitute the programmer's console connections of wiring diagram 89942600.

Note also that all series have one forced-air blower in the power supply and three axial fans installed in the top of the enclosure. Type identifiers C and D have two more fans, installed in the bottom of the enclosure.

THE POWER INPUT CIRCUIT

The input circuit of the enclosure (Line Filter Unit) is mounted at the top center of the rear panel. See figure 3-7 and the detail on this page. The following table summarizes the components and their functions.

DESIGNATION	NAME	FUNCTION
J1	Line power socket	Accommodates the line power cord
F1	Input fuse	Line protection
F2	Battery fuse	Battery protection
S1	AC line switch (on/off)	Applies ac line power to the equipment
FL1, FL2	Line filters	Isolate the equipment from surges and noises on the ac line
J2	Margin test socket	Used in the Margins test (Refer to section 6)



POWER SUPPLY UNIT (PSU)

The PSU is an autonomous assembly mounted at the top of the front door of the AB107/AB108 main computer enclosure and in the same place in the BT148 expansion enclosure. The PSU is part of the equipment which it supplies.

This sheet summarizes the circuit diagrams showing the power supply unit; the diagrams themselves are given in the following pages, together with a brief description of the circuit functions. All connectors for connecting the PSU to the rest of the AB107/AB108 or the BT148 equipment are brought out on the power supply connector panel on four terminal strips: TB1,TB2,TB3,TB6. These terminal strips are shown in a figure on one of the following pages.

The interconnection (wiring) diagrams show the interconnections between the main units of the power supply, including terminal strips, for all series of computers in the field.

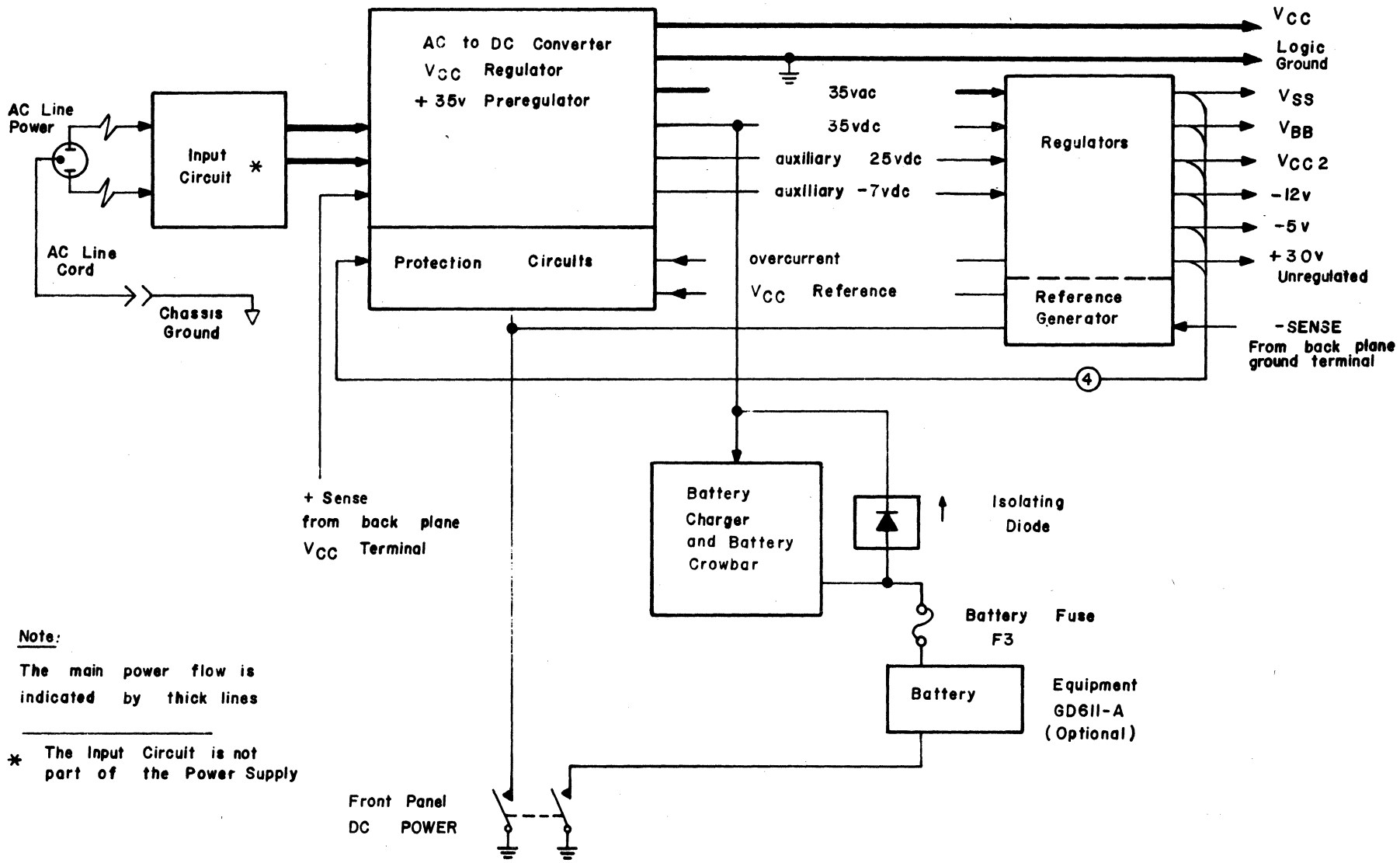
The power supply unit receives the main line power through the input circuit mounted at the rear of each enclosure. This input circuit, as well as the general power input connections to the enclosure, have already been presented.

The block diagrams of the PSU and their descriptions appear in section 4 of this manual. The diagrams are repeated in the following pages for convenience. Most of the circuitry of the PSU is mounted on two printed circuit boards within the power supply assembly, as follows:

BOARD DESIGNATION	DRAWING NO.	ASSOCIATED CIRCUITS
High Power (HP) and Control	89657700	Ac-to-dc converter, V_{cc} regulator, +35V preregulator, Protection and control circuits (except individual current limits)
Low Power (LP)	89640800	Regulators, individual current limit circuits, reference voltage generator, battery charge circuit

WARNING

The power supply does not use a main isolating line-transformer at its input. Its circuits between the ac line input and the isolating networks are therefore at line voltage. Do not handle the PSU while the computer line cord is connected to the ac supply.



Note:

The main power flow is indicated by thick lines

* The Input Circuit is not part of the Power Supply

POWER SUPPLY BLOCK DIAGRAM

POWER SUPPLY UNIT (continued)

COMPUTER DC SUPPLIES

Supply No.	Designation	Nominal voltage volts	Nominal Current	Remarks
1.	V_{cc}	+5	35A	R
2.	V_{cc2}	+5.3	3A	R,M
3.	V_{SS}	+16.7	5A	AB107/BA201-B,R,M
	V_{SS}	+19.7	5A	AB108/BA201-A,R,M
4.	V_{BB}	V_{SS} + 3.5	40mA	R, M
5.	-12V	-12	100mA	R,
6.	-5V	-5	1A	R
7.	+30V	+30	300mA	unregulated, M
8.	battery charger		200mA	current regulated
Internal supplies				
9.	+35V	+35		preregulated
10.	auxiliary no. 1	+25		unregulated
11.	auxiliary no. 2	-7		unregulated internal supply

NOTES:

R: regulated supply M: supply to the memory only

The tolerance on all regulated voltages is $\pm$ 0.5 percent.

The maximum permissible ripple is $\pm$ 2 percent of each regulated voltage.

See also table 6-1.

Use adjustment V_{BB} to adjust V_{SS}.

POWER SUPPLY WIRING DIAGRAMS

These drawings show the circuits of the complete power supply units for all computer series. The circuits accommodated on the two main printed circuit boards are shown on separate circuit diagrams. High Power and Control (HP) drawing number 89657700 and Low Power (LP) drawing number 89640800.

Terminal connector strips TB1, TB2, TB3, and TB6 on the power supply connector panel provide the connections between the power supply unit and the other circuits of the computer. A following figure and figure 3-5 show the connector panel. The following table lists the connections.

TABLE OF TERMINAL STRIP CONNECTIONS

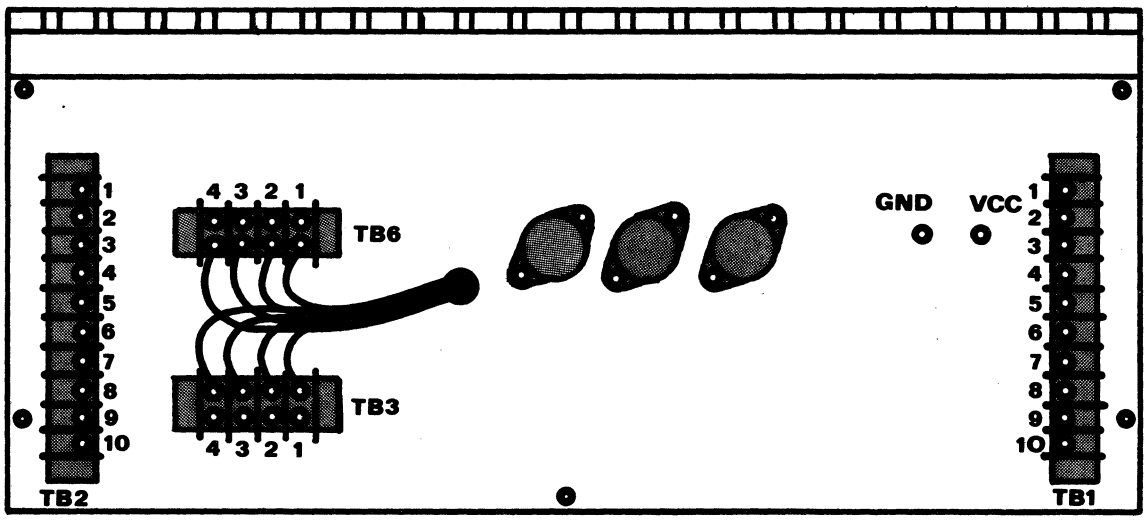
Connection	Designation	Connection/Function
TB-1/1	ON/OFF	Connection to programmer's console dc POWER on/off switch; controls power supply operation.
/2	+ SENSE	Sensing wire from $+V_{CC}$ connection on enclosure back-plane (Figure 3-7).
/3	$\overline{\text{RGPWR}}$	Power fail indicator signal for Low Power Data Retention (LPDR) operation (to Memory Control board).
/4	-SENSE	Sensing wire from logic ground on enclosure back-plane (Figure 3-7).
/5	-12V	-12V regulated supply output
/6	-5V	-5V regulated supply output
/7	+30V	+30V unregulated supply output
/8	V_{BB}	V_{BB} regulated supply output to Memory system
/9	V_{SS}	V_{SS} regulated supply output to Memory system
/10	V_{CC2}	V_{CC2} regulated supply output to Memory system

continued

POWER SUPPLY WIRING DIAGRAMS (continued)

TABLE OF TERMINAL STRIP CONNECTIONS (continued)

<table>
<tr><th>Connection</th><th>Designation</th><th>Connection/Function</th></tr>
<tr><td>TB-2/1</td><td>-</td><td rowspan="10">Main line voltage inputs from Input circuit:
<table><tr><th>Nominal voltage</th><th>Input to terminals</th><th>Shorting links (terminals)</th></tr><tr><td>110V</td><td>3, 7</td><td>1-2, 3-4-5, 6-7-8, 9-10</td></tr><tr><td>220V</td><td>3, 7</td><td>2-3, 5-6, 8-9</td></tr></table></td></tr>
<tr><td>/2</td><td>-</td></tr>
<tr><td>/3</td><td>-</td></tr>
<tr><td>/4</td><td>-</td></tr>
<tr><td>/5</td><td>-</td></tr>
<tr><td>/6</td><td>-</td></tr>
<tr><td>/7</td><td>-</td></tr>
<tr><td>/8</td><td>-</td></tr>
<tr><td>/9</td><td>-</td></tr>
<tr><td>/10</td><td>-</td></tr>
<tr><td>TB-3/1</td><td>V_{CC} MARG</td><td rowspan="2">Connections for margin-tests on V_{CC} and V_{BB} (refer to section 6)</td></tr>
<tr><td>/2</td><td>V_{BB} MARG</td></tr>
<tr><td>/3</td><td>+ 30 V</td><td></td></tr>
<tr><td>/4</td><td>GND</td><td>Ground for margin circuits</td></tr>
<tr><td>TB-6/1</td><td>+BAT</td><td>Battery positive terminal</td></tr>
<tr><td>/2</td><td></td><td>not used</td></tr>
<tr><td>/3</td><td></td><td>not used</td></tr>
<tr><td>/4</td><td>TEST</td><td></td></tr>
</table>



Power Supply Connector Panel (See also figure 3-5)

The main logic supply (V_{cc}) and logic ground are brought out on two separate terminals. A heavy gauge wire, suitable for carrying the high current of this supply (nominal 35 amperes), connects these terminals to the backplane of the enclosure. The cabling of the other supplies also terminates on the backplane, as shown in figure 3-4.

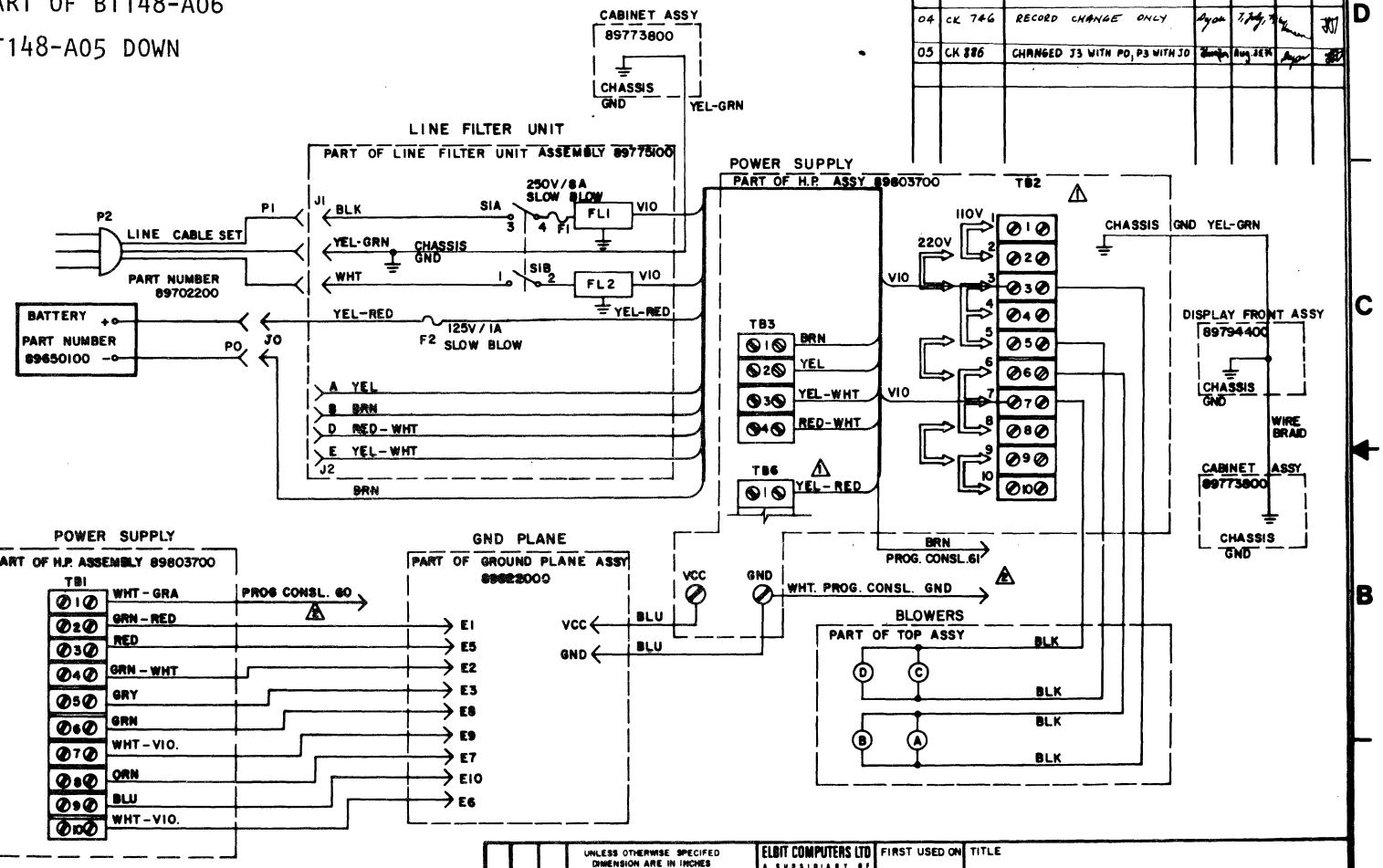
Power supply internal connections are made on terminal strips TB4 and TB5, mounted inside the power supply unit on the frame carrying the output filter and capacitors. Other components are shown on these drawings grouped according to the mounting positions within the power supply assembly. They are shown in their functional relation to the rest of the circuitry in circuit diagram 89657700 for the High Power and Control Unit (HP) and in circuit diagram 89640800 for the Low Power (LP) Card. They are described in the following pages.

For instructions and explanation of enclosure grounding, refer to the installation instructions in section 6 and to the maintenance aids in section 7 of this manual. Refer also to the Site Preparation Manual, publication number 60437000.

89633300 H

USED ON AB107-A04 to A12
AB108-A04 to A12
PART OF BT148-A06
BT148-A05 DOWN

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	01	CK493	RELEASED TO CLASS B		3.2.74		
	02	CK 608	REVISED		2 May 74		
	03	CK 723	FRONT DISPLAY ASSY WAS 89710200		22 May 74		
	04	CK 746	RECORD CHANGE ONLY		7 July 74		
	05	CK 886	CHANGED J3 WITH P0, P3 WITH J0		Aug 2 EEK		



⚠ 60, 61, AND GND ARE SOLDER POINTS ON THE PROGRAMMER'S CONSOLE PW ASSY 89649300.

⚠ REFER TO DWG NO. 89780800 FOR COMPLETE WIRING OF TB2, AND TB6.

WL 89670800
PL 89816700
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING
MATERIAL N/A
FINISH N/A

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

FIRST USED ON AB107-A

DWN	Naomi Peleg	3.2.74
CHKD		10.2.74
ENGR		10.2.74
MFG		
APPR		

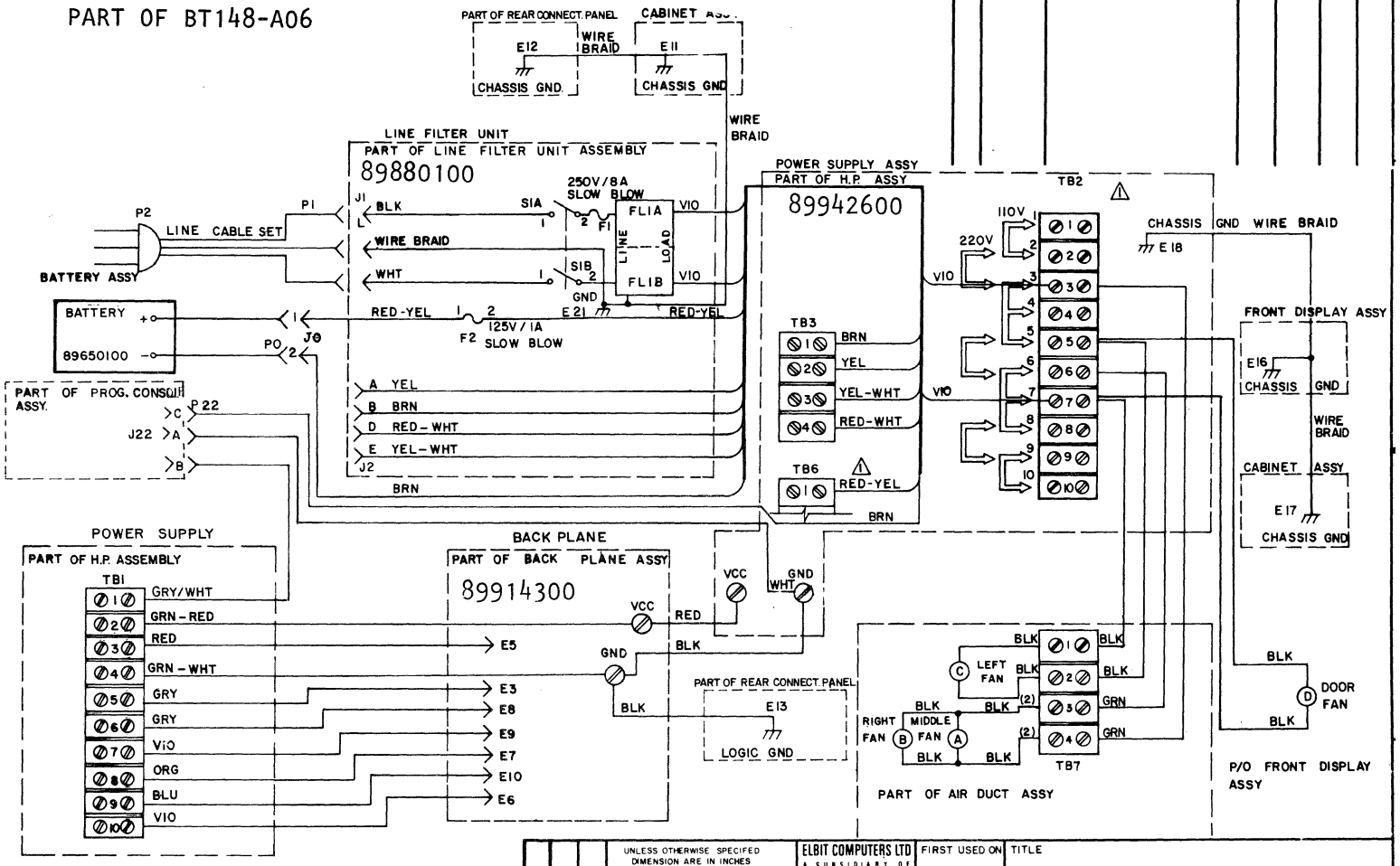
TITLE
POWER SUPPLY
INPUT-OUTPUT WIRING DIAGRAM

CODE IDENT C
DRAWING NO 89762200
SCALE
REF: POWER SUPPLY ASSY 89803700
SHEET 1 OF 1

5-429/5-430

USED ON AB107-A13 to A19
AB108-A13 to A19
PART OF BT148-A06

SHEET REVISION STATUS	REVISION RECORD						
	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	A	CK1066	REPLACES 89762200 FOR USE OF NEW PROGRAMMER CONSOLE ASSY 89881800				



⚠ REFER TO DWG NO. 89780800 FOR COMPLETE WIRING OF TB2, AND TB6.

WL 89942600
PL 89942600
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL N/A

FINISH N/A

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA CORPORATION

FIRST USED ON AB107/8-A

DWN	Naomi Pikovsky	3.2.74
CHKD	[illegible]	10.2.74
ENGR	G Horn	19.2.74
MFG	D. BARUCH	
APPR	Z. Nadiad	FEB. 19.74

TITLE
POWER SUPPLY
INPUT-OUTPUT WIRING DIAGRAM

CODE IDENT C

DRAWING NO 89942600

SCALE

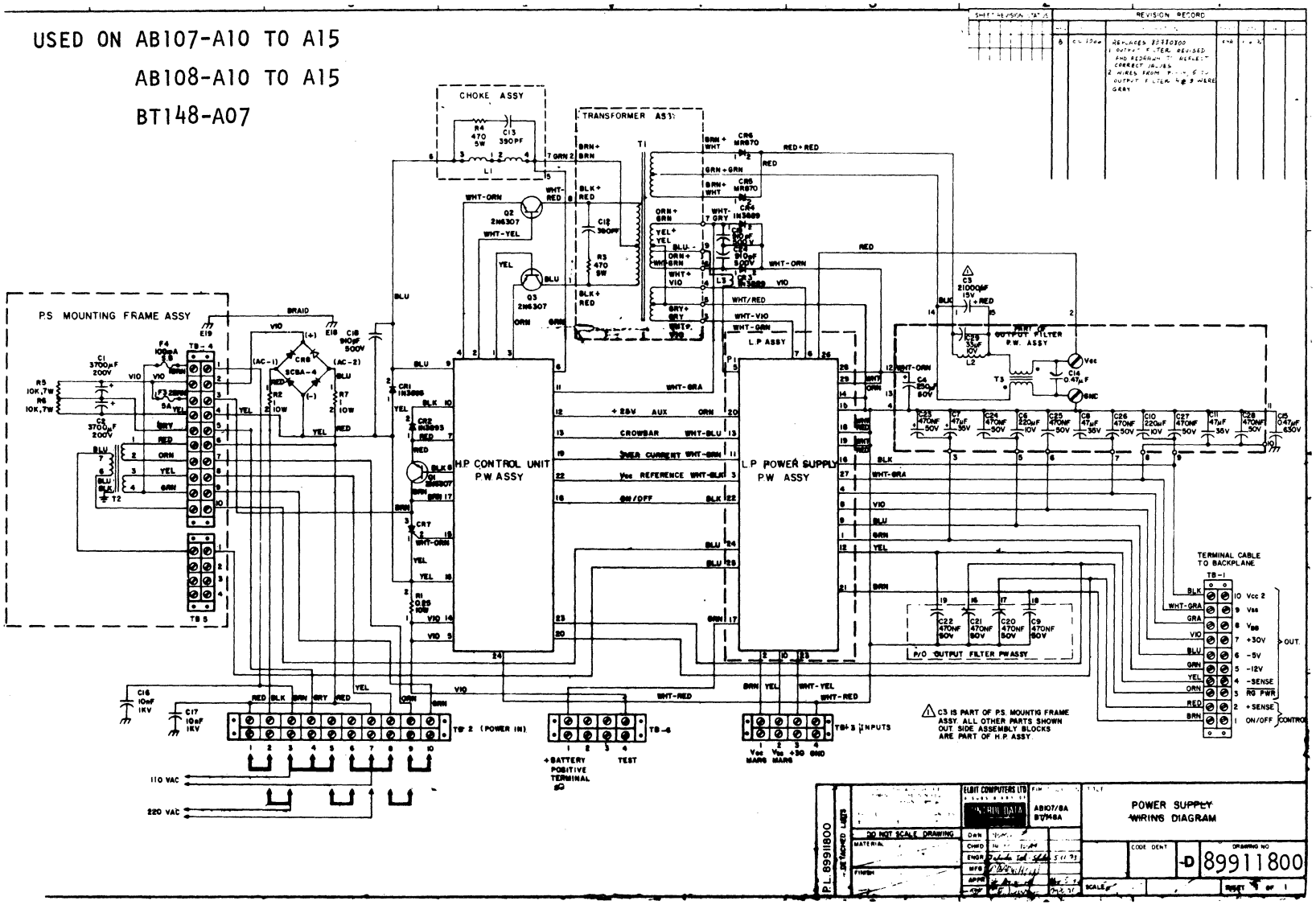
NHA: 8993[illegible]100

SHEET 1 OF 1

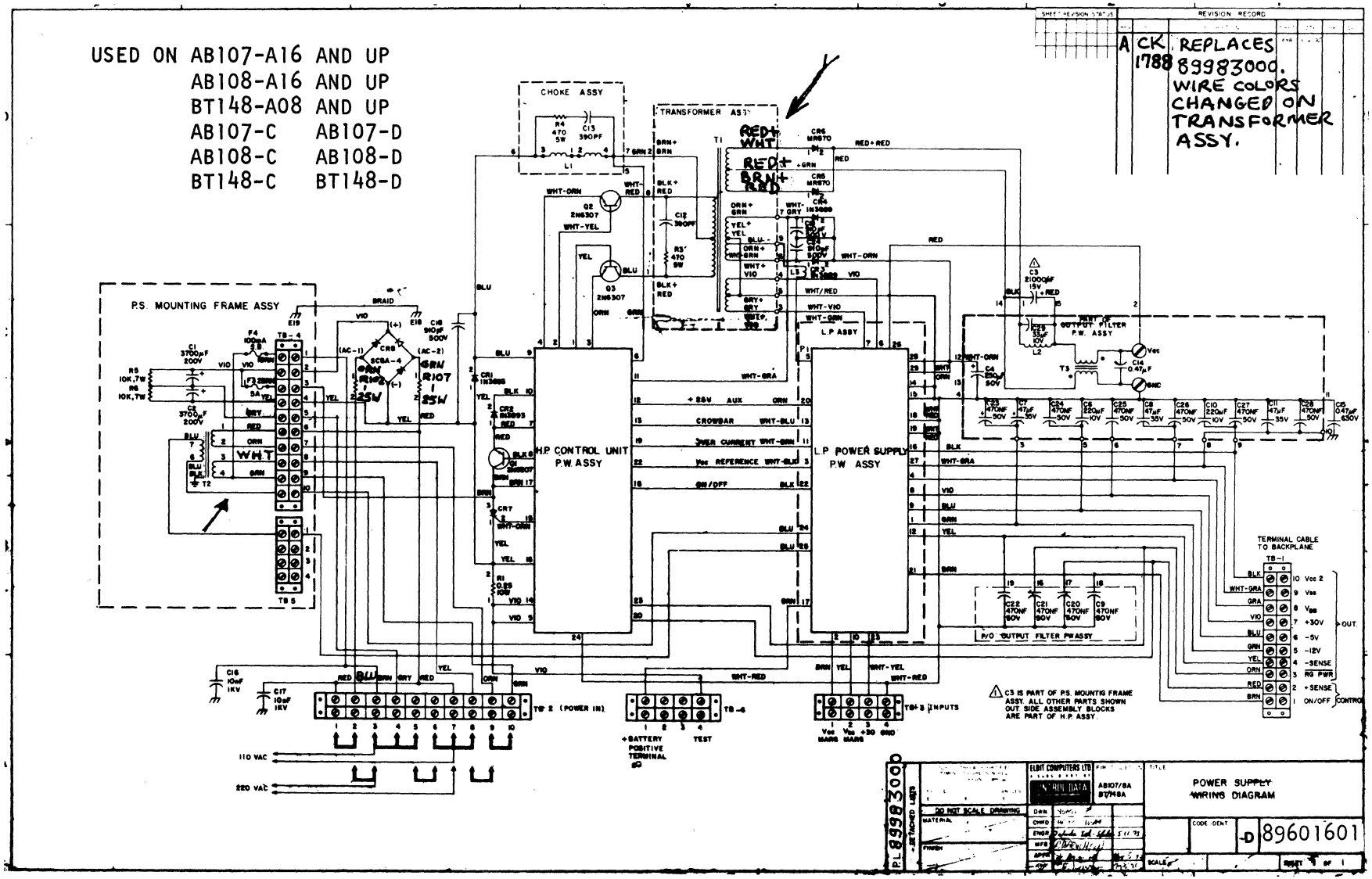
USED ON AB107-A10 TO A15

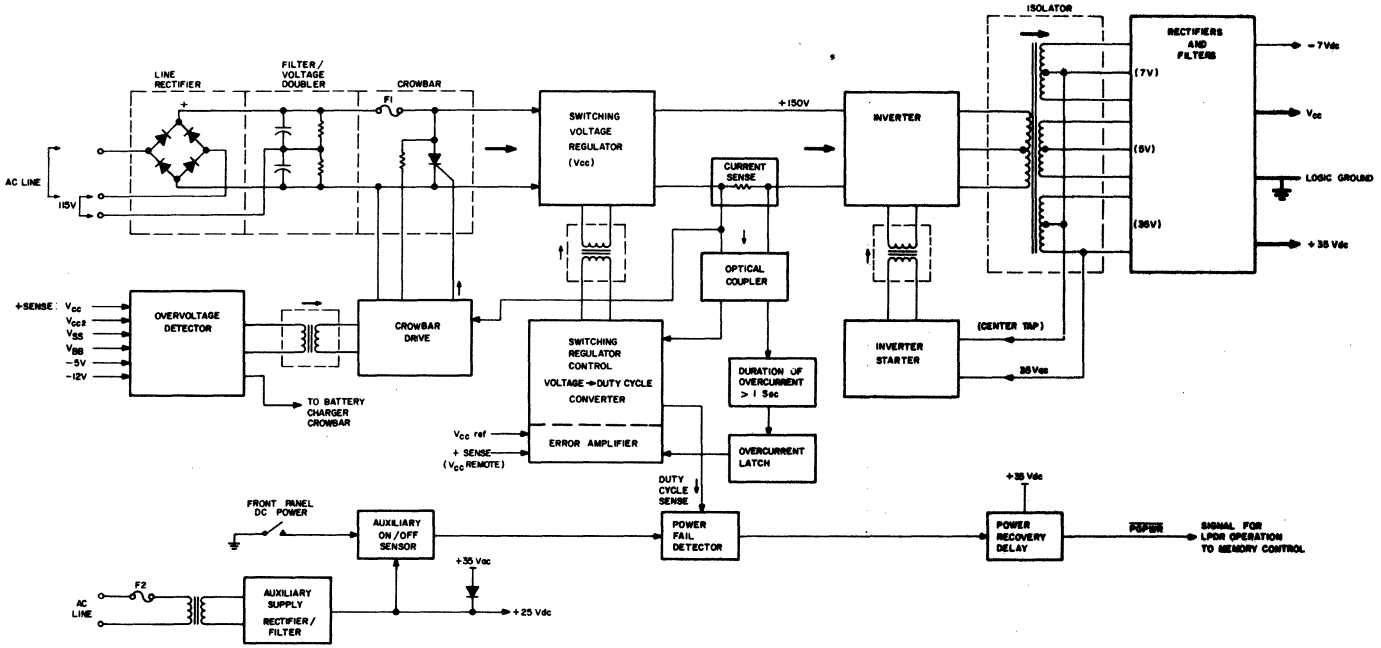
AB108-A10 TO A15

BT148-A07



USED ON AB107-A16 AND UP
AB108-A16 AND UP
BT148-A08 AND UP
AB107-C AB107-D
AB108-C AB108-D
BT148-C BT148-D





NOTES: 1. ARROWS SHOW DIRECTION OF POWER FLOW OR DIRECTION OF CONTROL. THE MAIN POWER FLOW IS INDICATED BY THICK LINES

2. ISOLATING TRANSFORMERS (1:1)

3. SINGLE LINE SIGNAL – FLOW REPRESENTATION IS USED IN THIS DIAGRAM, EXCEPT FOR THE CIRCUITS AT LINE VOLTAGE

4. SHORTING JUMPER
   115: SHORT FOR 115V OPERATION

POWER SUPPLY DETAILED BLOCK DIAGRAM

POWER SUPPLY UNIT (cont'd)

HIGH POWER (HP) AND CONTROL ASSEMBLY (Drawing number 89657700)

WARNING

The power supply does not use a main isolating line-transformer at its input; its circuits between the ac line input and the isolating networks are therefore at line voltage. Do not handle the power supply unit while the computer line cord is connected to the ac supply.

Function

The HP assembly is part of the power supply assembly. It carries the circuits in the main power path as well as protection and control circuits.

The circuits in the main power path are:

- main line rectifier and filter
- main fuse (F1) and crowbar
- switching regulator for V_{cc} with its control circuit and current limit detector
- inverter (chopper) and main isolating transformer (T1)
- rectifiers and output filters

The protection and control circuits are:

- inverter start circuit (associated with the inverter-chopper in the main power path)
- switching control circuit, associated with the V_{cc} switching regulator in the main power path
- current limit, overcurrent latch and crowbar driver
- power fail detector and recovery relay

These circuits are described in the following paragraphs; the block diagram on the next page may be referred to as an aid in understanding the interrelation of the circuits.

POWER SUPPLY UNIT (continued)

HIGH POWER (HP) AND CONTROL ASSEMBLY (drawing 89657700, continued)

Main Line Rectifier and Filter

The ac line voltage from the Input Circuit is applied to the rectifier bridge CR8. When working from 220V line input, the capacitors associated with the rectifier act as a filter, with the resistors aiding to divide the dc voltage across them evenly. When working from 110V line input, the line voltage is also applied to the junction between the two capacitors (refer to the wiring diagrams) which now act as a voltage-doubler and filter combined. As a result of this configuration, a dc voltage of about 350V is generated at the output of the circuit with either 110V or 220V line input.

Main Fuse and Crowbar

The power supply unit is protected by the main fuse F1 in the high voltage dc line at the main rectifier and filter output. It is blown when the SCR-type crowbar CR7 is gated-on by the Crowbar Drive circuit (see below).

Switching Regulator For V_{cc}

The main logic voltage V_{cc} is regulated in the switching regulator, consisting of main switching transistor Q1, filter inductor L1, catching diode CR1. None are mounted on the HP board assembly. Refer to section 4 for a description of the principles of operation of switching regulators. The Q1 emitter-base feedback path through two windings of pulse transformer T3 sustains oscillations in the circuit. The third winding of T3 is driven from the regulator control circuit output, which both initiates and controls the frequency of the switching.

The V_{cc} Regulator Control Circuit

Output circuit Q3,Q4,Q5 provides a drive pulse to pulse transformer T3 when a negative-going pulse appears on the base of transistor Q4. It prevents oscillations by shorting the T3 winding when transistors Q5,Q6 saturate (positive pulse at their base). Note that transistor Q3 extends the voltage

HIGH POWER (HP) AND CONTROL ASSEMBLY (drawing 89657700, cont'd.)

range of the output circuit. Transistors Q7, Q8, Q9, drive the output circuit, the point of control for the switching regulator being at the base input to Q9.

This point is driven normally by controlled pulses from comparator U4 through buffer Q13 and oscillator Q10, Q11. This circuit compares the V_{cc} voltage at the enclosure backplane (+SENSE) with the V_{cc} reference from the reference generator. The duty cycle of oscillations and therefore that of the switching regulator depends on the difference between these signal levels, thus closing the regulator feedback loop. Transistor Q14 and associated components control the rise and fall times at the comparator output.

The control signal at the input to the switching regulator driver (Q9 base line) is subject to control by the overcurrent circuits actuated from the overcurrent detectors of the various supplies, except that in the main power path (see below).

Note that transformer T3 provides voltage isolation between the regulator (at high voltage) and its control circuit.

Resistor R1 (mounted outside the HP board) in the main current path is connected to the current limit circuit. It is also connected to the crowbar to blow the fuse in case the current limit fails.

POWER SUPPLY UNIT (cont'd.)

HIGH POWER (HP) AND CONTROL ASSEMBLY (drawing 89657700, cont'd.)

Inverter and Main Isolating Transformer

The dc power from the V_{cc} regulator is inverted to 20 KHz ac in the chopper circuit of transistors Q2, Q3 (mounted off the HP board). The primary of transformer T1 is an essential part of the chopper; it also provides the isolation from the line voltage in the main power path. One pair of windings of transformer T3 is used for current-feedback in the chopper circuit, the other pair is for driving it.

The chopper is not self-starting. Phase shift oscillator Q15 is provided to drive it through output stage Q16, Q17 and the driver coils of transformer T3. This circuit is used as a starting oscillator for the chopper on initial switching on and during start-up after power failure. Once the chopper gives an output voltage the circuit provides a feedback path through transformer T2, resistor R55 and transformer T3. Note that the change in function of the circuit comes about because of the low impedance of R55 and the path through T2 as compared with the impedance of the resistor chain (R57 through R60) in the phase shift circuit.

The main isolating transformer is T1. It has three center-tapped output windings. One winding feeds the rectifiers and filters for the main logic supply V_{cc}. Another winding provides 35 vac to the LP board and also feeds the rectifiers for the internal +35 vdc supply. The third one (shown in the wiring diagrams) provides 7 vac to the LP board.

Note that the logic ground is not defined at the center tap of the winding supplying the main logic voltage V_{cc}, but is defined at the output of the filter for this supply.

HIGH POWER (HP) AND CONTROL ASSEMBLY (drawing 89657700, cont'd.)

Rectifiers and Output Filters

The main logic supply voltage (V_{cc}) is derived from one winding of the isolating transformer (T1) through full wave rectifier CR5, CR6 and its output filter (C3, C14, L2, T3; all mounted on the filter chassis off the HP board). Note that a comparatively simple filter network provides a dc supply with very low ripple content as the frequency of the alternating supply is high (20KHz) compared to line frequency.

Current Limit, Overcurrent Latch and Crowbar Driver Circuits

The power supply is protected against overcurrent by overcurrent detectors in a number of circuits. These detectors act through the current limit circuit, and the overcurrent latch, or directly on the crowbar driver circuit.

When the crowbar driver circuit is actuated, it blows the main fuse (F1); when the current limit circuit is activated it inhibits the V_{cc} regulator control circuit and activates the power fail detector and alarm.

The various current limit modes are as follows:

- if the current limit is exceeded in any one of the protected supplies on the LP board, a signal appears on the overcurrent bus which is an input to the current latch circuit;
- if the current limit is exceeded in the main power path, the current limit resistor associated with the V_{cc} regulator (R1, mounted off the HP board) actuates the Crowbar Driver circuit;
- if the current limit is exceeded in the main power path, the current limit resistor (R1) in the V_{cc} switching regulator also actuates the overcurrent circuit through optical coupler U1.

POWER SUPPLY UNIT (cont'd.)

HIGH POWER (HP) AND CONTROL ASSEMBLY (drawing 89657700, cont'd.)

In addition to the overcurrent protection, the power supply is protected against the voltage exceeding the preset maximum value on any one of the regulated supplies on the LP assembly. The overvoltage detectors situated there are ORed together and actuate the crowbar circuit through transformer T1.

The crowbar driver consists of three firing circuits for the crowbar SCR (UR7). When the crowbar is fired it blows the main power supply fuse (F1). The three circuits are described here.

One circuit consists of transistors Q1, Q2 connected in a Silicon-Controlled-Rectifier (SCR) configuration. When the voltage across the main power path current limit resistor (R1, off the HP board) exceeds the base-emitter "on" voltage of transistor Q1, the compound connected transistors short the crowbar SCR (CR7) anode to its gate through resistor R7, thus firing it.

As a further precaution against a short circuit, the voltage across the main power path current limit resistor (R1, off the HP board) is applied to the crowbar gating circuit, through diodes CR2, CR3, thus firing it almost directly. This precaution is included in view of the high currents in the main power circuits. This circuit comes into operation only if other parts of the drive fail.

The overcurrent circuit receives its input from the current limit resistor in the main power path (R1, mounted off the HP board) through optical coupler U1.

The signal from the optical coupler acts through amplifier Q18, Q19, Q20; should the instantaneous current exceed the preset value, Q18 applies a

HIGH POWER (HP) AND CONTROL ASSEMBLY (drawing 89657700, cont'd.)

positive voltage to the V_{cc} regulator control circuit and cuts the pulse controlling the regulator.

The overcurrent latch consists of transistors Q22, Q23 connected as a Silicon Controlled Rectifier (SCR) and associated components. A signal from the overcurrent bus from the LP card fires this and so stops the pulse train in the V_{cc} regulator control circuit. As an additional precaution this SCR may be fired through comparator U5. The comparator is actuated when the overcurrent signal from transistor Q19 has been present for about one second (time-constant C33, C32, R67).

The latch is reset by the signal from the POWER on/off switch on the Programmer's Console acting through the LP card.

The power fail detector (U2, U3), when activated, generates the power fail signal ($\overline{\text{RGPWR}}$). This is transmitted to the Memory Control board and initiates the Low Power Data Retention (LPDR) mode of operation.

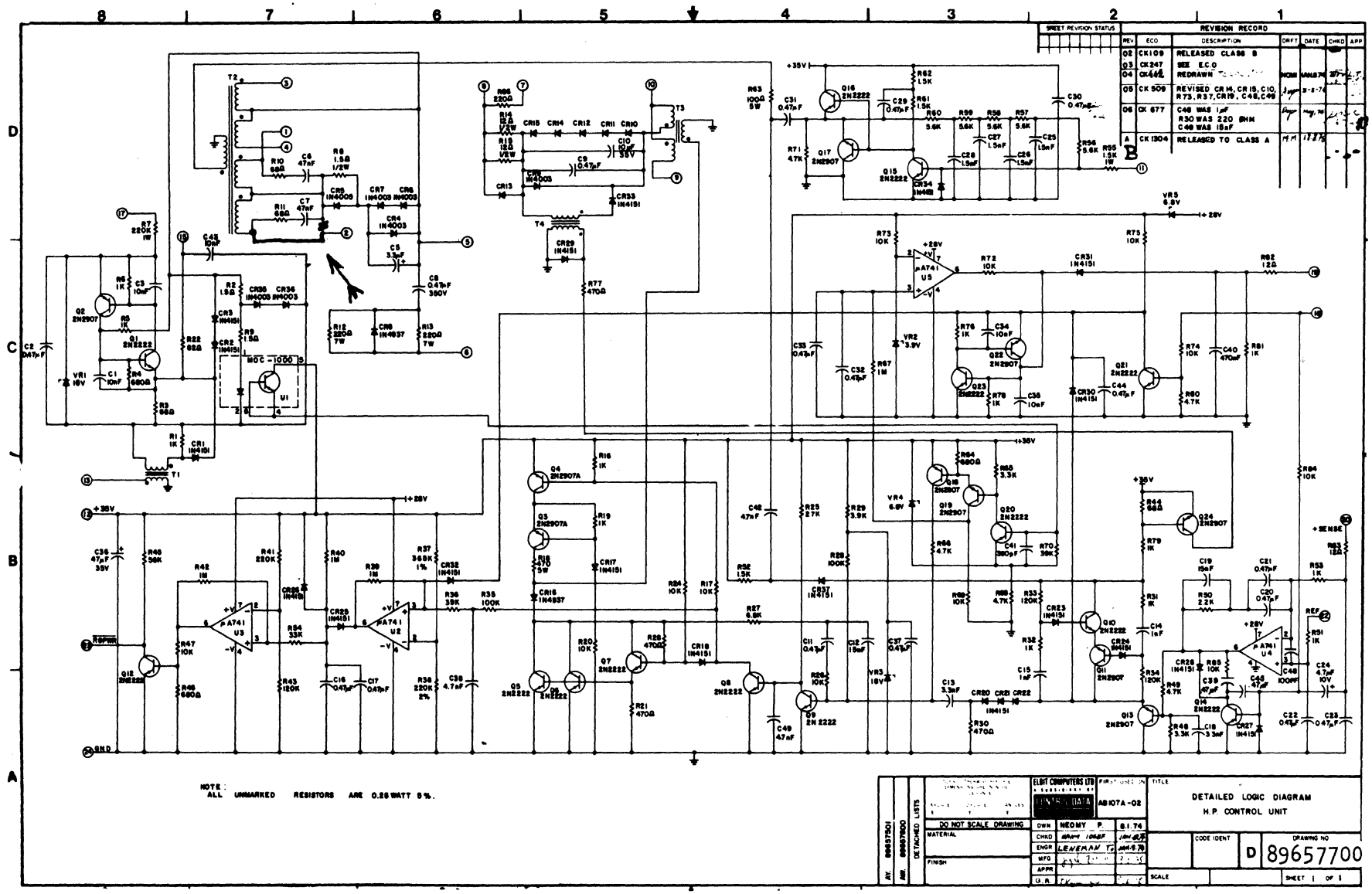
This circuit is activated in the following cases:

- when the V_{cc} regulator control circuit is stopped
- when the overcurrent latch circuit has been activated.

HIGH POWER (HP) AND CONTROL ASSEMBLY (drawing 89657700, cont'd.)

Comparators U2, U3 are connected as Schmitt-triggers and generate the output signal as soon as activated. To avoid hunting, capacitors C16, C17 act to delay the resetting of the circuit and the removal of the power fail condition.

This circuit, as the rest of the power supply protection circuits, receives its supply from the +35 vdc internal supply bus. Note that this bus is also connected to the +25 vdc auxiliary supply. Thus if the power supply as a whole fails, these circuits remain active, provided the main line voltage has not been removed.



REVISION RECORD: REVISION B, ECO CK1475, ZONE D-7: CONNECTION R11/CIRCLE 2 REPLACES C7/CR5/CIRCLE 2

POWER SUPPLY UNIT (cont'd.)

LOW POWER CIRCUIT ASSEMBLY (drawing number 89640800)

Function

The Low Power circuit assembly is part of the power supply assembly and carries the following circuits:

- regulated voltage supplies and associated over-voltage detectors (except V_{CC} supply)
- reference voltage generator
- current limit for +30V supply
- battery charging circuit with battery fuse crowbar
- general current limit crowbar driver
- auxiliary on/off sensor
- auxiliary internal supplies: +25V, -7V

These circuits are described in the following paragraphs. The block diagram on the next page may be referred to as an aid in understanding the interrelation of the circuits.

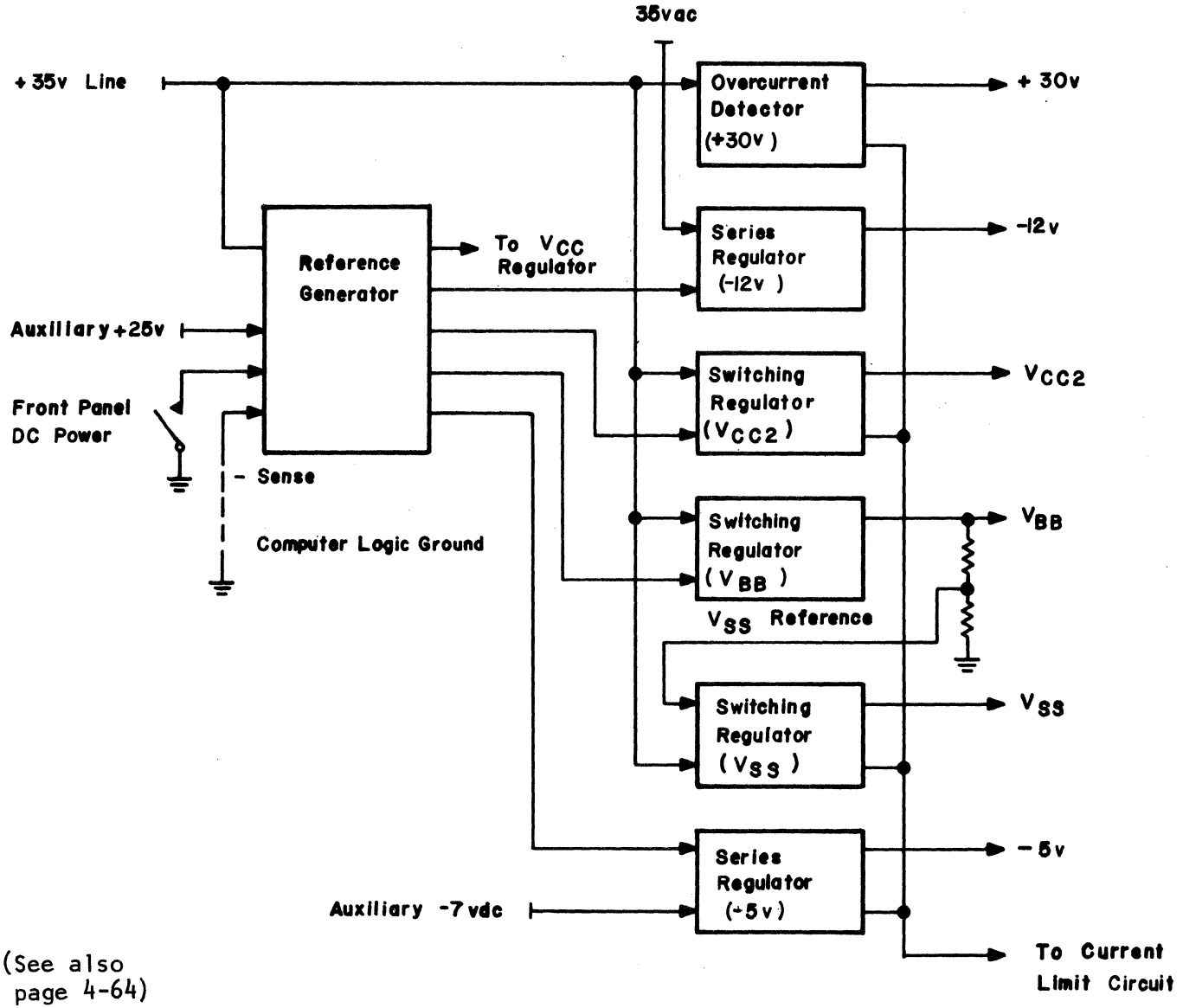
The +30V unregulated supply is derived directly from the +35 vdc internal preregulated supply through resistors (R62, R63) of the current limit circuit. The current limit detector is a conventional circuit: when the current taken from the supply causes a voltage drop across the resistors equal or greater than the turn-on voltage of the transistor (Q29), the transistor saturates and applies the +35V bus to the over-current bus at terminal 11, through resistor R67.

POWER SUPPLY UNIT (cont'd.)

LOW POWER CIRCUIT ASSEMBLY (drawing number 89640800, cont'd.)

The -12V regulated supply is derived from a half-wave rectifier on the 35 vac winding of transformer T1. It is regulated by a conventional series regulator circuit working between this voltage and the +35V bus. The two inputs of the regulator differential amplifier are remote ground (-SENSE) and the general voltage reference (VREF) from the reference generator. The output voltage of the regulator can be adjusted by means of potentiometer RV4 in the reference voltage divider chain. The potentiometer is accessible through the top cover of the power supply unit (refer to Figure 6-4). The supply is connected to the over-voltage detector through transistor Q23 (see below); its current is limited by resistor R58 in the emitter circuit of the series regulating transistor (Q28).

The -5V regulated supply is derived from the full wave rectifier (diodes CR12, CR13) on the 7 vac winding of transformer T1. It is regulated by a conventional series regulator circuit working between this voltage and the +35V bus. The two inputs of the regulator differential amplifier are remote ground (-SENSE) and the general voltage reference (VREF) from the reference generator. The output voltage of the regulator can be adjusted by means of potentiometer RV5 in the reference voltage divider chain. The potentiometer is accessible through the top cover of the power supply unit (refer to Figure 6-4). The supply is connected to the overvoltage detector through transistor Q22 (see below). The current in this supply is limited through the general overcurrent bus; the conventional detector (R28, Q19) saturates transistor Q29 when the supply current exceeds a preset value; Q29 in its turn applies the +35V bus to the overcurrent bus (terminal 11), through resistor R67. Note that Q29 and the Q16, Q17 pair are common to this circuit and the +30V supply.



(See also page 4-64)

Power Supply Regulator and Control Circuits: Block Diagram

POWER SUPPLY UNIT (cont'd.)

LOW POWER CIRCUIT ASSEMBLY (drawing 89640800, cont'd.)

The V_{BB} regulated supply is derived from the +35V internal supply. It is regulated by a conventional series regulator using transistor Q30 as the series element and the differential amplifier in the reference voltage generator package (U3) as the comparator. The two inputs of this comparator are the general voltage reference (VREF) through R79 and the tap on the voltage divider chain on the output. The output voltage of the regulator can be adjusted by means of potentiometer RV3 in the output voltage divider chain. The potentiometer is accessible through the top cover of the power supply unit (refer to Figure 6-4). Note that this adjustment affects the value of V_{SS} directly - see V_{SS} supply below. The supply is connected to the overvoltage detector through diode CR34; its current is limited by the conventional circuit of Q31, R77, which cuts off the series regulator on occurrence of overcurrent. The regulator output voltage (and therefore V_{SS}) can be changed by loading the output voltage divider chain and through it one of the comparator inputs through the V_{BB} MARGIN terminal (refer to Section 6 for Margin Tests).

The V_{SS} regulated supply is derived from the +35V internal supply, and is regulated by a switching regulator (see Section 4 for the principles of operation of switching regulators). The switching element in this circuit is transistor Q44 with Q9 as predriver and Q8, Q33 as parallel drivers. The main output filter capacitors are located on the filter board in the power supply assembly . See the relevant power supply wiring diagram.

The regulator is driven at about 22 KHz by emitter-coupled oscillator Q11, Q13. The duty-cycle of this oscillator (and therefore the proportional regulation of the circuit) is determined by the ratio of emitter currents of the two transistors. This in turn is controlled by the differential amplifier Q10, Q12 sharing the current source Q39, Q40. One input of the differential amplifier is the V_{SS} reference voltage derived from the V_{BB} supply through driver transistor Q34. To avoid sudden changes in the inductor current (and therefore large voltage spikes on the inductor) a rise-time limiter integrator (R101, C47 and Q45) is included in the reference line of the regulator.

LOW POWER CIRCUIT ASSEMBLY (drawing 89640800, cont'd.)

Overcurrent in this circuit is detected by the voltage developed on R98 acting as the gating voltage on transistors Q14, Q15 connected as a Silicon Controlled Rectifier (SCR). This is driven by the oscillator output and is therefore reset on every cycle of the switching inverter. When an excess current flows through the switching transistor, +35V is connected to the overcurrent bus through transistor Q15. This supply is connected to the overvoltage detector and crowbar circuit through diode CR33.

The V_{cc2} regulated supply has a similar circuit to that of the V_{SS} supply. It receives its reference voltage through a reference voltage divider chain and its output voltage can be adjusted by potentiometer RV2. Access to RV2 is obtained through the power supply assembly cover (refer to Figure 6-4).

The reference generator utilizes the reference portion of the voltage regulator package U3 (see the circuit diagram below) to supply the reference voltage to the regulated power supplies. Its supply is referred to the remote enclosure ground (-SENSE); it is switched through from either the auxiliary supply or battery by transistor Q32, under control of the dc POWER on/off switch on the Programmer's Console.

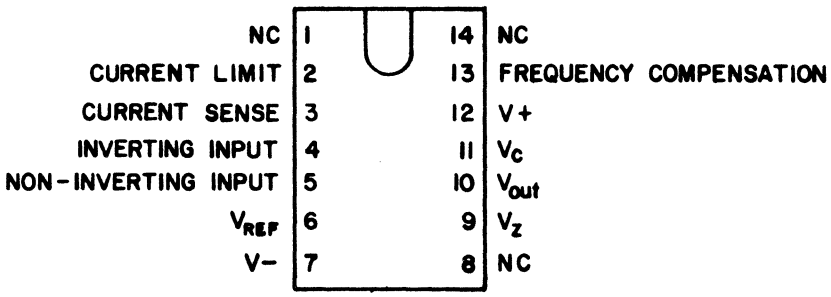
The overvoltage detector and crowbar input circuit utilize the comparator in the voltage regulator U1 to turn on the transistors Q24, Q25 connected in a Silicon-Controlled-Rectifier (SCR) configuration when an over-voltage occurs on any one of the regulated supplies (-12V, -5V, V_{cc2}, V_{SS}, V_{BB}, V_{cc}). The positive supplies are ORed to the inverting input through common base level shifters Q22, Q23. The comparator thus changes state when the absolute voltage on any one of the supplies increases over the value preset by the voltage divider on each supply. The inputs to the comparator are biased from the reference source in U1.

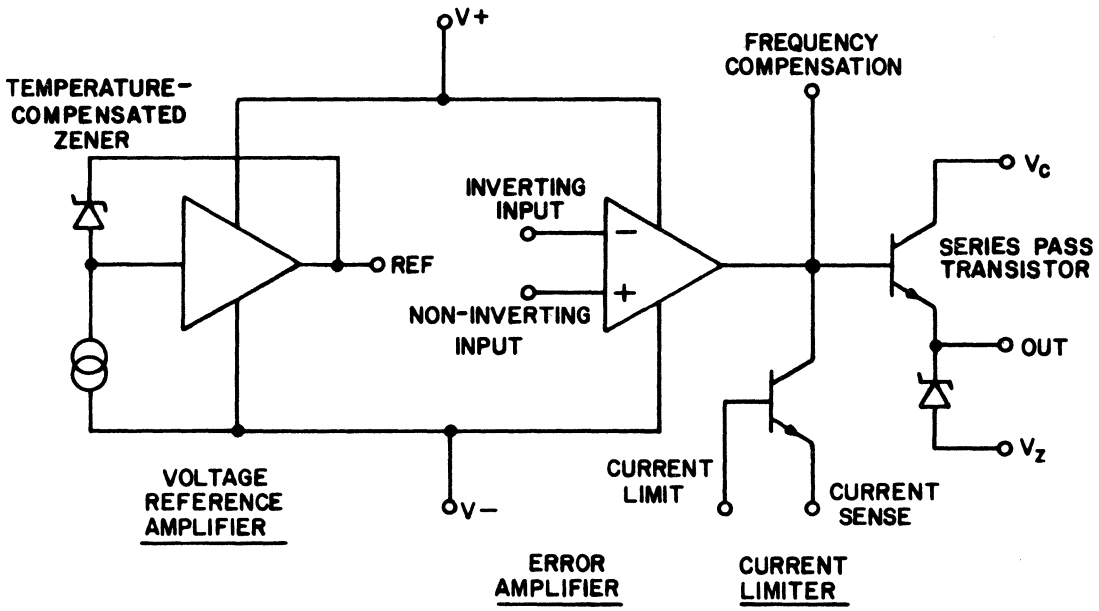
POWER SUPPLY UNIT (cont'd.)

LOW POWER CIRCUIT ASSEMBLY (drawing 89640800, cont'd.)

VOLTAGE REGULATOR (μA723C)

CIRCUIT AND TERMINAL ASSIGNMENTS





LOW POWER CIRCUIT ASSEMBLY (drawing 89640800, cont'd.)

Thus when U1 turns on transistors Q24, Q25, they apply the switched battery or auxiliary supply to the crowbar bus. This signal turns on the battery crowbar (SCR Q46) and actuates the crowbar circuit on the HP assembly (drawing 89657700), which in turn blows the main supply fuse (F1), and the battery fuse (F2).

The following text relies on HP assembly drawing 89657700 and on the relevant power supply wiring diagram.

The on/off dc POWER switch on the Programmer's Console controls the supply to the crowbar input circuit (just as it controls the supply to the reference generator). When it is on, transistor Q32 switches on the battery or the auxiliary supply through to the supply line of the crowbar circuit.

The auxiliary on/off sensor (U2) is a voltage regulator package connected as a Schmitt-trigger. The on/off dc POWER switch of the Programmer's Console controls its output frequency which forms the input signal of the power fail detector on the HP board.

Two auxiliary supplies are generated on the LP board. The -7V supply (feeding the -5V regulated supply) is generated by full-wave rectifier CR12, CR13 from the 7 vac output winding of the main transformer T1.

The +25V supply is generated by the rectifier bridge (CR21, CR22, CR23, CR24) from the separate auxiliary mains transformer T2. This supply feeds the auxiliary supply line while the main power circuit and isolating power transformer T1 do not reach their normal voltage. This may occur when the equipment is first switched on, or when it recovers from power failure.

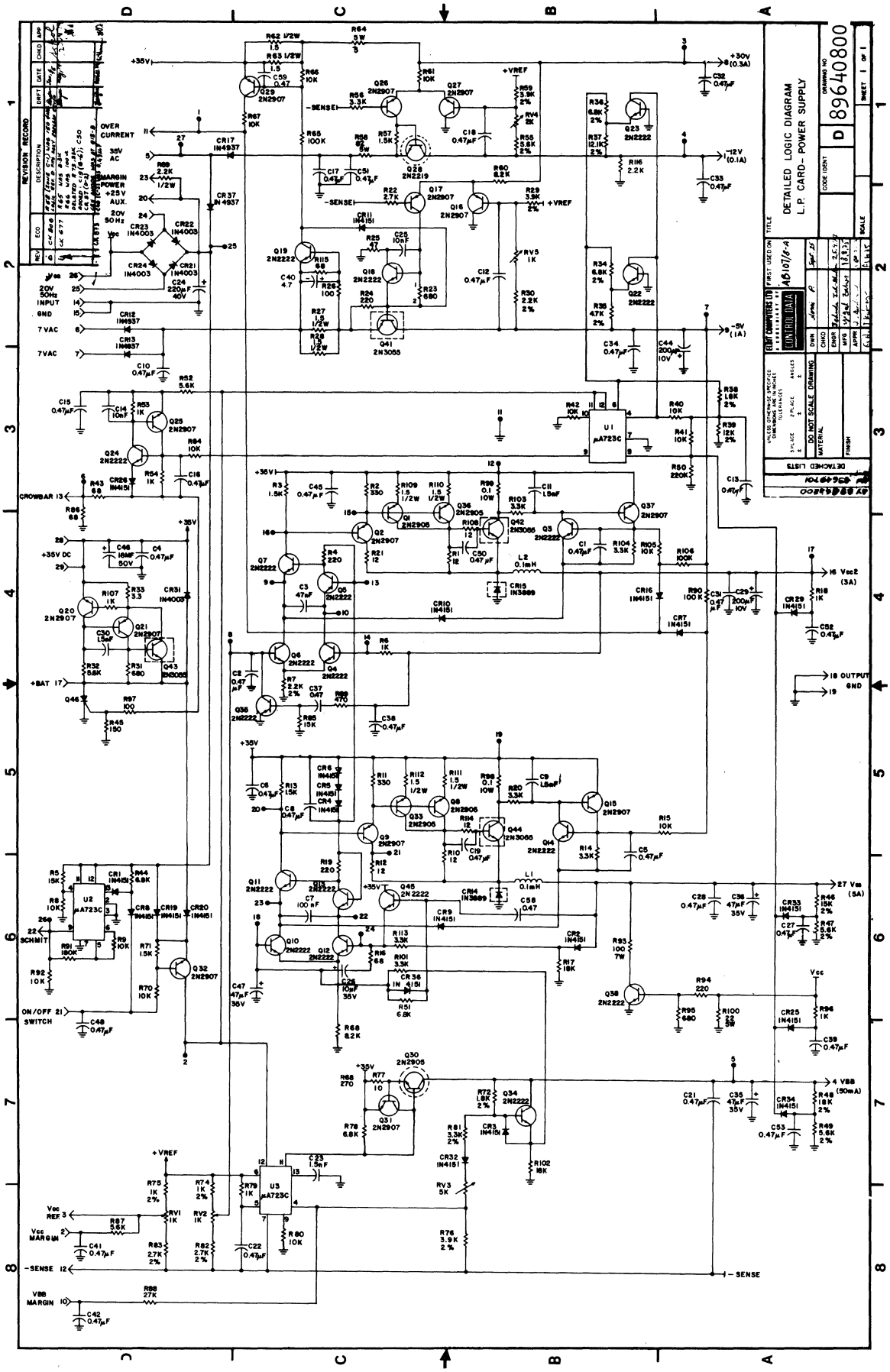
POWER SUPPLY UNIT (cont'd.)

LOW POWER CIRCUIT ASSEMBLY (drawing 89640800 cont'd.)

With the main power circuit supplying full voltage, the 35 vac winding on the main transformer (T1) takes control of the auxiliary line through half-wave rectifier CR30.

The battery charging circuit charges the Memory Hold Battery (equipment GD 611-A) from the +35V internal supply. When this supply is on, transistors Q20, Q21 form a current source which feeds the battery through current amplifier Q43 (terminal 17).

The battery supplies power to the +35V bus and through it to the equipment through isolating diode CR31 when the +35V supply fails (power fail condition: Low Power Data Retention (LPDR) mode of operation).


DETAILED LOGIC DIAGRAM
L.P. CARD - POWER SUPPLY
DRAWING NO D 89640800
SHEET 1 OF 1
SCALE
CODE IDENT
FIRST USED ON A6107/6-A
CONTROL DATA
DO NOT SCALE DRAWING
MATERIAL
FINISH
DETACHED LISTS
REVISION RECORD
DESCRIPTION
ECO
REV
+35V
-35V
+VREF
-SENSE
+30V (0.3A)
-12V (0.1A)
-5V (1A)
+15 Vcc2 (3A)
+27 Vm (5A)
+4 VBB (50mA)
OVER CURRENT
MARGIN POWER +25V AUX.
20V 50Hz INPUT
GND
7 VAC
CROWBAR
+35V DC
+BAT
ON/OFF SWITCH
SCHMIT
OUTPUT GND
Vcc REF
Vcc MARGIN
VBB MARGIN
U1 µA723C
U2 µA723C
U3 µA723C
Q1 2N2906
Q2 2N2907
Q3 2N2222
Q4 2N2222
Q5 2N2222
Q6 2N2222
Q7 2N2222
Q8 2N2906
Q9 2N2907
Q10 2N2222
Q11 2N2222
Q12 2N2222
Q13 2N2222
Q14 2N2222
Q15 2N2907
Q16 2N2907
Q17 2N2907
Q18 2N2222
Q19 2N2222
Q20 2N2907
Q21 2N2907
Q22 2N2222
Q23 2N2222
Q24 2N2222
Q25 2N2907
Q26 2N2907
Q27 2N2907
Q28 2N2219
Q29 2N2907
Q30 2N2905
Q31 2N2907
Q32 2N2907
Q33 2N2906
Q34 2N2222
Q35 2N2222
Q36 2N2905
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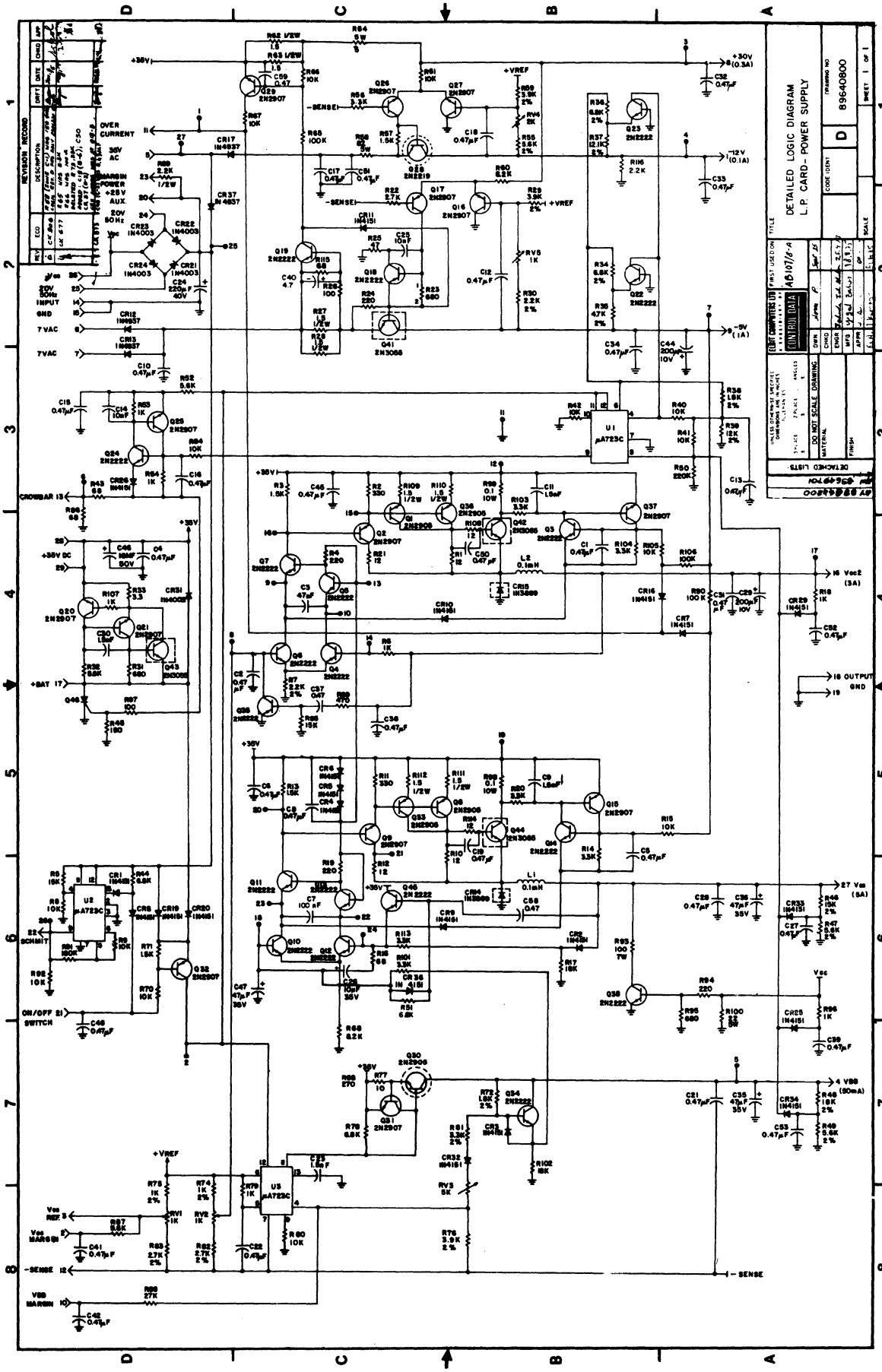
Q43 2N3055
Q44 2N3055
Q45 2N2222
Q46 2N2222


DETAILED LOGIC DIAGRAM
L.P. CARD - POWER SUPPLY
89640800
+30V (0.3A)
-12V (0.1A)
-9V (1A)
+16 Vcc2 (5A)
+27 Vm (5A)
+8 VBB (90mA)
-SENSE
+VREF
OVER CURRENT
CROWBAR
ON/OFF SWITCH
SCHMITT
U1 μA723C
U2 μA723C
U3 μA723C

SECTION 6

MAINTENANCE

MAINTENANCE

This section applies to the equipment listed in Section 1 of this manual.

TOOLS AND SPECIAL EQUIPMENT

The following is a list of maintenance tools for the equipment.

Part Number	Part Description	Quantity
12210275	Tweezer Fine Point	1
12210314	Iron Soldering 15W Miniature	1
12210315	Tip Soldering Iron .046 In. Spade	2
12210433	Stripper Wire 20-20 Ga	1
12210437	Solder 60/40 24 Ga. (.022 In)	1
12210849	Tool Wire Removal 20-26 Gauge	1
12210436	Desoldering Tool	1
89688700	Board Extender	2
▮ 89980600	Board Extractor	1
	Oscilloscope (Tektronix 453 or Equivalent)	1
	Voltmeter (20,000 ohm/V min)	1
	Load Resistor 60 ohm, 5%, 10 watt	2
	Isopropyl Alcohol	

The publications listed below are applicable to the equipment.

	Publication Number
Mini Computer Site Preparation Manual	60437000
1784 Reference Manual	89633400
1784 I/O Specification Manual	89673100
1700 Computer System Codes Manual	60163500
Teletypewriter C.E. Manual	60163700
System Maintenance Monitor (SMM 17)	60182000

Refer also to Preface of this Manual.

CALIBRATE POWER SUPPLY LEVELS

This calibration applies to both main and expansion enclosures.

Check/Condition	Action
1. System power on, system not operational.	1. Open the enclosure rear cover. 2. Connect the voltmeter (multimeter) to the test point (TP) for the main logic supply (V_{cc}); location of the test point is shown in Figure 6-1.
Check the value of the V_{cc} supply (see Table 6-1). Correct? No →	a. Adjust the V_{cc} supply voltage by screwdriver control located as shown in Figure 6-4. b. Repeat check.
Yes ↓ Go to next step	3. Repeat 2 with the computer running under test. 4. Repeat 2 and 3 for the following supplies: -12V, -5V, +30V (see Table 6-1).
2. System ac power switch OFF, front panel dc POWER switch ON, memory hold battery installed.	5. Repeat 2 above for the following supplies: V_{cc2}, V_{SS}, V_{BB} (see Table 6-1).

TABLE 6-1 - COMPUTER DC SUPPLIES

Supply No.	Designation	Nominal voltage volts	Nominal Current	Remarks
1.	V_{cc}	+ 5.0	35A	R
2.	V_{cc2}	+ 5.3	3A	R,M
3.	V_{SS}	+16.7	5A	AB107/BA201-B, R, M
	V_{SS}	+19.7	5A	AB108/BA201-A, R, M
4.	V_{BB}	V_{SS}+ 3.5	40mA	R, M
5.	-12V	-12.0	100mA	R,
6.	- 5V	- 5.0	1A	R
7.	+30V	+30.0	300mA	unregulated, M
8.	battery charger		200mA	current regulated
Internal supplies				
9.	+35V	+35		preregulated
10.	auxiliary no1			unregulated
11.	auxiliary no2	- 7		unregulated internal supply

NOTES: 1. R: regulated supply M: supply to the memory only

2. The tolerance on all regulated voltages is less than $\pm$ 1/2 %. The maximum permissible ripple is 2% of each regulated voltage.
3. All power supply levels are generated in the power supply unit (terminal configuration shown in Figure 6-5).
4. All power supply levels are to be measured on the computer backplane at the test points (TP) shown in Figure 6-1.
5. Memory supply voltage (V_{SS}) is varied by V_{BB} adjustment.

CHECK BATTERY (Optional power back-up source, equipment GD611-A)

Check/Condition	Action
1. System power off.	1. Make sure the battery is fully charged. Note: the battery is fully charged if it is charged 32 hours. If the battery is not fully discharged a shorter period of charging may be sufficient. Disconnect the battery from its terminals in the enclosure; refer to Figure 3-7. Connect the voltmeter (multimeter) across the battery. WARNING Do not short battery.
Check the battery voltage ($\geq$ 24.2V).	
Correct? No ⟶	Change battery (refer to instructions in Section 3).
Yes ↓ Go to next step	
	2. Connect two 60 ohm 5% 10 watt resistors across the battery in parallel. Connect the voltmeter (multimeter) across the resistors.
Check the battery voltage ($\geq$ 24.2V).	
Correct? No ⟶	Change battery (refer to instructions in Section 3).
Yes ↓ Reconnect battery Go to next step.	
	3. Switch off all power and close the enclosure rear cover.

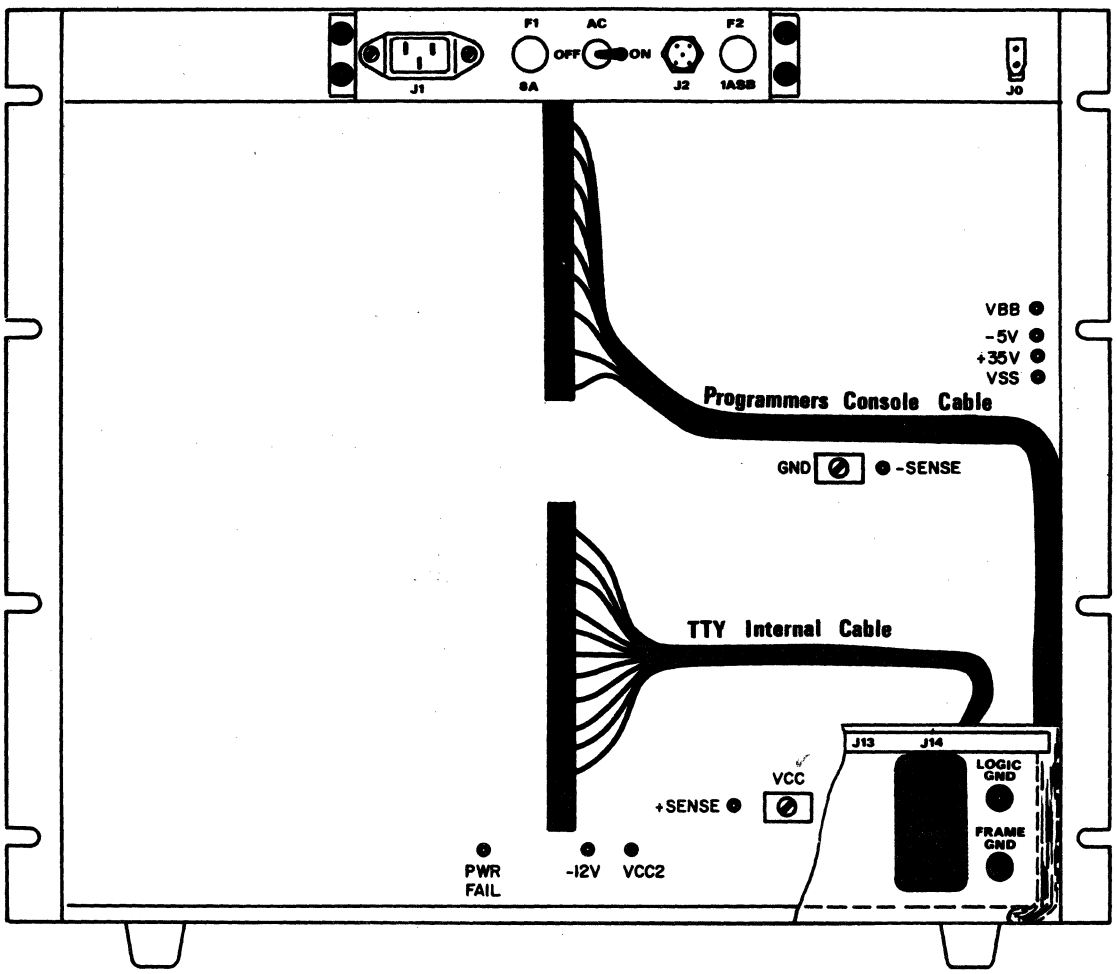


Figure 6-1. Computer Backplane Showing the Power Supply Test Points

INSPECTION OR REPLACEMENT OF PRINTED WIRING BOARD

Should it be deemed necessary to remove or inspect any of the printed circuit assemblies in the enclosure, proceed as follows:

NOTE

Make sure that system is not operational before switching off system power.

WARNING

Do not remove any circuits with the enclosure power on.

1. System power off. (Power off Procedure, refer to page 6-27).

2. In a system including the expansion enclosure its power must be switched off before the main enclosure.

1. Open enclosure front door.

NOTE

When removing a printed wiring assembly note its slot number carefully for future reference.

2. Remove the suspected printed wiring assembly from its place in the enclosure using the card extractor tool (part 89670300) as illustrated in Figure 6-2.

WARNING

Memory Module assemblies (equipments BA201-A, BA201-B) require special handling: refer to Section 7, Protection Against Catastrophic Damage.

3. Replace a suspected PWA into its slot only if it is not faulty. Otherwise substitute a fully tested similar PWA.

4. Close front door of enclosure.

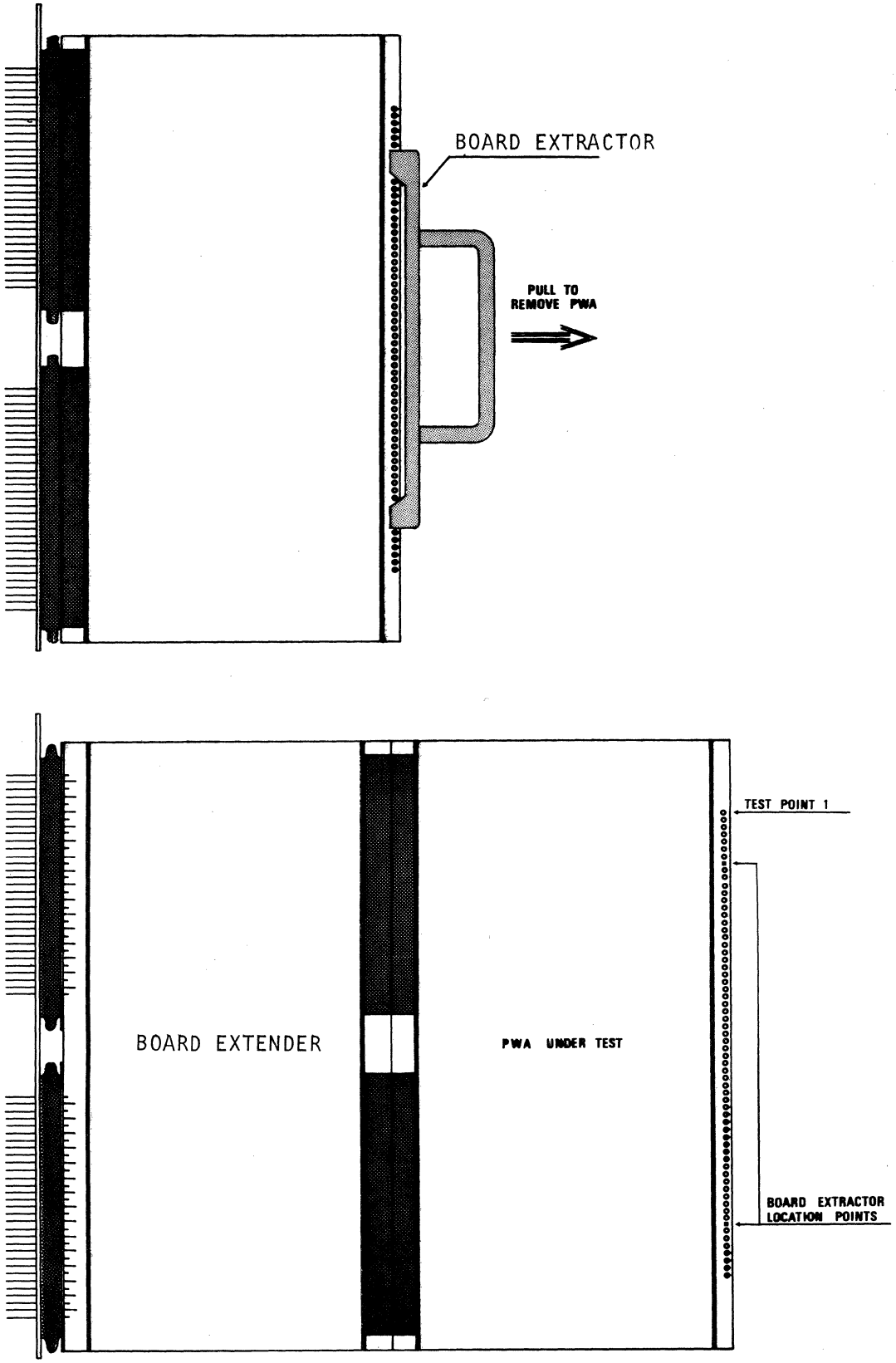


Figure 6-2. Use of Board Extractor and Board Extender

INSPECTION OR REPLACEMENT OF THE POWER SUPPLY UNIT

Should it be deemed necessary to remove or inspect the power supply unit in the enclosure, proceed as follows:

NOTE

The power supply unit should not be repaired in the field. In case of a fault the unit should be replaced as a whole.

1. System power off. (Power off procedure, refer to page 6-27).
2. In a system including the expansion enclosure, its power must be switched off before the power of the main enclosure.

1. Open the enclosure front door.

WARNING

The power supply does not use an input isolating transformer and parts of its circuits are at line voltage during operation. Do not touch the power supply unit while the line cord is plugged in.

2. Remove the power supply heat shield by removing its retaining screws on the inside of the enclosure front door (refer to Figure 6-3).
3. Remove all connections from power supply connector panel (refer to Figure 6-4).
4. Remove the power supply unit by removing its retaining screws (refer to Figure 6-5).
5. Reconnect the power supply after repair and testing or reconnect another one by reversing the procedures under 3 and 4 above.
6. Recalibrate the power supply voltages as described earlier in this section.
7. Replace the power supply heat shield by reversing procedure in 2 above).
8. Close enclosure front door.

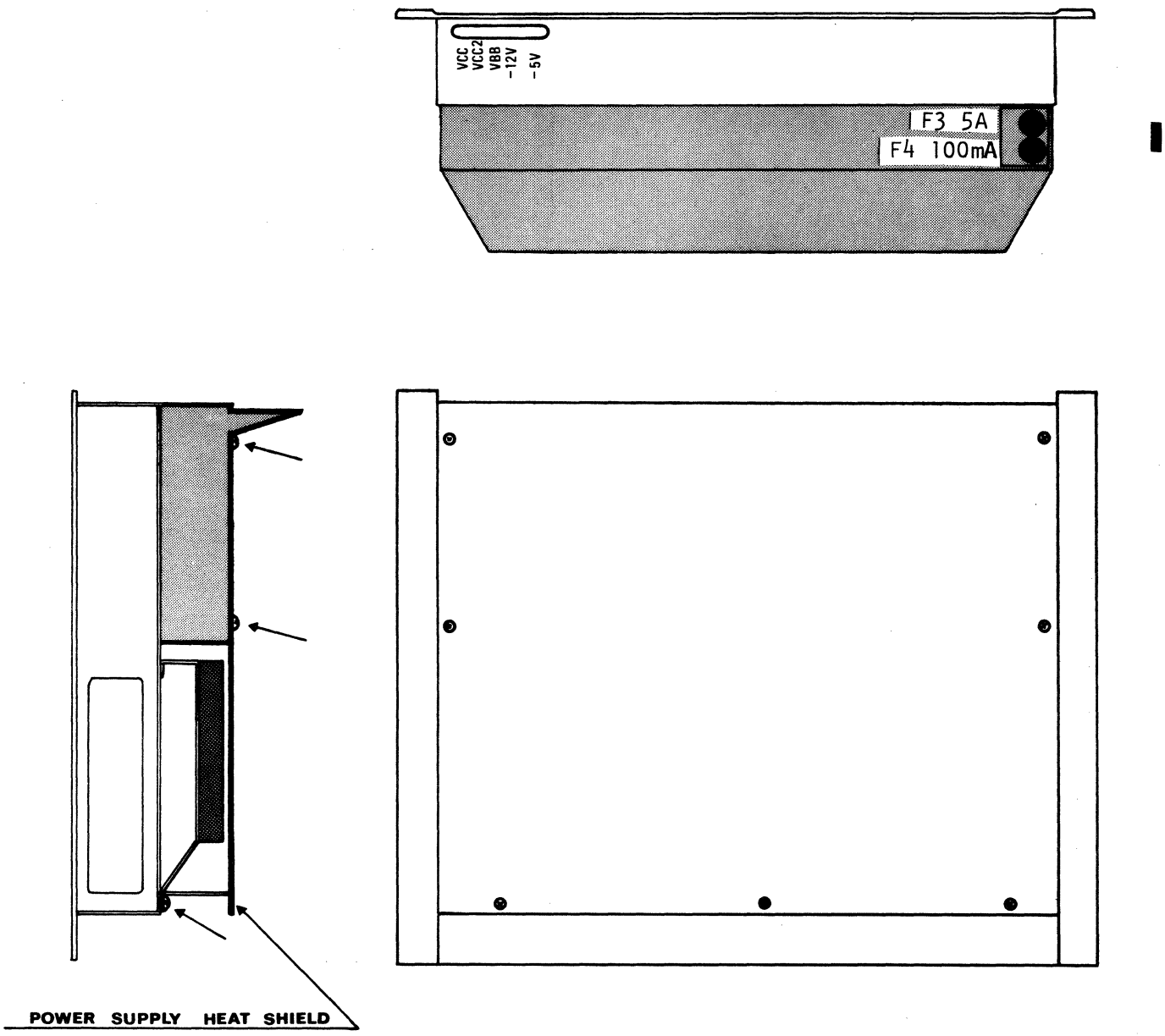


Figure 6-3. Power Supply Heat Shield and Retaining Screws

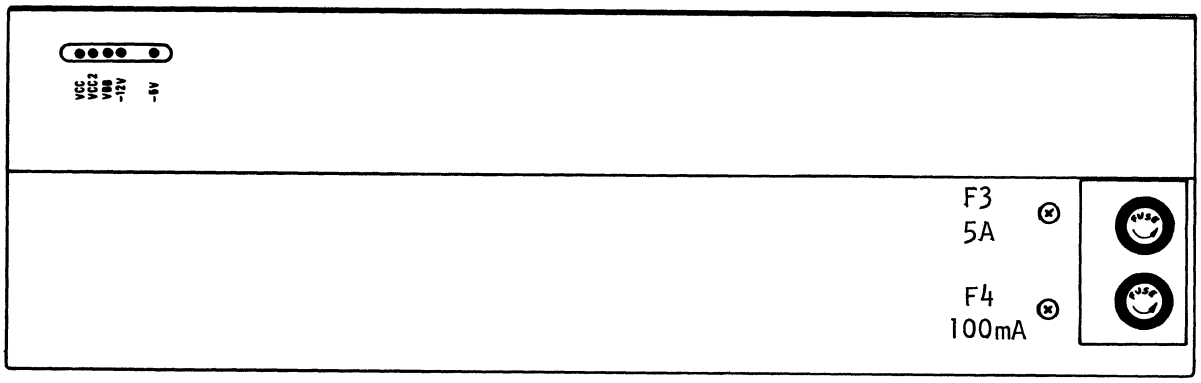


Figure 6-4. Power Supply Adjustments and Fuses

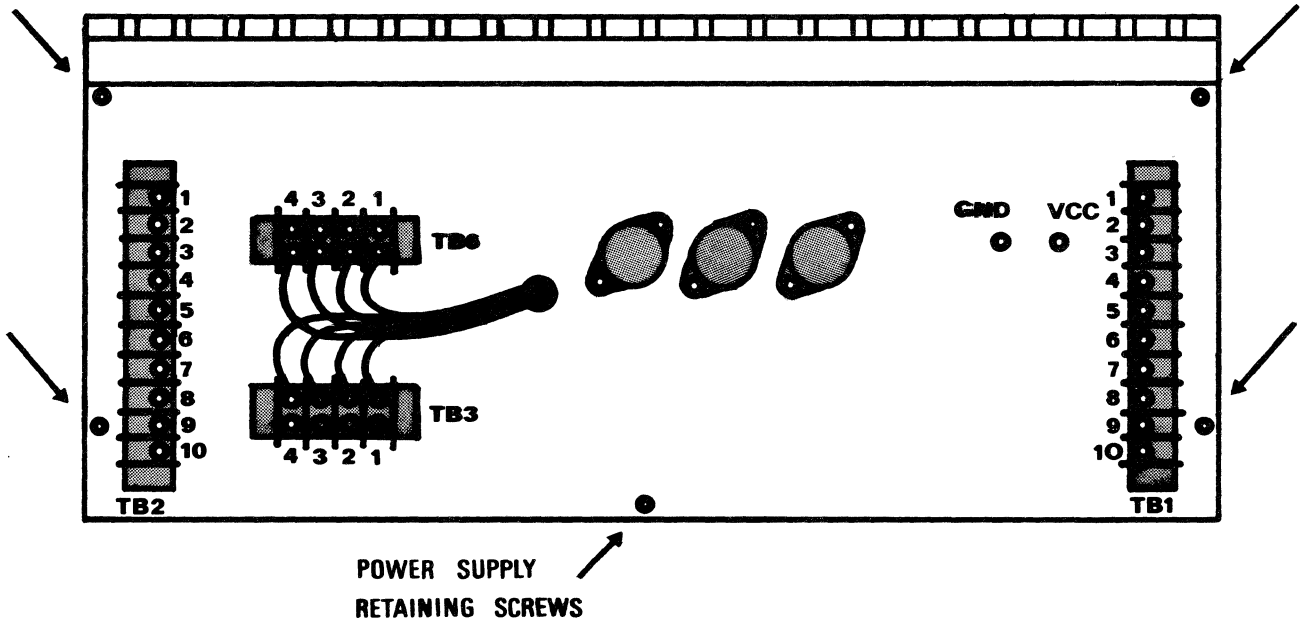


Figure 6-5. Power Supply Terminals and Retaining Screws

CHECK PROGRAMMER'S CONSOLE CONTROLS AND INDICATORS

NOTE

Section 2 describes the controls and indicators of the Programmer's Console. These tests relate only to the main computer enclosure after its proper installation.

Check/Condition	Action
1. System power on	1. Press MASTER CLEAR switch
Check that all lights corresponding to register positions (except the Breakpoint register) on the front panel are extinguished.	
Yes — No →	a. Take appropriate action b. Repeat check
→	2. Press the M register selector and the data enter pushbutton switches (0 through 15)
Check that all indicators corresponding to the switches pressed light	
Yes — No →	a. Take appropriate action (1) b. Repeat check
→	3. Press CLEAR button
Check that all data enter indicators are extinguished	
Yes — No →	a. Take appropriate action (2) b. Repeat check
↓ Go to next step	

Notes: refer to next page.

4. Repeat 2, 3 for registers P, Y, X, A, Q, B

5. Actuate each of the following switches in turn:

   AUTOLOAD, MANUAL INTRPT., STOP, MASTER CLEAR, GO

   All pushbutton switches

Check if the switches operate correctly (refer to Section 2 and the SMM manual).

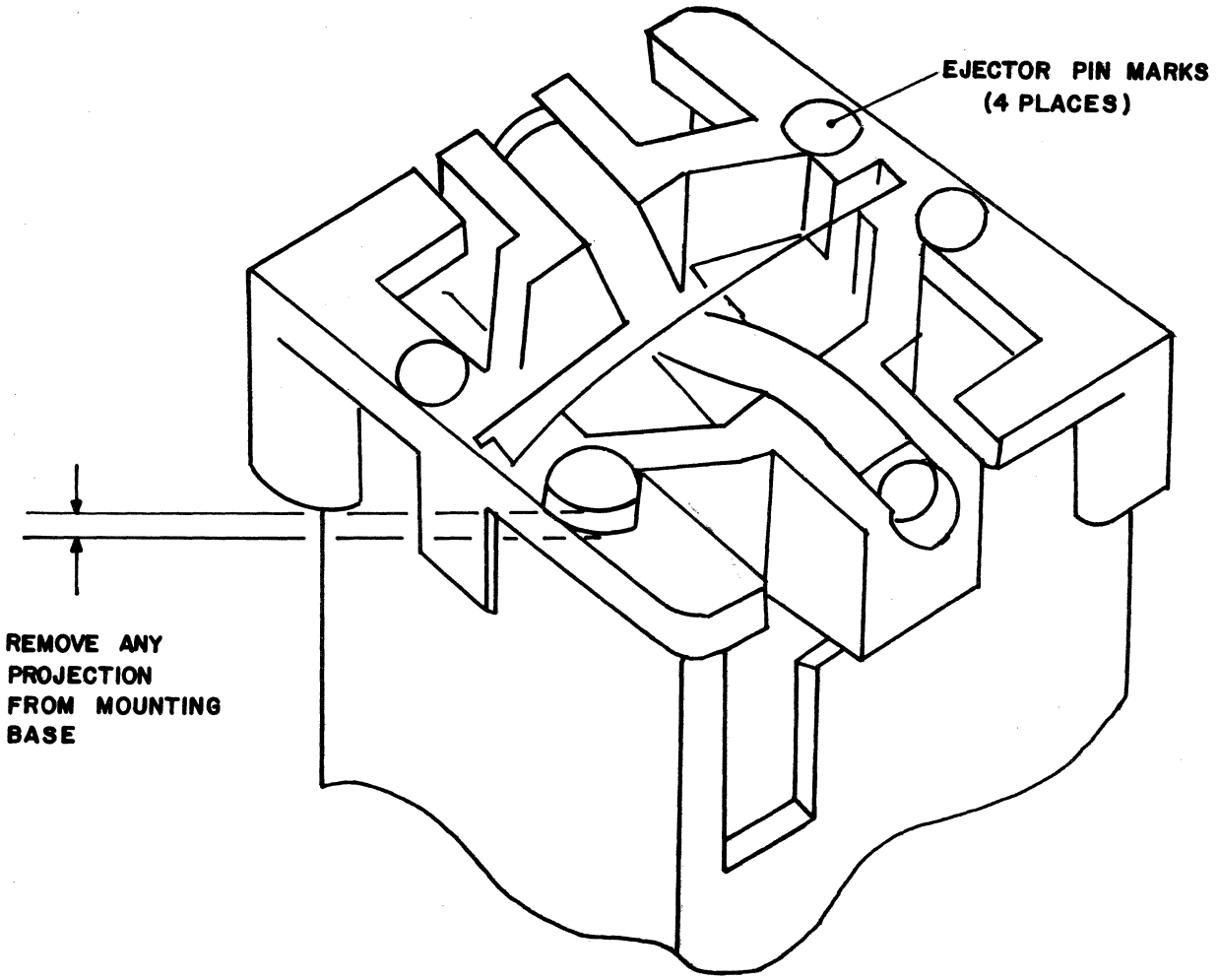
Yes ↓ Go to next step

No → a. Take appropriate action(3)
b. Repeat check

2. Controls and Indicators checked.

Notes:

1. The CLEAR and MASTER CLEAR functions are defined in the Computer System Reference Manual (publication number 89633400). The signals may be traced with the aid of the Programmer's Console basic diagram (refer to Section 5) and the back-plane wire list (refer to Section 9).
2. To replace an indicator lamp, carry out the appropriate procedure outlined in the following pages.
3. To replace a pushbutton switch, carry out the appropriate procedure outlined in the following pages.



Bottom View of Programmer's Console Pushbutton Switch Part No. 89652300
(See also CDC Specification 89652300)

INSPECTION OR REPLACEMENT OF PROGRAMMER'S CONSOLE

Should it be deemed necessary

- to inspect or remove the Programmer's Console printed wiring assembly;
- to inspect or replace a pushbutton switch or indicator lamp,

proceed as follows:

NOTE

Make sure that system is not operational before switching off system power.

1. Switch off system power according to Power Off procedure below.

1. Open the enclosure front door.

2. Remove the power supply heat shield by removing its retaining screws on the inside of the computer enclosure front door (refer to Figure 6-3).

3. Remove two screws holding cover of front panel from the rear of the front door (refer to Figure 6-6a).

4. Remove two small front covers (carrying names of switches and indicators) from the front of the door.

5. Remove three screws from each of the two edges of the front panel as shown on Figure 6-6b.

WARNING

Do not remove the other four screws on the (hinge side) edge of the front door, as these secure the door to the enclosure.

SYSTEM 17 PROGRAMMERS CONSOLE
PUSH BUTTON SWITCH INSTALLATION

1. SCOPE

These instructions detail requirements for installing push button switch P/N 89652300, used on System 17 Programmer's Console P/N 89640300.

2. APPLICABLE DOCUMENTS

CDC SPEC 89652300 - Push Button Switch, SPST.

3. REQUIREMENTS

4. Premounting Preparations

5. Switch Preparation - Switch mounting base shall be free from burrs, as outlined in Figure 1, and other undesireable projections. Note, the Rohdium alloy contacts project 0.0035 inches below the mounting base. A smooth, projection free, mounting base is imperative for proper switch operation.

6. Printed Wiring Board Preparation - Cleaning

The switch is sensitive to cleaning solvents. Safe cleaning solvents to use are trichlorethylene, methyl denatured alcohol or isopropyl alcohol. PWB's shall be cleaned and dryed before mounting the switch and not afterwards.

WARNING

Do not use Freon TMC. It will eat away at the plastic material. Freon TF will distort the silcone rubber tube.

Deleted per Rev F

9. Check the pushbutton switch (refer to previous subsection).

3. To replace an indicator lamp on the Programmer's Console assembly, perform steps 10÷13.

(Indicator lamp: CDC P/N 8963700)

10. Locate and remove the faulty indicator lamp: unsolder the two legs of the lamp and remove it. To remove unwanted solder use suitable copper braid.

WARNING

Do not use suction to remove unwanted solder, suction may lift off printed conductors from the board.

11. Clean the printed wiring board with methyl denatured alcohol or isopropyl alcohol.

12. Mount the replacement indicator lamp by inserting its two legs in the freed holes until the lamp is seated flat against the board. Carefully solder the two legs to the printed wiring pads. Remove unwanted solder and clean the area using the materials of step 11.

13. Check the indicator lamp (refer to previous subsection).

4. To replace the Programmer's Console assembly follow steps 14 through 16.

NOTE:

Steps noted by asterisks apply to series A12 and down. For other series, see the notes at the bottom of this page.

14. Proceed in removing the whole Programmer's Console by the following procedure:

- * unsolder the power supply connection at bottom right hand corner of the assembly (looked at from the inside of the front door of the enclosure: refer to Figure 6-6a)

- ** open rear cover of enclosure, remove the connector of the assembly (refer to Figure 6-1) and slide the cable and connector through under the card nest to the front of the enclosure

- remove the printed wiring assembly by removing 10 screws around its periphery.

15. To reconnect the printed wiring assembly after repair or with another, good one, reverse the order of procedures 1 through 5 and 8.

16. Check all Programmer's Console indicators and switches according to the instructions (refer to previous subsection).

* This step in the procedure applies only to series A12 and down. For series A13 and up, including models C and D, this instruction reads:
- remove the power supply connector at bottom right hand corner of assembly (looked at from the inside of the front door of the enclosure). Refer to figure 6-6a.

** This step applies only to series A12 and down. For series A13 and up, including models C and D, this instruction reads as follows:
- disconnect the two connectors on the programmer's console card which attach the main harness. They are marked J20 and J21 on the enclosure.

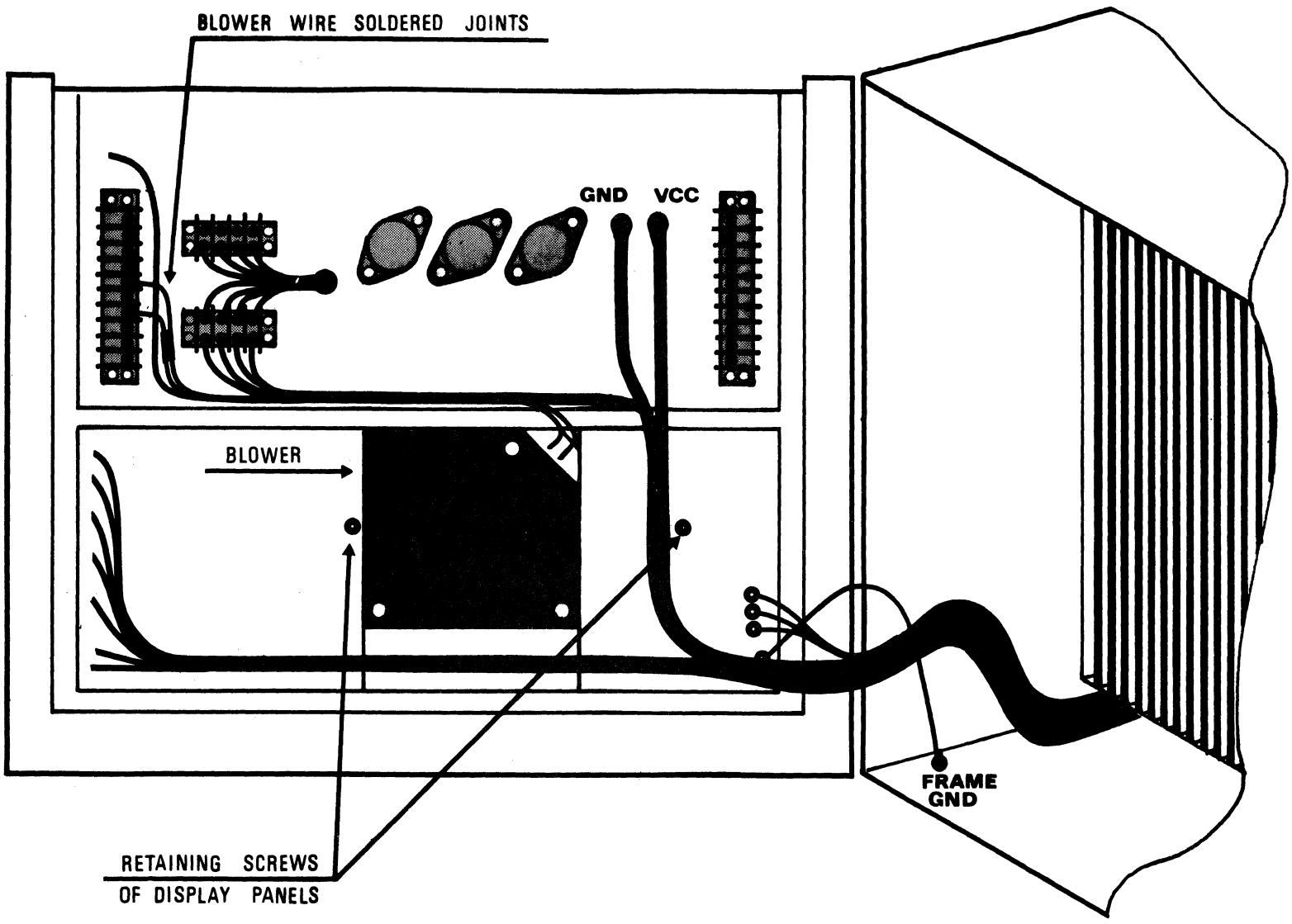


Figure 6-6a. Inside of Computer Enclosure Front Door

Note: This view does not apply to all series. See the note on page 3-7.

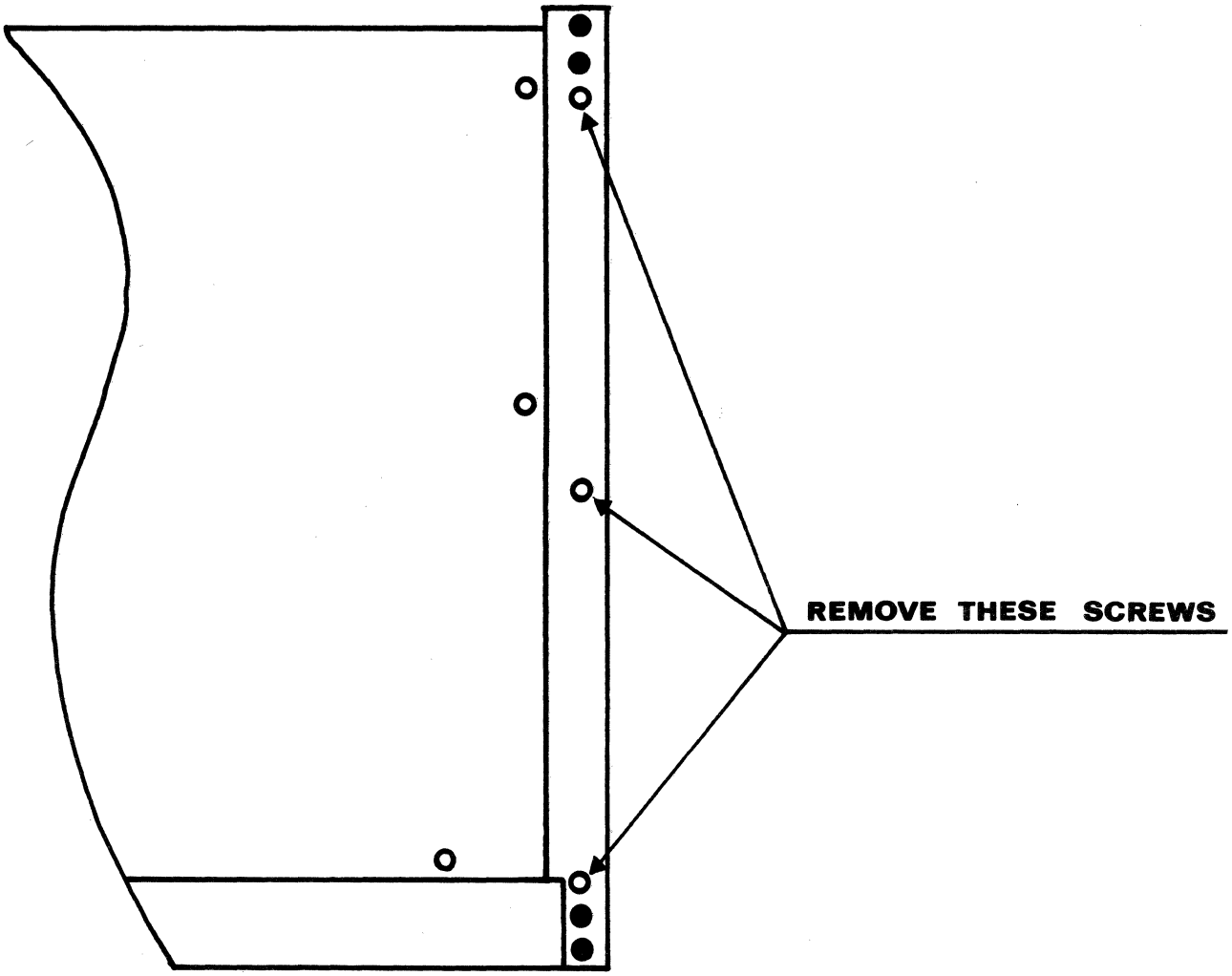
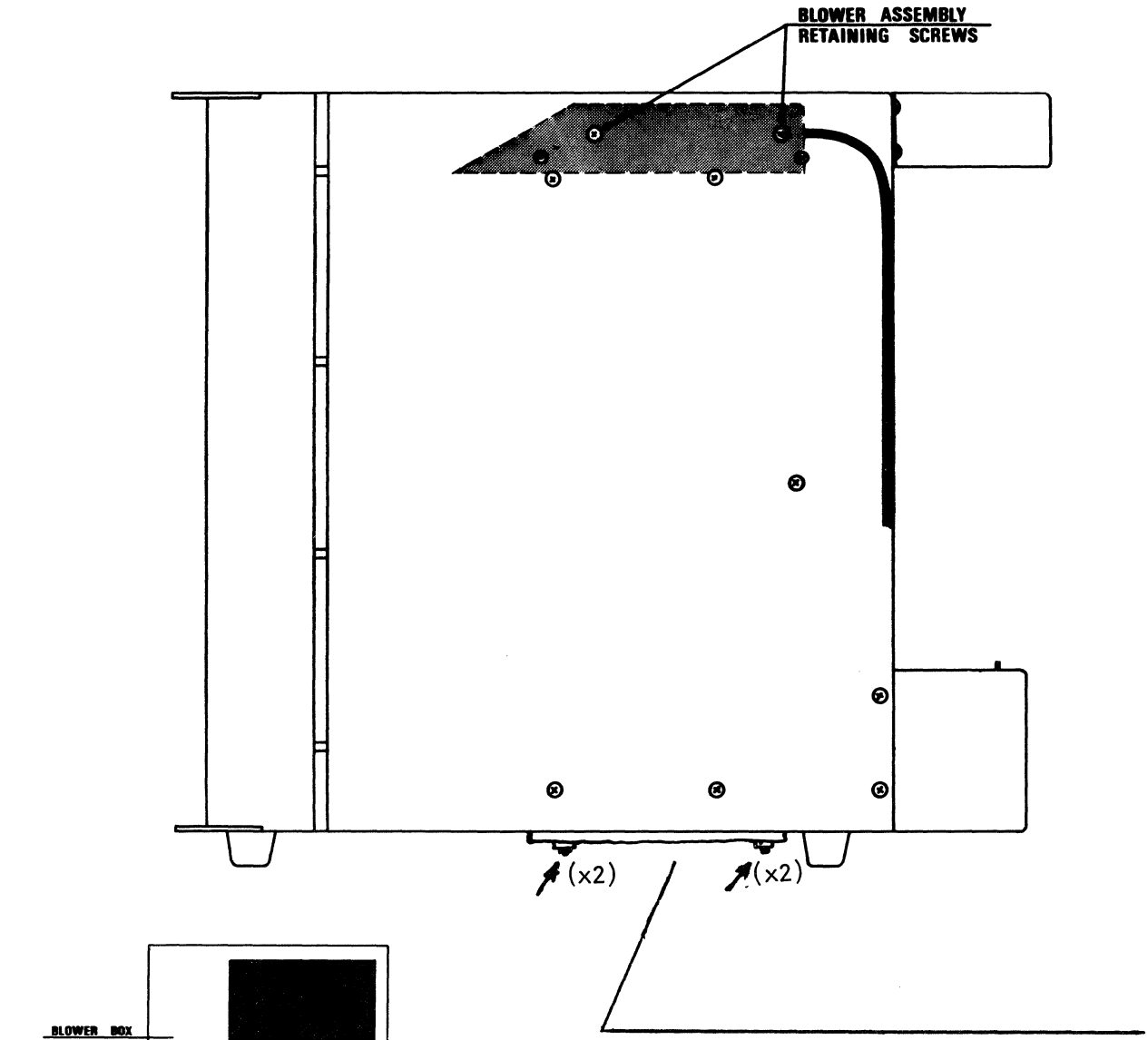


Figure 6-6b. Inside of Computer Enclosure Front Door.



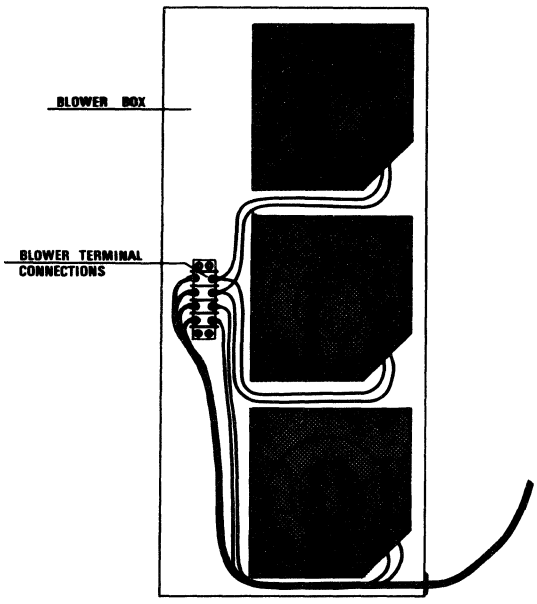


Figure 6-7. Blower Assembly in Top of Enclosure (All Type Identifiers)

INSPECTION OR REPLACEMENT OF COOLING BLOWERS

Each enclosure of type C or D is cooled by six centrifugal blowers. Three blowers are housed in the top of the enclosure (figure 6-7), two in the bottom of the enclosure(not installed in type A, see figure 6-7), and one blower is in the front door of the enclosure. (figure 6-6a). The blower in the front door cools the power supply unit mounted above it. The blowers in the enclosure (three on top and two on bottom) supply cooling air to the printed wiring assemblies in the main body of the enclosure.

Should it be deemed necessary to inspect or remove one or more of the blowers, follow the appropriate procedure outlined below.

WARNING

The computer must not be operated or switched on with the blowers outside the enclosure, or otherwise not operational.
Note that free access of air around the enclosure must be maintained.

Inspection of the blower in the front door

Provided proper care is exercised system power need not be switched off.

1. Open the enclosure front door.
2. Inspect the blower visually. To check the airflow a sheet of paper may be placed momentarily on the air inlet: with proper airflow the paper will be sucked close to the body of the blower.
3. If the blower does not function switch off the power to the enclosure immediately (refer to Power Off Procedure), check wiring continuity according to appropriate wiring diagram (see Section 5) and if necessary, remove the blower. Otherwise close the enclosure front door and proceed with normal operation or further checks.

Inspection of blowers in the enclosure

To inspect the three blowers in the top of the enclosure and the two blowers in the bottom, they have to be slid out from the body of the enclosure.

1. Make sure that the system is not operational and switch off the system power according to Power Off Procedure.

CAUTION

In step 2, do not let the blower box that is mounted in the bottom of the enclosure fall freely after its four mounting screws have been removed. Support it by hand or some other way, to prevent strain and possible damage to the two connectors.

2. Undo the screws holding the blower box (two screws on either side of the enclosure: refer to Figure 6-7). See Caution.

3. Open the enclosure front door.

4. Slide out the blower box carefully and inspect the blowers and the wiring. To check the airflow of the blowers, prepare a sheet of paper, switch on the power to the enclosure for a very short time and place the sheet of paper across the inlet of each blower momentarily; with proper airflow the paper will be sucked close to the body of the blower.

5. If one of the blowers does not function, check wiring continuity according to appropriate wiring diagram (refer to Section 5) and if necessary, remove the blower according to outline procedure below. Otherwise slide back blower box carefully, replace the four screws holding it, close the enclosure front door and proceed with normal operation or further checks.

Removal and replacement of a blower

NOTE

Make sure that the system is not operational before switching off system power.

Before removing a blower inspect it (see two previous subsections) and make sure that its removal is necessary.

1. Undo electrical connection of the blower:

   a. the wire of the blower in the front door is part of the cable form of the door; to remove the blower connection cut the lacing of this cable, cut the heat-shrinkable tubing over the blower connection and cut the wires (Figure 6-6a);

   b. the blowers in the top part of the enclosure are wired through a terminal block (refer to Figure 6-7); to disconnect a blower its wire has to be removed from this terminal block.

ADDENDUM:

c. the blowers in the bottom part of the enclosure are wired to individual connectors (figure 6-8). To disconnect a blower, pull out its plug.

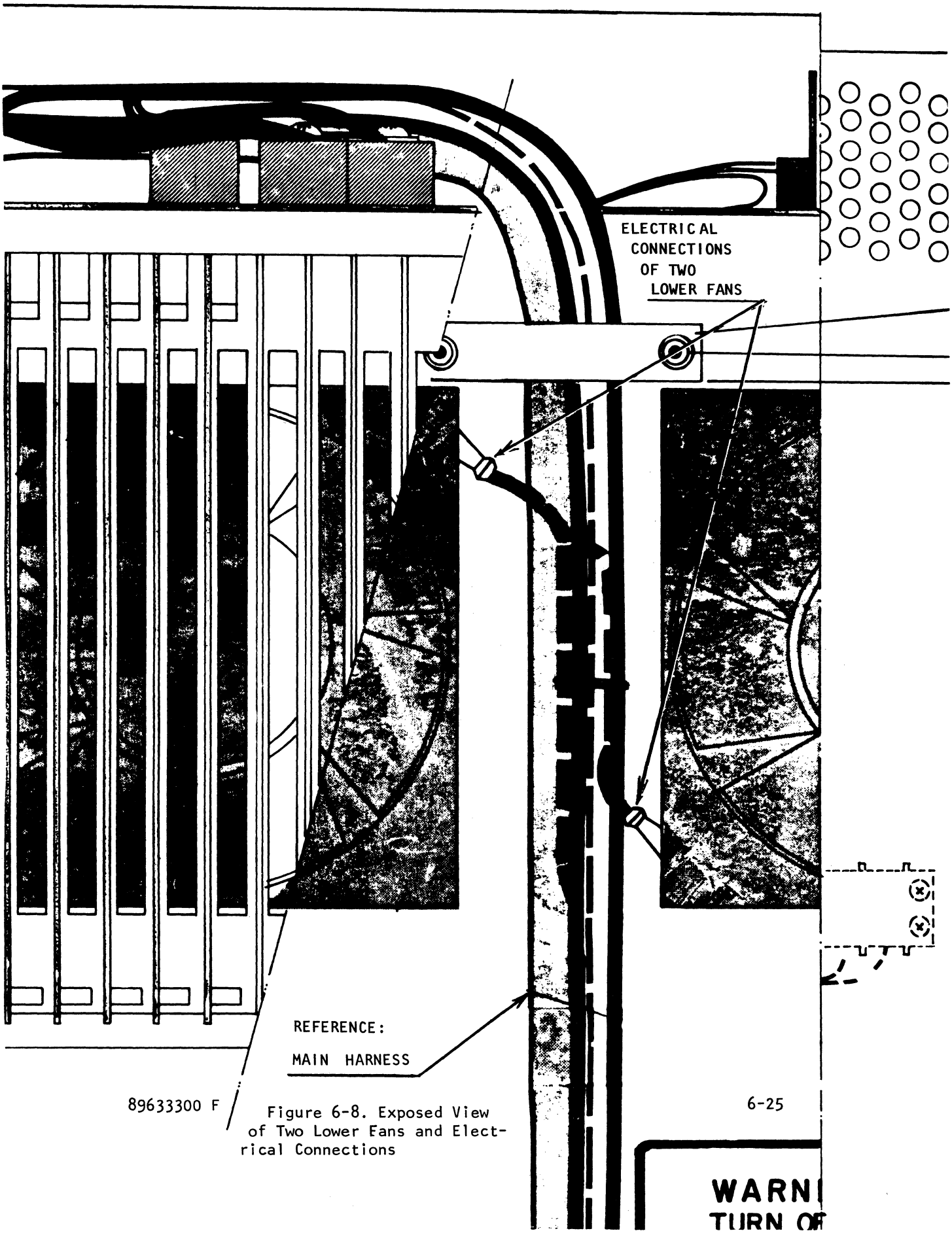
2. Remove the blower bodily by undoing the three screws holding it (refer to Figures 6-6a, 6-7).

WARNING

Do not operate or switch on the computer without one of the blowers.

3. Ensure that replacement blower is in good working order. Install it by reversing the procedure of paragraphs 2 and 1 above.

After installation inspect the blowers and close the enclosure (refer to previous subsections).



89633300 F

Figure 6-8. Exposed View of Two Lower Fans and Electrical Connections

POWER ON: PROCEDURE FOR SWITCHING ON POWER

To apply power to the computer (equipment AB107/AB108) and the Expansion Enclosure (equipment BT148), proceed as follows:

NOTE

It is assumed that the equipment has been installed and is operational. For Power On Procedure on first installation refer to Section 3 of this manual.

1. Make sure all the power switches of the computer are off. The switches are listed in the following table:

Equipment	Switch Designation	Location
AB107/AB108	AC POWER	Rear Panel
	DC POWER	Front Panel
BT148	AC POWER	Rear Panel
	DC POWER	Front Panel

2. Make sure that the power cord of each enclosure is connected to a utility outlet.

3. Switch on the power to the utility outlets.

4. Turn on the equipment switches in the following order.
On turning on the DC POWER, the associated indicator should light.

Step	Equipment	Switch Designation	Location
1.	AB107/AB108	AC POWER	Rear Panel
2.	AB107/AB108	DC POWER	Front Panel
3.	BT148	AC POWER	Rear Panel
4.	BT148	DC POWER	Front Panel

POWER OFF: PROCEDURE FOR SWITCHING OFF POWER

To remove the power from the computer (equipment AB107/AB108) and associated Expansion Enclosure (equipment BT148) proceed according to the following instructions:

EMERGENCY SHUT-DOWN

In case of emergency (suspected burning in the computer and associated equipment) perform any one or all of the following steps (the steps are given in order of preference):

Step	Action	Location
1.	Switch off circuit breaker of installation	Depends on installation
2.	Switch off AC POWER switch on each equipment	AB107, AB108, BT148 } rear panel
3.	Pull power cord(s) from utility outlet	Utility outlet(s)

REGULAR SHUT-DOWN

To shut down the computer proceed as follows:

1. Make sure that the system is not being operated.
2. Turn off the equipment switches in the following order:

Step	Equipment	Switch Designation	Location
1.	BT148	DC POWER	Front Panel
2.	BT148	AC POWER	Rear Panel
3.	AB107/AB108	DC POWER	Front Panel
4.	AB107/AB108	AC POWER	Rear Panel

DIAGNOSTICS AND MARGIN TESTS

TEST PROGRAMS

SMM17 Memory, Command and Random Protect Tests.

TEST CONDITIONS (See also table 6-1)

CONDITION	VCC	VSS	NOMINAL DC VOLTAGES
1	+5%	+5%	VCC: +5.0 VDC VCC2: +5.3 VDC VSS: +16.7 VDC (AB107) VSS: +19.7 VDC (AB108) VBB: VSS + 3.5 VDC -12 -12.0 VDC - 5 - 5.0 VDC
2	-5%	+5%	
3	-5%	-5%	
4	+5%	-5%	

Operational Tests

At nominal voltages, run several passes of each SMM test. No errors on any test are allowed.

Run several passes of each test at each of the 4 conditions listed above.

Return the supply to its nominal values, and re-run the tests. Shock testing is not recommended, but very light tapping should not produce errors.

SECTION 7

MAINTENANCE AIDS

TTL CIRCUIT OPERATION

The transistor-transistor logic (TTL) is analogous to diode-transistor logic (DTL) in certain respects. As shown in Figure 7-1 a low voltage at inputs A or B will allow current to flow through the diode associated with the low input, and no drive current will pass through diode D_3. If inputs A and B are raised to high voltage, drive current will pass through diode D_3.

In TTL circuitry the multiple-emitter transistor performs the same function as the diodes in DTL (see Figure 7-2). However the transistor action of the multiple-emitter transistor causes transistor Q_1 to turn-off more rapidly thus providing an inherent switching-time advantage over the DTL circuit.

Although one-volt dc noise margins are typical for TTL circuits, an absolute guarantee of 400 millivolts is given for every unit by manufacturers.

Each output is tested to ensure that the logic high output voltage will not fall below 2.4 volts. This is done with full fan-out, lowest V_{cc} and 0.8 volt on the input: 400 mV more than the logical low maximum.

Each output is tested to ensure that the logic low output voltage will not exceed 0.4 volt. This is done with full fan-out, lowest V_{cc} and 2 volts on the input: 400 mV less than the logic high minimum.

In actual system operation, the majority of circuits do not experience worst-case conditions of fan-out, supply voltage, temperature, and input voltage simultaneously. In addition the threshold voltage of the TTL circuits is about 1.5 volts. These characteristics allow a larger voltage change on an input without false triggering. This typical noise margin is shown in Figure 7-3.

Another important feature of the design is the output configuration which both supplies current (in the logical high state) and sinks current (in the logical low state) from a low impedance. Typically logical low output impedance is 12 ohm and logical high output impedance is 70 ohm. This low output impedance in either state rejects capacitively coupled pulses and ensures small R-C time constants which preserve wave-shape integrity.

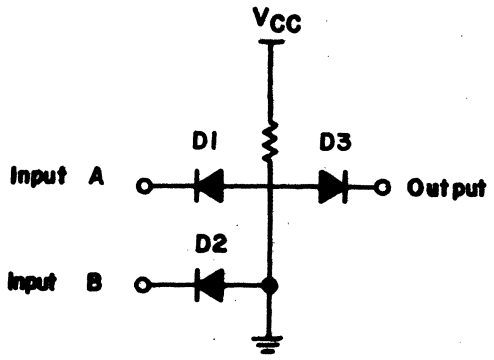


Figure 7-1. Diode AND Gate.

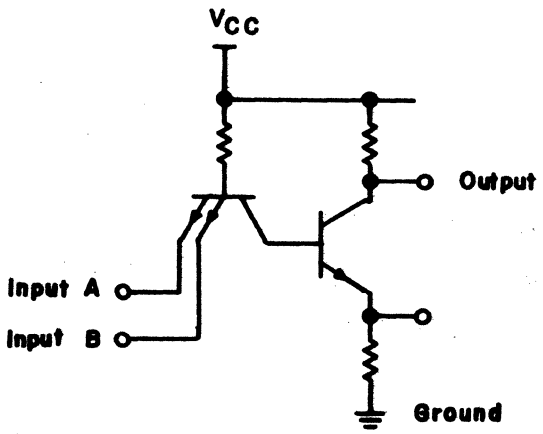


Figure 7-2. TTL AND Gate.

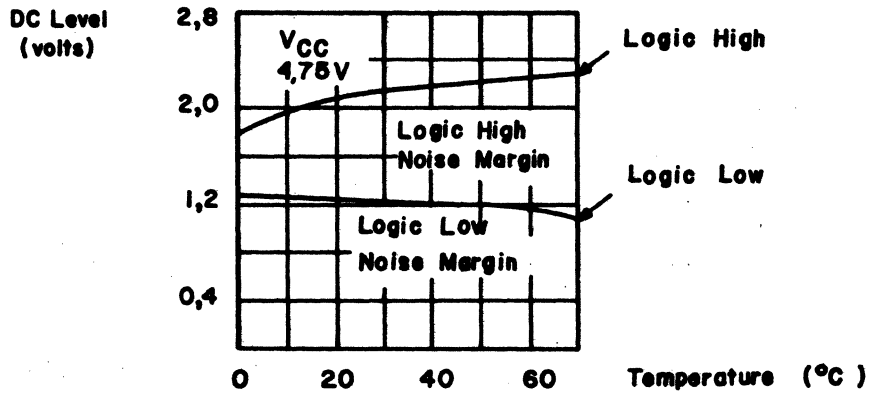


Figure 7-3. Typical Logic Level Margins for TTL Micrologic

MOS CIRCUIT OPERATION

THE MOS PROCESS AND SILICON GATE TECHNOLOGY

The memory unit is realized with silicon gate metal-oxide-silicon (MOS) technology. This technology offers a number of advantages over aluminum gate MOS technology; some of these are listed:

a. Gate oxide is protected immediately on formation in the silicon gate process.

b. The self-aligned gate of the silicon gate device permits the construction of a smaller device with less gate-to-drain capacitance than is possible with aluminum technology. Faster, more compact circuits are made possible.

c. The silicon layer can be used for interconnections, permitting reduced chip area per function. This is an important factor in large scale integrated (LSI) circuits where interconnection area affects cost even more than active component area.

d. Improved reliability of the silicon gate devices due to the number of layers above the gate.

e. Lower threshold voltage due to the use of silicon rather than aluminum as the gate material.

Static and Dynamic MOS Circuits

The characteristics of the MOS field-effect-transistor (MOSFET) permit the construction of a wide variety of logic circuits with a large device and function density while giving good reliability and yield. An example of the application of these circuits is the memory unit of the computer, a 1024-bit random access, fully decoded read-write memory unit, accommodated on a single semiconductor chip.

In general the MOS device may be used as an active amplifier or as a load resistor. Typical characteristics of a MOSFET device are shown in Figure 7-4, together with a curve corresponding to it used as a load resistor with a 12 volt supply. The curves show drain current (I_D) versus drain-to-source voltage (V_{DS}) with gate-to-source bias voltage (V_{GS}) as a parameter. The substrate is assumed to be at source potential. The load resistor curve is approximate as substrate bias effects have been neglected. In the following discussion on the various circuits high and low refer to the relative magnitude of the voltage with respect to the substrate voltage level (V_{SS}). Polarities are taken as correct for a p - channel device, i.e., all voltages negative with respect to the substrate. Note that the supply voltage for MOS devices is typically -15 to -18 volts; the logic high and low signals to the memory unit are typically as follows:

	min.	max.
input low voltage	V_{SS} - 17	V_{SS} - 14.5
input high voltage	V_{SS} - 0.7	V_{SS} + 1

Four types of MOSFET inverter stages are shown in Figure 7-5. In Figure 7-5a two MOS devices (Q1, Q2) are wired as a static inverter. When input is sufficiently high, Q2 turns on and the output is low. If the input is low it causes Q2 to be off and Q1 pulls the output high. This circuit requires that for equivalent bias, Q2 should have much higher conductance than Q1 to get reasonable noise margins; the two devices have therefore radically different geometries. This is shown in Figure 7-5a by representing Q1 as a resistor and Q2 as a FET. As a result of the low conductance of Q1, current available from it to charge load capacitances is quite limited in this inverter and low-to-high transitions are rather slow.

The circuit of Figure 7-5b is similar to that in Figure 7-5a when the clock is active. By making the clock voltage higher than V, a more consistent high output level is established. Once the output level is established, the clock may be switched off to save power. This technique is used in the low power data retention mode of operation (LPDR) to conserve battery and may be used also to give improved noise margins.

The circuit of Figure 7-5c behaves as an inverter when the clock is active (high). This circuit may be used to drive relatively large capacitive loads through the high conductance of Q1, though it may consume relatively large amount of power while both the input and the clock are active (high).

In the circuit of Figure 7-5d the capacitive load is charged when the clock input C is high and is discharged when C goes low, provided that the input is high. This circuit draws current only to charge and discharge the load and there is no dc drain. The load capacitance is, however, reflected back into the clock driver.

The circuits of Figures 7-5b, c, d make use of temporary retention of data on the load capacitance and are therefore said to be dynamic, while that of Figure 7-5a is dc-stable and therefore static.

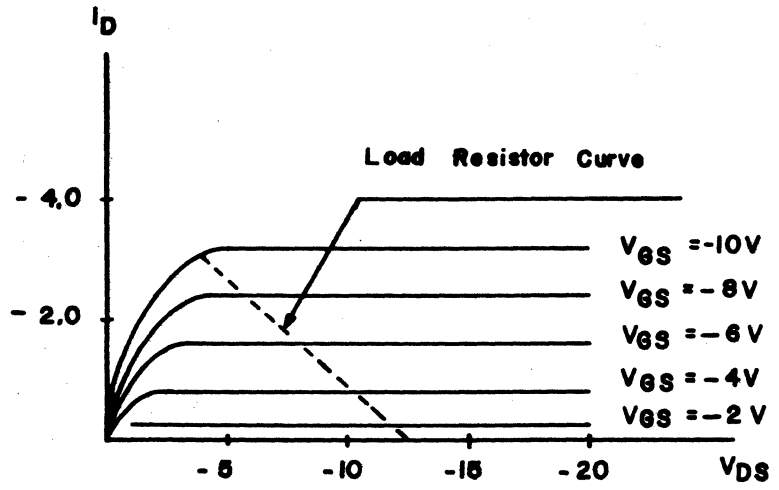


Figure 7-4. Typical MOS Characteristic

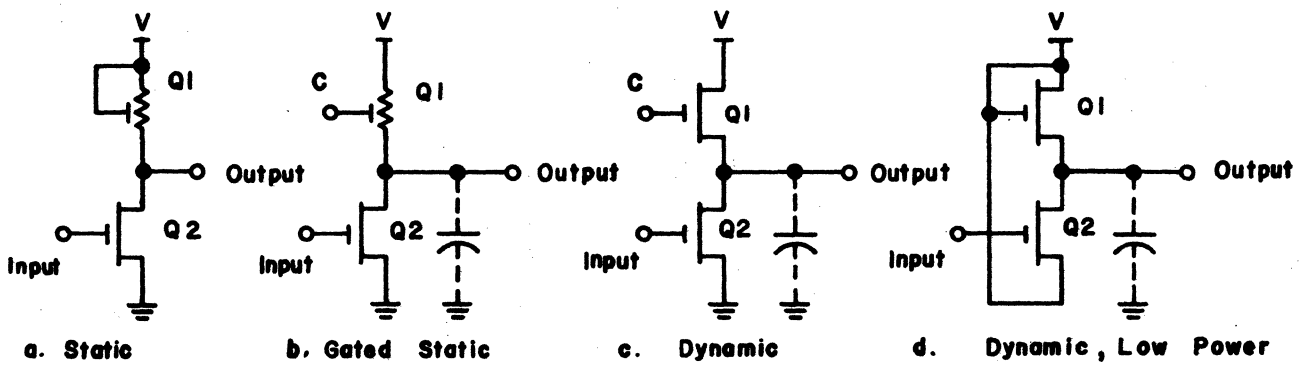


Figure 7-5. MOS Inverter Circuits

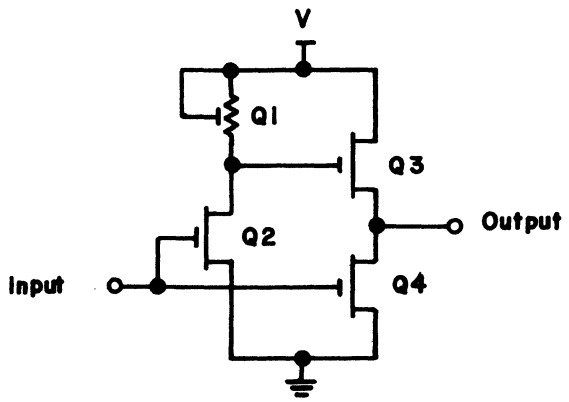


Figure 7-6. MOS Inverter with Output Booster

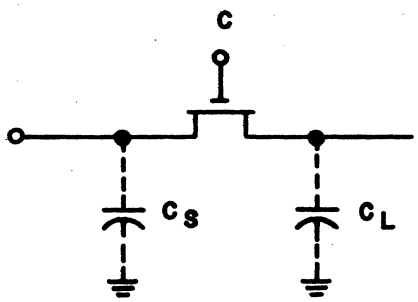


Figure 7-7. MOS Transmission Gate

Larger capacitive loads may be driven by static inverters only if a booster stage is added. A loss of high level is introduced unless bootstrap techniques are used. A booster stage is shown in Figure 7-6.

A transmission gate is shown in Figure 7-7. The load capacitance C_L is charged towards the voltage on the input capacitor C_S when the clock C is high. When the clock input is returned low it switches off Q1 and C_L retains the voltage it was charged to.

The circuit of Figure 7-7 may be driven from a number of different source circuits. When the source is dynamic the transmission gate clock C should be kept high during the entire period when C_S and C_L are being charged and discharged, otherwise improper voltages may result. For example if C_S is initially charged and C_L initially discharged, they will share their charge when the transmission gate is opened by the clock being made active. The voltage on the capacitors will thus be a function of the relative values of the two capacitors. Unless the circuit is designed to operate with such intermediate voltage levels incorrect operation will result.

Such circuits make up the memory unit (Section 4) which work together with auxiliary and control circuits in the memory module, memory address and memory control circuits.

PRECAUTIONS IN HANDLING THE MEMORY MODULES

The memory banks are arrays of memory units mounted on the Memory Modules. The memory units are MOSFET circuits characterized by very high impedances and some special precautions should be observed while handling them both in and out of circuit.

PROTECTION AGAINST CATASTROPHIC DAMAGE

As with any semiconductor component, the memory units can be damaged by misuse, or misapplied voltages. The component should be protected from such misuse during shipment, handling, and when installed in the system.

MOS circuits are characterized by high impedances, and therefore are capable of being charged to high voltages by static charges. The gate circuits of MOS transistors are subject to destructive breakdown if excessively charged. The memory unit has an effective gate protection circuit for all input connections, and requires no elaborate precautions in normal use. However, some environments are subject to extreme build up of static charge, and are capable of releasing sufficient amounts of energy to damage any semiconductor component. MOS components in particular should be protected from these static charges. Some precautions which are easy to implement and yet which are quite effective are:

a. Carry components and memory unit cards in conductive trays, such as metal or foil-lined pans.

b. Personnel must touch ground, the chassis or the carrier tray before picking up components and memory unit cards. Avoid high static materials and fabrics in work areas.

SECTION 8

PARTS LIST

PARTS DATA (Sheet 1)

Use the parts listed below to maintain the equipments listed on page iii. Numbers enclosed in parentheses indicate notes.

PART NAME	PART NUMBER IN EQUIPMENT			
	AB107-A/C/D	AB108-A/C/D	BT148-A/C/D	BU120-A
ALU PWA	89614100	89614100		
Timing PWA (1)	89778200	89778201		
Decoder PWA	89934400	89934400		
I/O Interface PWA (1)	89791300	89791300		
TTY Controller PWA (6)	89967400	89967400		
Console Interface PWA	89600043	89600043		
Memory Address PWA	89615000	89615000		89615000
Memory Control PWA	89949000	89949000		89949000
Programmer's Console PWA (2,3,4)	89602069	89602069		
Console Cable Assembly (2,5)	89893800	89893800		
Power Supply Unit (7)	89997700	89997700	89997700	
Fuse, 5A, fast blow	92371016	92371016	92371016	
Fuse, 100 mA, slow blow	93419306	93419306	93419306	
Fuse, 8A, slow blow	92383005	92383005	92383005	
Fuse, 1A, slow blow	93419222	93419222*	93419222	
Blower (mounted in door)	89637100	89637100	89637100	
Blower (mounted in enclosure)	89637100	89637100	89637100	
Lamp, indicator bulb	89637000	89637000		
Switch, pushbutton (3)	89652300	89652300		
Switch, pushbutton (4)	89690200	89690200		
Switch, pushbutton (4)	89764900	89764900		
Connector, plug (5)	53397915	53397915		
Contact, socket (5)	53397918	53397918		
Connector (2)	93947009	93947009		
Contact, socket (2)	51788834	51788834		
Switch, DPDT (AC input)	97030200	97030200	97030200	
Lamp, miniature, 6V (power on)			89818700	

P A R T S D A T A (Sheet 2)

PART NAME	PART NUMBER IN EQUIPMENT AB107/8-A/C/D	AB108-A/C/D	BT148-A/C/D	BU120-A
Switch,toggle, 2P, 7201/J1-CB	89640901	89640901	89640901	
Switch,toggle, 3P, 7203/J2-CB	89640904	89640904		
Lens, lamp red (power on)			89780201	
Lens, lamp, white	89633100	89633100		

Equipment BA201-A, 600 nanosecond Memory, Part Number 89876300
Equipment BA201-B, 900 nanosecond Memory, Part Number 89876600
Equipment GD611-A, Memory Hold Battery, Part Number 89650100

NOTES:

(1) Timing PWA 89778200 (or 89778201) and I/O Interface PWA 89791300 must both be used at the same time. If you replace one, you must also replace the other.

(2a) The P/N for the programmer's Console PWA with its related series code is as follows:

PWA	SERIES
89987600	A04-A12
89987700	A13-A16
89985400	A17-A19
89602068	C01-C03
88602669	D01-

(2b) Programmer's Console PWA P/Ns 89640300 and 89987600 include an integral cable assembly P/N 89893800, used in series A04 to A12. Programmer's Console PWA P/Ns 89881800 and 89987700, used in series A13 up, do not include the cable assembly. To install P/N 89881800 or 89987700 (more lately 89985400 and 89602069) into series A04 to A12, make sure of the following:

* Install cable assembly 89893800 at the same time.
* Use connector 93947009 and four socket contacts 51788834 on the power supply wire harness assembly (P22).

NOTES (continued)

(3) Pushbutton switch 89652300 is used with Console PWA 89640300 in A04 to A12.

(4) Pushbutton switch 89690200 is used with Console PWA 89602069 in A13 up. Twenty-nine switchcaps P/N 89764900 must be ordered together with Console PWA 89602069.

(5) Plug connector 53397915 and contact sockets 53397918 are parts of Console Cable Assembly 89893800.

(6) TTY Controller PWA 89967400 is one of four valid TTY Controller part numbers in the field. See page 5-373 for details.

(7a) The P/N for the power supply PWA and its related series code is as follows:

PWA	SERIES
89964700	A04-A09
89983000	A10-A19
89997700	D01

(7b) Two power supply wiring diagrams and two power supply I/O wiring harnesses are provided in section 5 to cover Power Supply Unit part number 89997700 and the other valid units in the field.

SECTION 9

WIRE LISTS

WIRE LISTS

Table 9-1a gives the wire list for the TTY Internal Cable.

Table 9-1b gives the wire list for the TTY External Shielded Cable.

Tables 9-2 and 9-3 are the wire lists for the Memory Expansion Cables, which form part of equipment BU120-A. Refer to Figure 3-4 for placement details of these cables.

Table 9-4(a) and 9-4(b) give the backplane wiring of the AB107/AB108 in, respectively, signal name order and card slot order. These tables incorporate the wiring for the CPU, Memory System, A/Q and DSA buses and that for the slots preassigned to equipments FA716, FA442, FA446, FV497 and FV618. For slot assigned allocation refer to page 5-6.

Table 9-5 gives the backplane wiring of the BT148 Expansion Enclosure in signal name order. For slot assignment allocation refer to page 5-7.

Table 9-6 supplies the CDT external cable assembly wire list.

Note:

The signal names shown in the wiring lists may differ slightly from those listed in Section 5. Equivalents of typical signal names are given below.

Signal name in - Section 5	Signal name in - Section 9	Notes
ACA05	ACAS	Double/single digit representation of numbers under 10
DØUT07	DOUT7	
ALU00	ALU0L	16 signals to the two ALU assemblies: suffix L: least significant suffix M: most significant
⋮	⋮	
ALU07	ALU7L	
ALU08	ALU0M	
⋮	⋮	
ALU15	ALU7M	
$\overline{MC}$	MC*	Inverse signal: overline/asterisk

TABLE 9-1a. TTY INTERNAL CABLE P/N 89684200

CON-DUCTOR IDENT.	COLOR	ORIGIN (1)	DESTINATION (2)	REMARKS/ SIGNAL NAME
1	RED	P2A03	P1-24	GROUND
2		A08	13	$\overline{\text{BAUD SEL}}$
3		A13	23	$\overline{\text{M.I.}}$
4		B21	58	GROUND
5		A22	41	$\overline{\text{PAR.SEL}}$
6		A23	43	-12V
7		A24	45	-12V
8		A25	47	TTY-KB
9		A26	49	TTY-PR
10		A27	51	CRT-TRANS
11		A28	53	EVEN PARITY
12		A29	55	$\overline{\text{MOTOR ON}}$
13		A30	57	CRT-REC
14	RED	P2A31	P1-08	VCC

(1) Origin: 66-hole connector shell plug.
(2) Destination: 62-hole connector block.

TABLE 9-1b. TTY EXTERNAL SHIELDED CABLE P/N 89642300

CON-DUCTOR IDENT.	COLOR	ORIGIN (1)	DESTINATION (2)	REMARKS/ SIGNAL NAME
1	BLK	5	43	-12V
2	RED	7	45	-12V
3	GRN	6	47	TTY-KB
4	WHT	8	49	TTY-PR
5	BRN			NOT USED
6	BLU			NOT USED
7	ORN			NOT USED
8	YEL			NOT USED

(1) Origin: Molex type.
(2) Destination: Continental type.

TABLE 9-2. MEMORY EXPANSION BU120-A08 EXTERNAL CABLE ASSEMBLY (P1) AWG 28
PART NUMBER 89658101 (sheet 1 of 3)

CONDUCTOR IDENTITY	COLOR	ORIGIN (1)	DESTINATION (2)	REMARKS/SIGNAL NAME	
				SLOT 31	SLOT 33
1	GRN-WHT	GND	GND		
2	BLK	P1B01	P1B01	MX0L	SD1
3	GRN-WHT	GND	GND		
4	GRN-WHT	GND	GND		
5	BRN	P1B02	P1B02	MX1L	SA2
6	GRN-WHT	GND	GND		
7	GRN-WHT	GND	GND		
8	RED	P1B04	P1B04	MX2L	SD0
9	GRN-WHT	GND	GND		
10	GRN-WHT	GND	GND		
11	ORN	P1B06	P1B06	MX3L	SD2
12	GRN-WHT	GND	GND		
13	GRN-WHT	GND	GND		
14	YEL	P1B08	P1B08	MX4L	SD3
15	GRN-WHT	GND	GND		
16	GRN-WHT	GND	GND		
17	GRN	P1B09	P1B09	MX5L	SD7
18	GRN-WHT	GND	GND		
19	GRN-WHT	GND	GND		
20	BLU	P1A10	P1A10	ALU3L	SA3
21	GRN-WHT	GND	GND		
22	GRN-WHT	GND	GND		
23	VIO	P1B10	P1B10	ALU2L	SD6
24	GRN-WHT	GND	GND		
25	GRN-WHT	GND	GND		
26	GRA	P1A11	P1A11	ALU1L	SD5
27	GRN-WHT	GND	GND		
28	GRN-WHT	GND	GND		
29	WHT	P1A12	P1A12	ALU0L	SD4
30	GRN-WHT	GND	GND		

Numbers enclosed in parentheses indicate notes. See sheet 3.

TABLE 9-2. MEMORY EXPANSION BU120-A08 EXTERNAL CABLE ASSEMBLY (P1) AWG 28 PART NUMBER 89658101 (sheet 2 of 3)

CONDUCTOR IDENTITY	COLOR	ORIGIN (1)	DESTINATION (2)	REMARKS/SIGNAL NAME	
				SLOT 31	SLOT 33
31	GRN-WHT	GND	GND		
32	BLK	P1B12	P1B12	MX6L	SA5
33	GRN-WHT	GND	GND		
34	GRN-WHT	GND	GND		
35	BRN	P1A13	P1A13	MX7L	SA4
36	GRN-WHT	GND	GND		
37	GRN-WHT	GND	GND		
38	RED	P1B13	P1B13	MX0M	$\overline{\text{SPBM}}$
39	GRN-WHT	GND	GND		
40	GRN-WHT	GND	GND		
41	ORN	P1B14	P1B14	MX1M	$\overline{\text{CPBM}}$
42	GRN-WHT	GND	GND		
43	GRN-WHT	GND	GND		
44	YEL	P1B15	P1B15	MX2M	SD8
45	GRN-WHT	GND	GND		
46	GRN-WHT	GND	GND		
47	GRN	P1A16	P1A16	MX3M	SD11
48	GRN-WHT	GND	GND		
49	GRN-WHT	GND	GND		
50	BLU	P1B17	P1B17	MX7M	SD9
51	GRN-WHT	GND	GND		
52	GRN-WHT	GND	GND		
53	VIO	P1B18	P1B18	MX4M	SD14
54	GRN-WHT	GND	GND		
55	GRN-WHT	GND	GND		
56	GRA	P1B21	P1B21	MX6M	SD13
57	GRN-WHT	GND	GND		
58	GRN-WHT	GND	GND		
59	WHT	P1A22	P1A22	MX5M	SD10
60	GRN-WHT	GND	GND		

Numbers enclosed in parentheses indicate notes. See sheet 3.

TABLE 9-2. MEMORY EXPANSION BU120-A08 EXTERNAL CABLE ASSEMBLY (P1) AWG 28
PART NUMBER 89658101 (sheet 3 of 3)

CONDUCTOR IDENTITY	COLOR	ORIGIN (1)	DESTINATION (2)	REMARKS/SIGNAL NAME	
				SLOT 31	SLOT 33
61	GRN-WHT	GND	GND		
62	BLK	P1B22	P1B22	ALU1M	SA6
63	GRN-WHT	GND	GND		
64	GRN-WHT	GND	GND		
65	BRN	P1A23	P1A23	ALU2M	SA11
66	GRN-WHT	GND	GND		
67	GRN-WHT	GND	GND		
68	RED	P1B23	P1B23	ALU0M	$\overline{CRI}$
69	GRN-WHT	GND	GND		

(1) Origin: 62-contact connector

(2) Destination: 62-contact connector

TABLE 9-3. MEMORY EXPANSION BU120-A08 EXTERNAL CABLE ASSEMBLY (P2) AWG 28 PART NUMBER 89658501 (sheet 1 of 3)

CONDUCTOR IDENTITY	COLOR	ORIGIN (1)	DESTINATION (2)	REMARKS/SIGNAL NAME	
				SLOT 31	SLOT 33
1	GRN-WHT	GND	GND		
2	BLK	P2B02	P2B02	ALU3M	SD12
3	GRN-WHT	GND	GND		
4	GRN-WHT	GND	GND		
5	BRN	P2B03	P2B03	MX17	SA7
6	GRN-WHT	GND	GND		
7	GRN-WHT	GND	GND		
8	RED	P2B04	P2B04	MPRY	SD15
9	GRN-WHT	GND	GND		
10	GRN-WHT	GND	GND		
11	ORN	P2B05	P2B05	$\overline{\text{CVIOT}}$	SA10
12	GRN-WHT	GND	GND		
13	GRN-WHT	GND	GND		
14	YEL	P2B06	P2B06	$\overline{\text{WE}}$	SA12
15	GRN-WHT	GND	GND		
16	GRN-WHT	GND	GND		
17	GRN	P2A09	P2A09	$\overline{\text{PRTM}}$	SA9
18	GRN-WHT	GND	GND		
19	GRN-WHT	GND	GND		
20	BLU	P2B09	P2B09	$\overline{\text{CPEC}}$	SA14
21	GRN-WHT	GND	GND		
22	GRN-WHT	GND	GND		
23	VIO	P2A10	P2A10	$\overline{\text{SPI}}$	SA8
24	GRN-WHT	GND	GND		
25	GRN-WHT	GND	GND		
26	GRA	P2B10	P2B10	$\overline{\text{S WRITE}}$	SA13
27	GRN-WHT	GND	GND		
28	GRN-WHT	GND	GND		
29	WHT	P2A11	P2A11	CRQ	$\overline{\text{EDX}}$
30	GRN-WHT	GND	GND		

Numbers inside parentheses insicate notes. See sheet 3.

TABLE 9-3. MEMORY EXPANSION BU120-A08 EXTERNAL CABLE ASSEMBLY (P2) AWG 28 PART NUMBER 89658501 (sheet 2 of 3)

CONDUCTOR IDENTITY	COLOR	ORIGIN (1)	DESTINATION (2)	REMARKS/SIGNAL NAME	
				SLOT 31	SLOT 33
31	GRN-WHT	GND	GND		
32	BLK	P2B11	P2B11	$\overline{\text{CCPE}}$	GOM2
33	GRN-WHT	GND	GND		
34	GRN-WHT	GND	GND		
35	BRN	P2A12	P2A12		SA15
36	GRN-WHT	GND	GND		
37	GRN-WHT	GND	GND		
38	RED	P2B12	P2B12	ALU7L	PRTSW
39	GRN-WHT	GND	GND		
40	GRN-WHT	GND	GND		
41	ORN	P2A13	P2A13	ALU5M	32KW
42	GRN-WHT	GND	GND		
43	GRN-WHT	GND	GND		
44	YEL	P2B13	P2B13	ALU6L	NORMAL
45	GRN-WHT	GND	GND		
46	GRN-WHT	GND	GND		
47	GRN	P2B14	P2B14	ALU7M	$\overline{\text{MSXA}}$
48	GRN-WHT	GND	GND		
49	GRN-WHT	GND	GND		
50	BLU	P2B15	P2B15	ALU5L	SD17
51	GRN-WHT	GND	GND		
52	GRN-WHT	GND	GND		
53	VIO	P2B16	P2B16	ALU4M	$\overline{\text{SRSM}}$
54	GRN-WHT	GND	GND		
55	GRN-WHT	GND	GND		
56	GRA	P2B17	P2B17	ALU6M	$\overline{\text{SS}}$
57	GRN-WHT	GND	GND		
58	GRN-WHT	GND	GND		
59	WHT	P2A18	P2A18	ALU4L	SD16
60	GRN-WHT	GND	GND		

Numbers inside parentheses indicate notes. See sheet 3.

TABLE 9-3. MEMORY EXPANSION BU120-A08 EXTERNAL CABLE ASSEMBLY (P2) AWG 28 PART NUMBER 89658501 (sheet 3 of 3)

CONDUCTOR IDENTITY	COLOR	ORIGIN (1)	DESTINATION (2)	REMARKS/SIGNAL NAME	
				SLOT 31	SLOT 33
61	GRN-WHT	GND	GND		
62	BLK	P2B18	P2B18	DFEO	$\overline{\text{SVIO}}$
63	GRN-WHT	GND	GND		
64	GRN-WHT	GND	GND		
65	BRN	P2A19	P2A19	MDEL	SAO
66	GRN-WHT	GND	GND		
67	GRN-WHT	GND	GND		
68	RED	P2B19	P2B19		SA1
69	GRN-WHT	GND	GND		
70	GRN-WHT	GND	GND		
71	ORN	P2B20	P2B20	$\overline{\text{GPEC}}$	$\overline{\text{SRQ}}$
72	GRN-WHT	GND	GND		
73	GRN-WHT	GND	GND		
74	YEL	P2A22	P2A22	$\overline{\text{PEL}}$	RGPWR
75	GRN-WHT	GND	GND		

(1) Origin: 62-contact connector

(2) Destination: 62-contact connector

TABLE 9-4.a WIRE LIST AB 107/AB 108 BACKPLANE
(in signal name order)

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
20P2A23	20P2A24	-12V	89879100	1	1
10P2A25	08P2A01	A NOENV(1)	89879100	2	2
10P1A24	08P1A31	A POSTAMBLE	89879100	2	2
10P2B07	08P1B30	A POSTAMBLE	89879100	1	1
10P2B30	08P2A11	A READY F	89879100	1	1
10P2A04	08P2B11	A READY G	89879100	2	2
10P2B06	08P2B08	A.SKEWCVF F	89879100	1	1
10P1B26	08P2A07	A.SKEWCVF G	89879100	2	2
13P2B13	12P1B06	A/D	89879100	2	2
14P2B12	13P2B13	A/D	89879100	1	1
12P1B06	11P1B31	A/D	89879100	1	1
16P1B31	15P2A18	A/Q CLEAR	89879100	2	2
14P1B17	13P1A13	A=B	89879100	2	2
09P2A06	08P1A11	AB CLOCKOUT	89879100	2	2
10P2A06	09P2A06	AB CLOCKOUT	89879100	1	1
10P2A26	09P2A26	AB DATA	89879100	1	1
09P2A26	08P1A19	AB DATA	89879100	2	2
10P1A04	09P1A04	AB DEN	89879100	2	2
09P1A04	08P2A16	AB DEN	89879100	1	1
10P1A28	09P1A28	AB DOT	89879100	1	1
09P1A28	08P1B29	AB DOT	89879100	2	2
10P1A11	09P1A11	AB LOZ	89879100	2	2
09P1A11	08P1A22	AB LOZ	89879100	1	1
09P2A13	08P2B06	AB PARITY	89879100	1	1
10P2A13	09P2A13	AB PARITY	89879100	2	2
09P1A18	08P2A09	AB PRESET	89879100	2	2
10P1A18	09P1A18	AB PRESET	89879100	1	1
10P1B30	09P1B30	AB RENABLE*	89879100	1	1
09P1B30	08P1A14	AB RENABLE*	89879100	2	2
09P2A22	08P1A12	AB TOG	89879100	2	2
10P2A22	09P2A22	AB TOG	89879100	1	1
10P1A17	09P1A17	ABONE	89879100	1	1
09P1A17	08P1A06	ABONE	89879100	2	2
10P2B09	09P2B09	ABWRES(5)	89879100	2	2
09P2B09	08P1B12	ABWRES(5)	89879100	1	1
29P2B26	28P2B19	ACA5	89879100	2	2
34P2B26	35P2B26	ACA5	89879101	2	2
32P2B26	33P2B26	ACA5	89879101	2	2
30P2B26	31P2B26	ACA5	89879101	2	2
35P2B26	36P2B26	ACA5	89879101	1	1
33P2B26	34P2B26	ACA5	89879101	1	1
31P2B26	32P2B26	ACA5	89879101	1	1
29P2B26	30P2B26	ACA5	89879101	1	1
29P2B23	30P2B23	ACA6	89879101	1	1
33P2B23	34P2B23	ACA6	89879101	1	1
31P2B23	32P2B23	ACA6	89879101	1	1
35P2B23	36P2B23	ACA6	89879101	1	1
32P2B23	33P2B23	ACA6	89879101	2	2
30P2B23	31P2B23	ACA6	89879101	2	2
34P2B23	35P2B23	ACA6	89879101	2	2
29P2B23	28P2B17	ACA6	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
28P2B24	29P2A23	ACA7	89879100	2	2
30P2A23	31P2A23	ACA7	89879101	2	2
34P2A23	35P2A23	ACA7	89879101	2	2
32P2A23	33P2A23	ACA7	89879101	2	2
29P2A23	30P2A23	ACA7	89879101	1	1
33P2A23	34P2A23	ACA7	89879101	1	1
31P2A23	32P2A23	ACA7	89879101	1	1
35P2A23	36P2A23	ACA7	89879101	1	1
29P2B22	30P2B22	ACA8	89879101	1	1
33P2B22	34P2B22	ACA8	89879101	1	1
31P2B22	32P2B22	ACA8	89879101	1	1
35P2B22	36P2B22	ACA8	89879101	1	1
34P2B22	35P2B22	ACA8	89879101	2	2
32P2B22	33P2B22	ACA8	89879101	2	2
30P2B22	31P2B22	ACA8	89879101	2	2
29P2B22	28P2A18	ACA8	89879100	2	2
29P2A27	28P2B20	ACA9	89879100	2	2
30P2A27	31P2A27	ACA9	89879101	2	2
34P2A27	35P2A27	ACA9	89879101	2	2
32P2A27	33P2A27	ACA9	89879101	2	2
29P2A27	30P2A27	ACA9	89879101	1	1
35P2A27	36P2A27	ACA9	89879101	1	1
33P2A27	34P2A27	ACA9	89879101	1	1
31P2A27	32P2A27	ACA9	89879101	1	1
10P2B02	08P2A17	AC1*	89879100	2	2
10P2A02	08P2A15	AC2	89879100	1	1
19P1B09	15P2A29	ADDR ERR	89879100	1	1
19P1A05	17P2A18	ADDR.CKWD=0	89879100	2	2
16P1B22	15P2B30	ADDR.ERR*	89879100	1	1
19P2B25	16P1B24	ADDRESS ECP	89879100	1	1
19P2B30	17P2B24	ADDRESS 12*	89879100	1	1
19P2B16	17P2A05	ADDRESS*	89879100	1	1
19P2B17	18P1B30	ADDT INDEX*	89879100	2	2
26P2A14	22P2B28	ADD7M	89879100	1	1
22P2B22	23P1A31	ADR*	89879100	1	1
23P1A31	24P1B07	ADR*	89879100	2	2
28P2B14	27P2B25	ADVANCE*	89879100	2	2
24P2B07	23P1A24	ADY*	89879100	1	1
24P1B24	23P1A16	AD1	89879100	1	1
24P1A26	23P1B20	AD2	89879100	2	2
10P2A24	08P2B05	AENV(1)	89879100	1	1
10P2A09	08P2A02	AENV(2)	89879100	2	2
10P1B03	08P2A04	AENV(4)	89879100	1	1
10P1A26	08P1B26	AENV(5)	89879100	2	2
25P1B16	21P1B26	AL	89879100	2	2
25P1B19	23P1B14	ALCK	89879100	1	1
25P2A09	25P2B11	ALUCAM	89879100	2	2
26P1A27	25P2A09	ALUCAM	89879100	1	1
28P1B12	25P1B24	ALUCL	89879100	2	2
28P1A28	26P1B24	ALUCM	89879100	2	2
31P1A12	28P1B12	ALUCL	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
31P1B23	28P1A28	ALU0M	89879100	1	1
31P1A11	28P1A11	ALU1L	89879100	1	1
28P1A11	25P1B30	ALU1L	89879100	2	2
28P1A22	26P1B30	ALU1M	89879100	2	2
31P1B22	28P1A22	ALU1M	89879100	1	1
31P1B10	28P1B10	ALU2L	89879100	1	1
28P1B10	25P1B27	ALU2L	89879100	2	2
28P1A27	26P1B27	ALU2M	89879100	2	2
31P1A23	28P1A27	ALU2M	89879100	1	1
31P1A10	28P1A10	ALU3L	89879100	1	1
28P1A10	25P1A21	ALU3L	89879100	2	2
28P1B28	26P1A21	ALU3M	89879100	2	2
31P2B02	28P1B28	ALU3M	89879100	1	1
31P2A18	28P2A17	ALU4L	89879100	1	1
28P2A17	25P2B17	ALU4L	89879100	2	2
28P2A16	26P2B17	ALU4M	89879100	2	2
31P2B16	28P2A16	ALU4M	89879100	1	1
31P2B15	28P2A15	ALU5L	89879100	1	1
28P2A15	25P2A16	ALU5L	89879100	2	2
28P2B09	26P2A16	ALU5M	89879100	2	2
31P2A13	28P2B09	ALU5M	89879100	1	1
31P2B13	28P2A12	ALU6L	89879100	1	1
28P2A12	25P2A15	ALU6L	89879100	2	2
28P2B16	26P2A15	ALU6M	89879100	2	2
31P2B17	28P2B16	ALU6M	89879100	1	1
26P2A04	25P2B02	ALU7AL	89879100	1	1
26P2A04	26P2B05	ALU7AL	89879100	2	2
26P2B02	25P2A04	ALU7AM	89879100	1	1
25P2A04	22P2A29	ALU7AM	89879104		
31P2B12	28P2A09	ALU7L	89879100	1	1
28P2A09	25P2B15	ALU7L	89879100	2	2
28P2B13	26P2B15	ALU7M	89879100	2	2
31P2B14	28P2B13	ALU7M	89879100	1	1
13P2B22	12P1B16	AL1	89879100	2	2
13P2A21	08P2A24	AL2	89879100	2	2
26P1B16	21P1A26	AM	89879100	1	1
26P1B19	23P2A11	AMCK	89879100	2	2
10P1A07	08P2A12	ANODROPOUT(	89879100	1	1
10P2A10	08P1A23	ANOENV(2)	89879100	1	1
10P1A16	08P1B25	ANOENV(3)	89879100	2	2
10P1A03	08P2B04	ANOENV(4)	89879100	1	1
10P1B25	08P1B27	ANOENV(5)	89879100	2	2
25P2A27	24P2A02	AO*	89879100	2	2
10P2A29	08P2B19	AONEF*	89879100	2	2
10P2B05	08P2A19	AONEG*	89879100	1	1
25P2A30	22P1A21	AQC*	89879100	2	2
26P2A30	25P2A30	AQC*	89879100	1	1
28P2B15	29P2A25	ARA0	89879100	2	2
33P2A25	34P2A25	ARA0	89879101	1	1
31P2A25	32P2A25	ARA0	89879101	1	1
29P2A25	30P2A25	ARA0	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
35P2A25	36P2A25	ARA0	89879101	1	1
34P2A25	35P2A25	ARA0	89879101	2	2
32P2A25	33P2A25	ARA0	89879101	2	2
30P2A25	31P2A25	ARA0	89879101	2	2
30P2A29	31P2A29	ARA1	89879101	2	2
34P2A29	35P2A29	ARA1	89879101	2	2
32P2A29	33P2A29	ARA1	89879101	2	2
29P2A29	30P2A29	ARA1	89879101	1	1
33P2A29	34P2A29	ARA1	89879101	1	1
31P2A29	32P2A29	ARA1	89879101	1	1
35P2A29	36P2A29	ARA1	89879101	1	1
28P2B22	29P2A29	ARA1	89879100	2	2
29P2A28	28P2A23	ARA2	89879100	2	2
29P2A28	30P2A28	ARA2	89879101	1	1
33P2A28	34P2A28	ARA2	89879101	1	1
31P2A28	32P2A28	ARA2	89879101	1	1
35P2A28	36P2A28	ARA2	89879101	1	1
32P2A28	33P2A28	ARA2	89879101	2	2
30P2A28	31P2A28	ARA2	89879101	2	2
34P2A28	35P2A28	ARA2	89879101	2	2
30P2B25	31P2B25	ARA3	89879101	2	2
34P2B25	35P2B25	ARA3	89879101	2	2
32P2B25	33P2B25	ARA3	89879101	2	2
31P2B25	32P2B25	ARA3	89879101	1	1
33P2B25	34P2B25	ARA3	89879101	1	1
29P2B25	30P2B25	ARA3	89879101	1	1
35P2B25	36P2B25	ARA3	89879101	1	1
28P2A21	29P2B25	ARA3	89879100	2	2
28P2B23	29P2B28	ARA4	89879100	2	2
29P2B28	30P2B28	ARA4	89879101	1	1
33P2B28	34P2B28	ARA4	89879101	1	1
31P2B28	32P2B28	ARA4	89879101	1	1
35P2B28	36P2B28	ARA4	89879101	1	1
34P2B28	35P2B28	ARA4	89879101	2	2
32P2B28	33P2B28	ARA4	89879101	2	2
30P2B28	31P2B28	ARA4	89879101	2	2
19P2B04	18P1A14	ARCUR CWA*	89879100	2	2
18P2B07	16P2B02	ARCUR-CA*	89879100	1	1
08P2B13	10P2A11	ASYNC(2)	89879104		
10P1A27	08P2A13	ASYNC(4)	89879100	1	1
26P2A21	25P2A21	ATAUG	89879100	2	2
25P2A21	24P2A24	ATAUG	89879100	1	1
26P2B08	22P2A28	AUG7M	89879100	2	2
10P1B20	05P1B18	AUTOLOAD	89879100	2	2
16P2B08	10P1B20	AUTOLOAD	89879100	1	1
20P1A01	10P1B19	AUTOLOAD	89879100	1	1
04P1B18	05P1B18	AUTOLOAD	89879102	2	1
03P1B18	04P1B18	AUTOLOAD	89879102	1	1
10P1B19	05P1B18	AUTOLOAD	89879100	3	3
17P1B29	16P2B05	AUTOLOAD2*	89879100	1	1
19P2B12	17P1B29	AUTOLOAD2*	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
21P2A08	20P1A09	AUTRSW*	89879100	1	1
10P2A05	08P1A17	AWRES(1-4)	89879100	1	1
18P1A25	17P2A04	A0	89879100	1	1
17P2A04	15P2A14	A0	89879100	2	2
16P1B21	15P2A28	A0AF+MC*	89879100	2	2
19P2B03	17P1B09	A0AF+MC*	89879100	2	2
17P1B09	16P1B21	A0AF+MC*	89879100	1	1
17P2B03	15P2B15	A1	89879100	1	1
19P2A10	18P1B29	A1	89879100	1	1
18P1B29	17P2B03	A1	89879100	2	2
17P2A21	15P2A16	A10	89879100	2	2
18P1B20	17P2A21	A10	89879100	1	1
18P1B24	17P2B20	A11	89879100	1	1
17P2B20	15P2A13	A11	89879100	2	2
17P2B19	15P2B13	A12	89879100	2	2
18P1A30	17P2B19	A12	89879100	1	1
18P1A28	17P2A17	A13	89879100	1	1
17P2A17	15P2A12	A13	89879100	2	2
17P2A16	15P2B12	A14	89879100	2	2
18P1B27	17P2A16	A14	89879100	1	1
18P1B13	17P2A15	A15	89879100	1	1
17P2A15	15P2B14	A15	89879100	2	2
17P2B02	15P2A22	A2	89879100	2	2
19P2A19	18P1A26	A2	89879100	2	2
18P1A26	17P2B02	A2	89879100	1	1
19P2B28	18P1B26	A3	89879100	1	1
17P2A06	15P2A23	A3	89879100	1	1
18P1B26	17P2A06	A3	89879100	2	2
19P2A27	18P1A23	A4	89879100	2	2
17P2B12	15P2B17	A4	89879100	2	2
18P1A23	17P2B12	A4	89879100	1	1
18P1B18	17P2A10	A5	89879100	1	1
18P1A24	17P2A09	A6	89879100	2	2
17P2A08	15P2B16	A7	89879100	2	2
13P1A18	12P2B07	A7	89879100	2	2
18P1B19	17P2A08	A7	89879100	1	1
14P2B08	12P2B07	A7	89879100	1	1
21P1B08	22P2A20	A7M	89879100	2	2
22P2A20	26P2B23	A7M	89879100	1	1
18P1B23	17P2B14	A8	89879100	1	1
17P2B14	15P2B05	A8	89879100	2	2
17P2B13	15P2A15	A9	89879100	2	2
18P1A20	17P2B13	A9	89879100	1	1
27P2B12	28P2B08	B	89879100	1	1
09P2A25	08P1A30	B NOENV(1)	89879100	2	2
09P2A10	08P2B03	B NOENV(2)	89879100	2	2
09P1A16	08P2B02	B NOENV(3)	89879100	2	2
09P1A03	08P2B01	B NOENV(4)	89879100	2	2
09P2B07	08P1B31	B POSTABLEF	89879100	2	2
09P2B30	08P2A10	B READY F	89879100	2	2
09P2B06	08P2B07	B SKEWOVF F	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
09P2A05	08P1A28	B WRES(1-4)	89879100	2	2
24P1B25	22P2A27	BB	89879100	1	1
24P1A22	23P1B30	BBCK	89879100	2	2
13P2A14	11P1A17	BCD	89879100	2	2
09P2B02	08P2B17	BC1*	89879100	2	2
09P2A02	08P2B15	BC2	89879100	2	2
21P2B31	20P1A07	BEA	89879100	1	1
21P2A30	20P1B26	BEAC	89879100	1	1
18P1A13	17P1A30	BL-BORROW*	89879100	1	1
18P1A27	17P1B17	BL-LOAD*	89879100	2	2
18P2A07	16P1A23	BL>CYL	89879100	2	2
17P1A14	16P1A08	BL=0	89879100	1	1
15P1A31	16P1A08	BL=0	89879104		
09P2A29	08P2B20	BCNEF*	89879100	2	2
14P2B19	13P2B01	BOT	89879100	1	1
28P2B29	27P2B22	BRWRA*	89879100	1	1
09P2A01	08P2B14	BS1*	89879100	2	2
14P1B14	13P1B14	BUF I/O*	89879100	1	1
13P1B14	12P1B20	BUF I/O*	89879100	2	2
17P1B15	16P1A16	BUFF1-BUFF2	89879100	2	2
18P2B23	16P1A15	BUFF1BUFF2*	89879100	1	1
17P1B18	16P1B15	BUFF2 FULL*	89879100	1	1
12P1B09	08P1A15	BUFF2FL*WMO	89879100	1	1
14P2A07	12P2B10	BUSY	89879100	1	1
13P1B28	12P2B10	BUSY	89879100	2	2
19P2A30	15P2A07	BUSY RR*	89879100	1	1
24P2A28	22P2B27	BX15	89879100	2	2
28P1B19	27P1A25	CAA15	89879100	1	1
19P1A31	18P1A15	CACWA0	89879100	2	2
19P2A04	18P1B14	CACWA1	89879100	1	1
19P1B13	18P1A12	CACWA10	89879100	2	2
19P1A12	18P1B12	CACWA11	89879100	1	1
19P1A11	18P1A16	CACWA12	89879100	2	2
19P1A08	18P1B15	CACWA13	89879100	1	1
19P1A06	18P1B17	CACWA14	89879100	2	2
19P1B04	18P1A18	CACWA15	89879100	1	1
19P1B21	18P1B16	CACWA2	89879100	2	2
19P1B20	18P1A17	CACWA3	89879100	1	1
19P1A21	18P1A21	CACWA4	89879100	2	2
19P1B19	18P1B21	CACWA5	89879100	1	1
19P1A18	18P1A22	CACWA6	89879100	2	2
19P1B15	18P1B22	CACWA7	89879100	1	1
19P1B14	18P1B10	CACWA8	89879100	2	2
19P1B10	18P1A10	CACWA9	89879100	1	1
17P1B10	16P1A09	CAL-SHIFT*	89879100	2	2
14P1A17	13P1B17	CARCURAD*	89879100	2	2
19P2B05	18P2A06	CARST*	89879100	1	1
17P1A24	16P1B13	CAU SHIFT*	89879100	1	1
19P2A29	17P1A24	CAU SHIFT*	89879100	2	2
18P2B09	16P2B25	CA1J*	89879100	1	1
18P2B11	16P2B27	CA12*	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
18P2A08	16P2B20	CA13*	89879100	1	1
18P2A10	16P2B28	CA15*	89879100	1	1
18P2B08	16P2B31	CA16*	89879100	1	1
18P2A05	16P2B29	CA17*	89879100	1	1
18P2A01	16P2B30	CA18*	89879100	1	1
18P2A04	16P2B14	CA19*	89879100	1	1
18P1A05	16P2B15	CA20*	89879100	1	1
18P2A22	15P2A08	CA6	89879100	2	2
18P2B06	15P2A17	CA65M*	89879100	2	2
18P2B06	16P2B19	CA65M*	89879100	1	1
18P2A09	16P2B18	CA7*	89879100	1	1
27P2A10	30P1B23	CCPE*	89879100	2	2
30P1B23	20P1A28	CCPE*	89879100	1	1
31P2B11	27P2A10	CCPE*	89879100	1	1
35P2A26	36P2A26	CE*	89879101	1	1
33P2A26	34P2A26	CE*	89879101	1	1
31P2A26	32P2A26	CE*	89879101	1	1
29P2A26	30P2A26	CE*	89879101	1	1
32P2A26	33P2A26	CE*	89879101	2	2
30P2A26	31P2A26	CE*	89879101	2	2
34P2A26	35P2A26	CE*	89879101	2	2
27P2B27	29P2A26	CE*	89879100	2	2
15P1B07	12P1B21	CHI*	89879100	1	1
23P2B31	20P2B25	CHI*	89879100	1	1
20P2B25	15P1B07	CHI*	89879100	2	2
12P1B21	07P1B07	CHI*	89879100	2	2
02P1B07	06P1B07	CHI*	89879103	2	2
06P1B07	07P1B07	CHI*	89879103	1	1
01P1B07	02P1B07	CHI*	89879103	1	1
26P1A03	25P1B01	CI	89879100	2	2
19P1B29	17P1B06	CKWD SHIFT	89879100	2	2
19P2A05	17P1B24	CKWD11	89879100	2	2
19P2A13	17P1A18	CLEAR CKWD*	89879100	1	1
19P2B06	16P2B05	CLEAR CONTR	89879100	1	1
18P2B17	17P1B22	CLEAR-SHIFT	89879100	1	1
13P2A02	12P1A05	CLR LOWER*	89879100	2	2
26P1A28	25P1A28	CLREG*	89879100	2	2
25P1A28	20P1B07	CLREG*	89879100	1	1
23P2A15	21P2B12	CLREQ	89879100	2	2
23P1A23	24P1A31	CLRIR	89879100	2	2
21P2B10	23P1A23	CLRIR	89879100	1	1
22P1B07	25P1A13	CLRQ*	89879100	1	1
25P1A13	26P1A13	CLRQ*	89879100	2	2
26P1B20	21P2A29	CLRXM	89879100	1	1
28P2A06	27P2B07	CMDR*	89879100	2	2
25P1B31	20P1B17	CNSOL*	89879100	1	1
26P1B31	20P1A14	CNSCM*	89879100	1	1
25P1A31	20P1B19	CNS1L*	89879100	1	1
26P1A31	20P1B15	CNS1M*	89879100	1	1
25P1B29	20P1A18	CNS2L*	89879100	1	1
26P1B29	20P1B14	CNS2M*	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
25P1B28	20P1A20	CNS3L*	89879100	1	1
26P1B28	20P1A15	CNS3M*	89879100	1	1
25P2B12	20P1A07	CNS4L*	89879100	1	1
26P2B12	20P1B03	CNS4M*	89879100	1	1
25P2A11	20P1A06	CNS5L*	89879100	1	1
26P2A11	20P1A03	CNS5M*	89879100	1	1
25P2B13	20P1B13	CNS6L*	89879100	1	1
26P2B13	20P1A04	CNS6M*	89879100	1	1
25P2B14	20P1A13	CNS7L*	89879100	1	1
26P2B14	20P1B05	CNS7M*	89879100	1	1
22P1A17	23P2A09	CNTE2*	89879100	1	1
23P2A09	24P2A30	CNTE2*	89879100	2	2
25P1B23	22P1A04	CO	89879100	2	2
26P1B23	25P1B23	CO	89879100	1	1
19P2A12	17P1B16	COMPARE	89879100	2	2
14P1A28	12P2A06	CONTACT	89879100	2	2
13P2A01	12P2A02	CONTACT*	89879100	2	2
28P1B13	22P1B17	CPBM*	89879100	2	2
33P1B14	28P1B13	CPBM*	89879100	1	1
31P2B09	27P1A31	CPEC*	89879100	1	1
12P1A31	11P2B30	CRCC STATE*	89879100	1	1
27P1B26	28P1B22	CRI*	89879100	2	2
33P1B23	28P1B22	CRI*	89879100	1	1
22P1A12	27P1B26	CRI*	89879100	1	1
23P1A03	24P1B26	CRQ	89879104		
31P2A11	27P2A09	CRQ	89879104		
24P1B26	27P2A09	CRQ	89879104		
25P1B03	23P1B19	CRQ*	89879100	1	1
21P1B25	20P2B05	CRQ*	89879100	1	1
26P1B03	25P1B03	CRQ*	89879100	2	2
23P1B19	21P1B25	CRQ*	89879100	2	2
24P2B20	20P1B27	CSA*	89879100	1	1
24P2A04	20P1B17	CSM*	89879100	1	1
24P1B03	20P1A25	CSP*	89879100	1	1
23P1A04	20P1B10	CSPR	89879100	1	1
24P2A10	20P1A27	CSQ*	89879100	1	1
22P1A31	20P1B31	CSX*	89879100	1	1
24P2A21	22P1A31	CSX*	89879100	2	2
23P1B29	20P1B29	CSY*	89879100	1	1
16P1A26	15P2B31	CTRLR BUSY	89879100	1	1
19P2A08	16P1A26	CTRLR BUSY	89879100	2	2
31P2B05	27P1A28	CVIO1*	89879100	1	1
27P1A28	21P2B04	CVIO1*	89879100	2	2
18P1B28	17P1A08	CWA-COUNT*	89879100	2	2
18P1B28	19P1B25	CWA-COUNT*	89879100	1	1
27P2B16	28P2B26	CXP*	89879100	1	1
22P1B09	25P2A10	C1	89879100	1	1
25P2A10	26P2A10	C1	89879100	2	2
25P1A01	22P1B01	C2	89879100	2	2
26P1A01	25P1A01	C2	89879100	1	1
22P1B04	25P2B31	C3	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
25P2B31	26P2B31	C3	89879100	2	2
19P1B17	17P1A10	D.NO.COMP.	89879100	1	1
18P2B13	17P1B14	DATA	89879100	2	2
13P2B14	12P1A03	DATA	89879100	2	2
24P1B21	21P1A06	DBB	89879100	1	1
27P2B17	28P2B18	DE*	89879100	1	1
24P1A14	22P1A15	DEL*	89879100	2	2
22P2B30	24P2B10	DELTAUG*	89879100	2	2
24P2B10	25P2B16	DELTAUG*	89879100	1	1
24P1A15	21P2A26	DEL2	89879100	1	1
19P2A24	15P2A05	DF-GATED	89879100	2	2
27P2B19	21P2B08	DFEO	89879100	2	2
21P2B08	23P1B01	DFEO	89879100	1	1
31P2B18	27P2B19	DFEO	89879100	1	1
29P1B03	28P1A02	DINO	89879100	2	2
32P1B03	33P1B03	DINO	89879101	2	2
30P1B03	31P1B03	DINO	89879101	2	2
34P1B03	35P1B03	DINO	89879101	2	2
35P1B03	36P1B03	DINO	89879101	1	1
33P1B03	34P1B03	DINO	89879101	1	1
31P1B03	32P1B03	DINO	89879101	1	1
29P1B03	30P1B03	DINO	89879101	1	1
29P1A03	30P1A03	DIN1	89879101	1	1
33P1A03	34P1A03	DIN1	89879101	1	1
31P1A03	32P1A03	DIN1	89879101	1	1
35P1A03	36P1A03	DIN1	89879101	1	1
30P1A03	31P1A03	DIN1	89879101	2	2
34P1A03	35P1A03	DIN1	89879101	2	2
32P1A03	33P1A03	DIN1	89879101	2	2
29P1A03	28P1B02	DIN1	89879100	2	2
29P1A28	28P1A17	DIN10	89879100	2	2
34P1A28	35P1A28	DIN10	89879101	2	2
32P1A28	33P1A28	DIN10	89879101	2	2
30P1A28	31P1A28	DIN10	89879101	2	2
35P1A28	36P1A28	DIN10	89879101	1	1
33P1A28	34P1A28	DIN10	89879101	1	1
31P1A28	32P1A28	DIN10	89879101	1	1
29P1A28	30P1A28	DIN10	89879101	1	1
29P1A27	30P1A27	DIN11	89879101	1	1
33P1A27	34P1A27	DIN11	89879101	1	1
31P1A27	32P1A27	DIN11	89879101	1	1
35P1A27	36P1A27	DIN11	89879101	1	1
30P1A27	31P1A27	DIN11	89879101	2	2
34P1A27	35P1A27	DIN11	89879101	2	2
32P1A27	33P1A27	DIN11	89879101	2	2
29P1A27	28P1B16	DIN11	89879100	2	2
28P1B24	29P1B25	DIN12	89879100	2	2
34P1B25	35P1B25	DIN12	89879101	2	2
32P1B25	33P1B25	DIN12	89879101	2	2
30P1B25	31P1B25	DIN12	89879101	2	2
29P1B25	30P1B25	DIN12	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
33P1B25	34P1B25	DIN12	89879101	1	1
31P1B25	32P1B25	DIN12	89879101	1	1
35P1B25	36P1B25	DIN12	89879101	1	1
29P1B27	30P1B27	DIN13	89879101	1	1
33P1B27	34P1B27	DIN13	89879101	1	1
31P1B27	32P1B27	DIN13	89879101	1	1
35P1B27	36P1B27	DIN13	89879101	1	1
30P1B27	31P1B27	DIN13	89879101	2	2
34P1B27	35P1B27	DIN13	89879101	2	2
32P1B27	33P1B27	DIN13	89879101	2	2
29P1B27	28P1B26	DIN13	89879100	2	2
29P1B28	28P1A25	DIN14	89879100	2	2
32P1B28	33P1B28	DIN14	89879101	2	2
30P1B28	31P1B28	DIN14	89879101	2	2
34P1B28	35P1B28	DIN14	89879101	2	2
29P1B28	30P1B28	DIN14	89879101	1	1
33P1B28	34P1B28	DIN14	89879101	1	1
31P1B28	32P1B28	DIN14	89879101	1	1
35P1B28	36P1B28	DIN14	89879101	1	1
29P1B26	30P1B26	DIN15	89879101	1	1
33P1B26	34P1B26	DIN15	89879101	1	1
31P1B26	32P1B26	DIN15	89879101	1	1
35P1B26	36P1B26	DIN15	89879101	1	1
30P1B26	31P1B26	DIN15	89879101	2	2
34P1B26	35P1B26	DIN15	89879101	2	2
32P1B26	33P1B26	DIN15	89879101	2	2
29P1B26	28P1B25	DIN15	89879100	2	2
28P2B12	29P2A04	DIN16	89879100	2	2
34P2A04	35P2A04	DIN16	89879101	2	2
32P2A04	33P2A04	DIN16	89879101	2	2
30P2A04	31P2A04	DIN16	89879101	2	2
35P2A04	36P2A04	DIN16	89879101	1	1
33P2A04	34P2A04	DIN16	89879101	1	1
31P2A04	32P2A04	DIN16	89879101	1	1
29P2A04	30P2A04	DIN16	89879101	1	1
35P2A05	36P2A05	DIN17	89879101	1	1
33P2A05	34P2A05	DIN17	89879101	1	1
31P2A05	32P2A05	DIN17	89879101	1	1
29P2A05	30P2A05	DIN17	89879101	1	1
30P2A05	31P2A05	DIN17	89879101	2	2
34P2A05	35P2A05	DIN17	89879101	2	2
32P2A05	33P2A05	DIN17	89879101	2	2
28P2A10	29P2A05	DIN17	89879100	2	2
29P1A05	28P1A04	DIN2	89879100	2	2
32P1A05	33P1A05	DIN2	89879101	2	2
30P1A05	31P1A05	DIN2	89879101	2	2
34P1A05	35P1A05	DIN2	89879101	2	2
29P1A05	30P1A05	DIN2	89879101	1	1
33P1A05	34P1A05	DIN2	89879101	1	1
31P1A05	32P1A05	DIN2	89879101	1	1
35P1A05	36P1A05	DIN2	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
29P1B07	30P1B07	DIN3	89879101	1	1
33P1B07	34P1B07	DIN3	89879101	1	1
31P1B07	32P1B07	DIN3	89879101	1	1
35P1B07	36P1B07	DIN3	89879101	1	1
30P1B07	31P1B07	DIN3	89879101	2	2
34P1B07	35P1B07	DIN3	89879101	2	2
32P1B07	33P1B07	DIN3	89879101	2	2
29P1B07	28P1A03	DIN3	89879100	2	2
29P1A07	28P1A08	DIN4	89879100	2	2
34P1A07	35P1A07	DIN4	89879101	2	2
32P1A07	33P1A07	DIN4	89879101	2	2
30P1A07	31P1A07	DIN4	89879101	2	2
29P1A07	30P1A07	DIN4	89879101	1	1
33P1A07	34P1A07	DIN4	89879101	1	1
31P1A07	32P1A07	DIN4	89879101	1	1
35P1A07	36P1A07	DIN4	89879101	1	1
29P1B16	30P1B16	DIN5	89879101	1	1
33P1B16	34P1B16	DIN5	89879101	1	1
31P1B16	32P1B16	DIN5	89879101	1	1
35P1B16	36P1B16	DIN5	89879101	1	1
30P1B16	31P1B16	DIN5	89879101	2	2
34P1B16	35P1B16	DIN5	89879101	2	2
32P1B16	33P1B16	DIN5	89879101	2	2
29P1B16	28P1A07	DIN5	89879100	2	2
29P1A15	28P1A16	DIN6	89879100	2	2
32P1A15	33P1A15	DIN6	89879101	2	2
30P1A15	31P1A15	DIN6	89879101	2	2
34P1A15	35P1A15	DIN6	89879101	2	2
29P1A15	30P1A15	DIN6	89879101	1	1
33P1A15	34P1A15	DIN6	89879101	1	1
31P1A15	32P1A15	DIN6	89879101	1	1
35P1A15	36P1A15	DIN6	89879101	1	1
29P1A18	30P1A18	DIN7	89879101	1	1
33P1A18	34P1A18	DIN7	89879101	1	1
31P1A18	32P1A18	DIN7	89879101	1	1
35P1A18	36P1A18	DIN7	89879101	1	1
30P1A18	31P1A18	DIN7	89879101	2	2
34P1A18	35P1A18	DIN7	89879101	2	2
32P1A18	33P1A18	DIN7	89879101	2	2
29P1A18	28P1B17	DIN7	89879100	2	2
29P1B19	28P1A14	DIN8	89879100	2	2
34P1B19	35P1B19	DIN8	89879101	2	2
32P1B19	33P1B19	DIN8	89879101	2	2
30P1B19	31P1B19	DIN8	89879101	2	2
29P1B19	30P1B19	DIN8	89879101	1	1
33P1B19	34P1B19	DIN8	89879101	1	1
31P1B19	32P1B19	DIN8	89879101	1	1
35P1B19	36P1B19	DIN8	89879101	1	1
29P1B20	30P1B20	DIN9	89879101	1	1
33P1B20	34P1B20	DIN9	89879101	1	1
31P1B20	32P1B20	DIN9	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
35P1B20	36P1B20	DIN9	89879101	1	1
30P1B20	31P1B20	DIN9	89879101	2	2
34P1B20	35P1B20	DIN9	89879101	2	2
32P1B20	33P1B20	DIN9	89879101	2	2
29P1B20	28P1A18	DIN9	89879100	2	2
27P2B10	29P2A21	DISABLE	89879100	2	2
30P2A21	31P2A21	DISABLE	89879101	2	2
34P2A21	35P2A21	DISABLE	89879101	2	2
32P2A21	33P2A21	DISABLE	89879101	2	2
35P2A21	36P2A21	DISABLE	89879101	1	1
33P2A21	34P2A21	DISABLE	89879101	1	1
31P2A21	32P2A21	DISABLE	89879101	1	1
29P2A21	30P2A21	DISABLE	89879101	1	1
19P2B08	18P1B31	DOF	89879100	1	1
18P1B31	17P1A16	DOF	89879100	2	2
19P2A09	17P1A15	DOF-LA	89879100	1	1
19P1B30	16P1A28	DOF-LA-AUTO	89879100	2	2
27P1B01	29P1A02	DOUT0	89879100	2	2
29P1A02	30P1A02	DOUT0	89879101	1	1
33P1A02	34P1A02	DOUT0	89879101	1	1
31P1A02	32P1A02	DOUT0	89879101	1	1
35P1A02	36P1A02	DOUT0	89879101	1	1
34P1A02	35P1A02	DOUT0	89879101	2	2
32P1A02	33P1A02	DOUT0	89879101	2	2
30P1A02	31P1A02	DOUT0	89879101	2	2
30P1A04	31P1A04	DOUT1	89879101	2	2
34P1A04	35P1A04	DOUT1	89879101	2	2
32P1A04	33P1A04	DOUT1	89879101	2	2
29P1A04	30P1A04	DOUT1	89879101	1	1
33P1A04	34P1A04	DOUT1	89879101	1	1
31P1A04	32P1A04	DOUT1	89879101	1	1
35P1A04	36P1A04	DOUT1	89879101	1	1
27P1A02	29P1A04	DOUT1	89879100	2	2
29P1B24	27P1A16	DOUT10	89879100	2	2
35P1B24	36P1B24	DOUT10	89879101	1	1
33P1B24	34P1B24	DOUT1C	89879101	1	1
31P1B24	32P1B24	DOUT10	89879101	1	1
29P1B24	30P1B24	DOUT10	89879101	1	1
34P1B24	35P1B24	DOUT1C	89879101	2	2
32P1B24	33P1B24	DOUT10	89879101	2	2
30P1B24	31P1B24	DOUT10	89879101	2	2
30P1A30	31P1A30	DOUT11	89879101	2	2
34P1A30	35P1A30	DOUT11	89879101	2	2
32P1A30	33P1A30	DOUT11	89879101	2	2
29P1A30	30P1A30	DOUT11	89879101	1	1
33P1A30	34P1A30	DOUT11	89879101	1	1
31P1A30	32P1A30	DOUT11	89879101	1	1
35P1A30	36P1A30	DOUT11	89879101	1	1
29P1A30	27P1A17	DOUT11	89879100	2	2
29P1A31	27P1A21	DOUT12	89879100	2	2
29P1A31	30P1A31	DOUT12	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
33P1A31	34P1A31	DOUT12	89879101	1	1
31P1A31	32P1A31	DOUT12	89879101	1	1
35P1A31	36P1A31	DOUT12	89879101	1	1
34P1A31	35P1A31	DOUT12	89879101	2	2
32P1A31	33P1A31	DOUT12	89879101	2	2
30P1A31	31P1A31	DOUT12	89879101	2	2
30P1B29	31P1B29	DOUT13	89879101	2	2
34P1B29	35P1B29	DOUT13	89879101	2	2
32P1B29	33P1B29	DOUT13	89879101	2	2
29P1B29	30P1B29	DOUT13	89879101	1	1
33P1B29	34P1B29	DOUT13	89879101	1	1
31P1B29	32P1B29	DOUT13	89879101	1	1
35P1B29	36P1B29	DOUT13	89879101	1	1
29P1B29	27P1A24	DOUT13	89879100	2	2
29P1B30	27P1B24	DOUT14	89879100	2	2
29P1B30	30P1B30	DOUT14	89879101	1	1
33P1B30	34P1B30	DOUT14	89879101	1	1
31P1B30	32P1B30	DOUT14	89879101	1	1
35P1B30	36P1B30	DOUT14	89879101	1	1
32P1B30	33P1B30	DOUT14	89879101	2	2
30P1B30	31P1B30	DOUT14	89879101	2	2
34P1B30	35P1B30	DOUT14	89879101	2	2
30P1B31	31P1B31	DOUT15	89879101	2	2
34P1B31	35P1B31	DOUT15	89879101	2	2
32P1B31	33P1B31	DOUT15	89879101	2	2
29P1B31	30P1B31	DOUT15	89879101	1	1
33P1B31	34P1B31	DOUT15	89879101	1	1
31P1B31	32P1B31	DOUT15	89879101	1	1
35P1B31	36P1B31	DOUT15	89879101	1	1
29P1B31	27P1B25	DOUT15	89879100	2	2
29P2A01	27P2A16	DOUT16	89879100	2	2
29P2A01	30P2A01	DOUT16	89879101	1	1
33P2A01	34P2A01	DOUT16	89879101	1	1
31P2A01	32P2A01	DOUT16	89879101	1	1
35P2A01	36P2A01	DOUT16	89879101	1	1
32P2A01	33P2A01	DOUT16	89879101	2	2
30P2A01	31P2A01	DOUT16	89879101	2	2
34P2A01	35P2A01	DOUT16	89879101	2	2
30P2A02	31P2A02	DOUT17	89879101	2	2
34P2A02	35P2A02	DOUT17	89879101	2	2
32P2A02	33P2A02	DOUT17	89879101	2	2
29P2A02	30P2A02	DOUT17	89879101	1	1
33P2A02	34P2A02	DOUT17	89879101	1	1
31P2A02	32P2A02	DOUT17	89879101	1	1
35P2A02	36P2A02	DOUT17	89879101	1	1
27P2B05	28P2B10	DOUT17	89879100	1	1
28P2B10	29P2A02	DOUT17	89879100	2	2
29P1A06	27P1B04	DOUT2	89879100	2	2
29P1A06	30P1A06	DOUT2	89879101	1	1
33P1A06	34P1A06	DOUT2	89879101	1	1
31P1A06	32P1A06	DOUT2	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
35P1A06	36P1A06	DOUT2	89879101	1	1
32P1A06	33P1A06	DOUT2	89879101	2	2
30P1A06	31P1A06	DOUT2	89879101	2	2
34P1A06	35P1A06	DOUT2	89879101	2	2
30P1A08	31P1A08	DOUT3	89879101	2	2
34P1A08	35P1A08	DOUT3	89879101	2	2
32P1A08	33P1A08	DOUT3	89379101	2	2
29P1A08	30P1A08	DOUT3	89879101	1	1
33P1A08	34P1A08	DOUT3	89879101	1	1
31P1A08	32P1A08	DOUT3	89879101	1	1
35P1A08	36P1A08	DOUT3	89879101	1	1
29P1A08	27P1B05	DOUT3	89879100	2	2
29P1A09	27P1B07	DOUT4	89879100	2	2
29P1A09	30P1A09	DOUT4	89379101	1	1
33P1A09	34P1A09	DOUT4	89879101	1	1
31P1A09	32P1A09	DOUT4	89879101	1	1
35P1A09	36P1A09	DOUT4	89879101	1	1
34P1A09	35P1A09	DOUT4	89879101	2	2
32P1A09	33P1A09	DOUT4	89879101	2	2
30P1A09	31P1A09	DOUT4	89879101	2	2
30P1A14	31P1A14	DOUT5	89879101	2	2
34P1A14	35P1A14	DOUT5	89879101	2	2
32P1A14	33P1A14	DOUT5	89879101	2	2
29P1A14	30P1A14	DOUT5	89879101	1	1
33P1A14	34P1A14	DOUT5	89879101	1	1
31P1A14	32P1A14	DOUT5	89879101	1	1
35P1A14	36P1A14	DOUT5	89879101	1	1
29P1A14	27P1B09	DOUT5	89879100	2	2
29P1A17	27P1B10	DOUT6	89879100	2	2
29P1A17	30P1A17	DOUT6	89879101	1	1
33P1A17	34P1A17	DOUT6	89379101	1	1
31P1A17	32P1A17	DOUT6	89879101	1	1
35P1A17	36P1A17	DOUT6	89879101	1	1
32P1A17	33P1A17	DOUT6	89879101	2	2
30P1A17	31P1A17	DOUT6	89879101	2	2
34P1A17	35P1A17	DOUT6	89879101	2	2
30P1A19	31P1A19	DOUT7	89879101	2	2
34P1A19	35P1A19	DOUT7	89879101	2	2
32P1A19	33P1A19	DOUT7	89879101	2	2
29P1A19	30P1A19	DOUT7	89879101	1	1
33P1A19	34P1A19	DOUT7	89879101	1	1
31P1A19	32P1A19	DOUT7	89879101	1	1
35P1A19	36P1A19	DOUT7	89879101	1	1
29P1A19	27P1B12	DOUT7	89879100	2	2
29P1A20	27P1A13	DOUT8	89379100	2	2
29P1A20	30P1A20	DOUT8	89879101	1	1
33P1A20	34P1A20	DOUT8	89879101	1	1
31P1A20	32P1A20	DOUT8	89879101	1	1
35P1A20	36P1A20	DOUT8	89879101	1	1
34P1A20	35P1A20	DOUT8	89879101	2	2
32P1A20	33P1A20	DOUT8	89879101	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
30P1A20	31P1A20	DOUT8	89879101	2	2
30P1A25	31P1A20	DOUT9	89879101	2	2
34P1A25	35P1A20	DOUT9	89879101	2	2
32P1A25	33P1A20	DOUT9	89879101	2	2
29P1A25	30P1A20	DOUT9	89879101	1	1
33P1A25	34P1A20	DOUT9	89879101	1	1
31P1A25	32P1A20	DOUT9	89879101	1	1
35P1A25	36P1A20	DOUT9	89879101	1	1
29P1A25	27P1B15	DOUT9	89879100	2	2
19P2B23	16P2B23	DRIVE FAULT	89879100	1	1
19P2A20	16P2B11	DRIVE RD*	89879100	1	1
19P2A25	16P2B24	DRIVE SE*	89879100	1	1
19P1A24	16P1B07	DSA CONNECT	89879100	2	2
13P2A20	12P1A23	DSA WREN*	89879100	2	2
14P2B30	13P2A20	DSA WREN*	89879100	1	1
18P2B04	16P1A07	DSA-BUFF1*	89879100	2	2
30P2B01	28P2A01	DX1*	89879100	1	1
31P2B01	28P2B01	DX2*	89879100	1	1
32P2B01	28P1B31	DX3*	89879100	1	1
33P2B01	28P2B11	DX4*	89879100	1	1
34P2B01	28P2B06	DX5*	89879100	1	1
35P2B01	28P2B05	DX6*	89879100	1	1
36P2B01	28P2A05	DX7*	89879100	1	1
28P2A22	27P2B06	D16	89879100	1	1
28P2A13	27P1B27	D17	89879100	2	2
23P2B14	22P1A26	EAD*	89879100	2	2
13P2B10	12P1A11	EARLY WDS	89879100	2	2
33P2A11	27P2A05	EDX*	89879100	1	1
22P2B18	20P2B03	EINT	89879100	2	2
22P2B18	21P1A19	EINT	89879100	1	1
24P2B18	23P2A17	EI5*	89879100	2	2
13P2B20	12P1B28	ENA*	89879100	2	2
14P2B29	13P2B20	ENA*	89879100	1	1
21P1A15	24P1B02	ENI	89879100	2	2
21P1A15	23P2B15	ENI	89879100	1	1
22P1B15	24P1B18	ENI2E*	89879100	1	1
23P2A20	24P1B18	ENI2E*	89879100	2	2
21P1B24	22P1A05	ENI20*	89879100	2	2
22P1A05	24P1A07	ENI20*	89879100	1	1
21P1B24	23P2A21	ENI20*	89879100	1	1
22P1A08	23P2B16	ENI3*	89879100	2	2
22P1A10	21P2B14	ENI4*	89879100	1	1
21P1B18	20P1A24	ENTER*	89879100	1	1
22P2B11	21P1B18	ENTER*	89879100	2	2
13P1A31	12P1A25	EOG*	89879100	2	2
14P2A27	13P1A31	EOG*	89879100	1	1
14P2B01	13P2A13	EOP	89879100	1	1
12P2A08	11P2B03	EOP	89879100	1	1
19P1A20	16P1B30	EOP	89879100	2	2
13P2A13	12P2A08	EOP	89879100	2	2
19P1B31	16P1B29	EOPMCT BSY*	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
16P1B29	15P2B03	ECPMCT BSY*	89879100	1	1
12P1A24	11P2B16	EORS	89879100	1	1
17P1A06	16P1B25	EOS	89879100	1	1
14P2B27	13P2B23	EOT*	89879100	1	1
19P1B03	15P2A19	ECU.NUM.MAT	89879100	1	1
23P1B27	22P1B08	EXT	89879100	1	1
21P2A10	23P2B17	FEO*	89879100	2	2
21P2A10	22P1A18	FEO*	89879100	1	1
23P2B20	22P1B18	FIEF	89879100	2	2
14P2B03	11P1B28	FILL	89879100	1	1
13P2B18	11P2B15	FM/TM	89879100	1	1
14P1B24	12P2A17	FM/TM	89879100	1	1
14P1B24	13P2B18	FM/TM	89879100	2	2
24P1A03	21P1A27	FS*	89879100	1	1
22P1A27	21P1A09	F1E1	89879100	2	2
22P1A20	24P2B29	F1E23	89879100	1	1
23P2B02	22P2B08	F23	89879100	1	1
14P2B28	13P2B25	GAP CLOCK	89879100	1	1
14P2B26	12P2B17	GC128	89879100	1	1
08P1B22	12P2B17	GC128	89879104		
25P1B21	21P2B02	GLL	89879100	2	2
26P1B21	21P1B20	GLM	89879100	1	1
25P2B03	21P1B31	GML	89879100	1	1
26P2B03	21P2B03	GMM	89879100	2	2
09P1A01	09P1B11	GND	89879104		
23P1B11	27P2B21	GND	89879104		
22P2A26	23P1B16	GOAQ*	89879100	1	1
20P2B02	23P1B21	GOCS	89879100	1	1
21P2A05	24P2B25	GOCS	89879100	1	1
22P1A11	23P1B21	GOCS	89879100	2	2
20P2B02	21P2A05	GOCS	89879100	2	2
21P2A04	20P1B28	GOCSW*	89879100	1	1
27P2B09	23P1A08	GOM1	89879104		
33P2B11	23P1A05	GOM2	89879104		
31P2B20	27P2B23	GPEC*	89879100	1	1
27P2B23	21P1B21	GPEC*	89879100	2	2
25P1A02	21P1A22	GSL*	89879100	2	2
21P1A24	25P2A12	GSM*	89879100	2	2
21P1A24	26P1A02	GSM*	89879100	1	1
26P1A25	26P1A24	HIGH	89879100	1	1
26P2B10	26P2A12	HIGH	89879100	1	1
25P2B06	26P2B16	HIGH	89879100	1	1
26P2B16	26P2B10	HIGH	89879100	2	2
26P2A12	26P1A25	HIGH	89879100	2	2
27P2B14	28P2A25	HOLD	89879100	2	2
27P2A24	28P2A19	HOLDW	89879100	1	1
27P2B13	27P2A02	ICA*ICO*	89879100	2	2
27P2A08	27P2B03	ICA-ICO	89879100	2	2
14P2B14	08P1A24	ID ABORT*	89879100	1	1
14P1B30	13P2B03	ILLUSCODE	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
13P1B18	12P1B08	INCCA*	89879100	2	2
18P1A31	16P1B23	INCR TA	89879100	2	2
16P1B23	15P2B23	INCR TA	89879100	1	1
19P2A26	18P1A31	INCR TA	89879100	1	1
18P2A02	17P2B01	INCR.SECTCR	89879100	2	2
19P2A17	16P2B09	INDEX GATED	89879100	1	1
22P2A08	21P1B23	INDIND*	89879100	1	1
22P2A08	20P2A18	INDIND*	89879100	2	2
17P2A14	16P1B10	INHIBIT NEE	89879100	1	1
19P2A21	17P1A17	INIT	89879100	2	2
19P1B28	16P1B27	INIT Q	89879100	2	2
23P1A21	22P1B27	INO	89879100	1	1
19P1B23	17P1A28	INPUT CKWD	89879100	2	2
23P2A27	22P1B23	INR	89879100	2	2
23P2A27	21P2A23	INR	89879100	1	1
13P2B15	12P2B16	INT	89879100	2	2
21P1B16	20P1A30	INT.SW*	89879100	1	1
21P2B07	25P1A10	INTOL	89879100	1	1
25P1B10	20P2A12	INT1L*	89879100	1	1
23P2A07	22P1B29	IN32	89879100	2	2
23P1A25	22P1A30	IN41	89879100	1	1
23P1B17	21P2B23	IO	89879100	1	1
24P1B13	23P1B17	IO	89879100	2	2
21P1A20	23P1A09	IRCK	89879100	2	2
23P1A09	24P1A21	IRCK	89879100	1	1
24P1B17	22P2A25	IRJ*	89879100	2	2
27P2B15	27P2A04	ISAISO	89879100	1	1
12P1B05	11P2B12	ISTSP	89879100	1	1
25P1A25	21P2A16	ITA2L*	89879100	1	1
25P1A24	21P2A18	ITA3L	89879100	2	2
25P2B10	21P2A20	ITA4L*	89879100	1	1
22P1A02	24P2A15	ITR	89879100	2	2
23P2B29	24P2A15	ITR	89879100	1	1
24P1B05	23P1B18	I1	89879100	1	1
24P1B10	23P1A17	I2	89879100	2	2
24P1A10	23P1B05	I3	89879100	1	1
23P1B24	21P1B01	I4	89879100	1	1
24P2B26	23P1B24	I4	89879100	2	2
21P1A01	23P2A10	I5	89879100	2	2
23P2A10	24P2B24	I5	89879100	1	1
23P2B10	24P2B23	I6	89879100	1	1
21P1B05	23P2B10	I6	89879100	2	2
22P1B02	24P2A22	I65	89879100	2	2
22P1A01	21P1A05	I7*	89879100	1	1
24P2A23	22P1A01	I7*	89879100	2	2
21P2A25	23P2A13	JENI	89879100	1	1
23P2B09	22P2A13	JITR*	89879100	2	2
21P2B18	22P2A19	JKCK	89879100	2	2
22P2A19	23P2B05	JKCK	89879100	1	1
23P2B04	22P2B12	JOP	89879100	1	1
23P2A05	22P2A18	JOP2	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
24P1A04	23P2A24	JRNI*	89879100	2	2
23P2A24	22P2B10	JRNI*	89879100	1	1
23P1A20	21P1A28	KENI1*	89879100	1	1
23P2A23	22P2B13	KITR	89879100	1	1
22P2B19	21P1A10	KOVF	89879100	1	1
23P2B25	21P2A06	KRNI	89879100	2	2
22P2B14	21P1B28	KRNI1	89879100	2	2
19P2A28	15P2B07	LA	89879100	2	2
19P2A28	16P2B01	LA	89879100	1	1
19P2B11	16P2B26	LA CLEAR*	89879100	1	1
16P2B04	15P2B02	LA DIFF=C*	89879100	1	1
14P1B13	12P1A09	LAST WORD	89879100	2	2
19P2A06	17P1A09	LBL*	89879100	2	2
25P1B26	21P1A23	LCNL	89879100	2	2
26P1B26	21P1B29	LCNM	89879100	2	2
13P1B09	12P2B19	LDLWA*	89879100	2	2
14P1A09	13P1B09	LDLWA*	89879100	1	1
14P1B31	12P2B12	LEGCC	89879100	2	2
14P2B10	12P2A07	LEGCF	89879100	1	1
14P2B22	12P2A04	LEGMF	89879100	1	1
13P2B02	12P2A12	LEGUS	89879100	2	2
19P1A25	17P2A24	LOAD CKWD I	89879100	1	1
18P2A15	16P1B19	LOAD SHIFT*	89879100	2	2
28P2A29	27P2A26	LOADRA*	89879100	1	1
14P2A14	12P1A10	LOCKOUT*	89879100	1	1
19P2A18	16P1A22	LOST DATA	89879100	1	1
13P2A12	12P1B04	LOST DATA	89879100	2	2
13P2A23	12P1A16	LOST DATA*	89879100	2	2
13P1A02	12P1A04	LOWX1*	89879100	2	2
12P1A26	11P2A18	LRCC STATE	89879100	1	1
25P2B07	24P2A07	M	89879100	2	2
24P2A07	22P2B03	M	89879100	1	1
26P2B07	25P2B07	M	89879100	1	1
22P2A23	25P2B30	MC	89879100	1	1
18P1B25	17P1A22	MC	89879100	2	2
16P1A19	15P2B18	MC	89879100	2	2
17P1A22	16P1A19	MC	89879100	1	1
25P2B30	26P2B30	MC	89879100	2	2
21P2B29	22P2A23	MC	89879100	2	2
14P2A04	13P2A09	MC*	89879100	1	1
18P2B20	16P1B28	MC*	89879100	1	1
15P1B23	16P2B07	MC*	89879100	1	1
25P1B20	20P2B08	MC*	89879100	1	1
19P2B26	18P2B20	MC*	89879100	2	2
13P2A09	12P2B02	MC*	89879100	2	2
20P2B08	21P2A27	MC*	89879100	2	2
15P1B23	07P1B23	MC*	89879100	2	2
03P1A09	01P1B23	MC*	89879100	2	2
02P1B23	06P1B23	MC*	89879103	2	2
06P1B23	07P1B23	MC*	89879103	1	1
01P1B23	02P1B23	MC*	89879103	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
25P1B20	15P1B23	MC*	89879100	3	3
21P2A27	13P2B11	MC*	89879100	3	3
03P1A09	04P1A09	MC*	89879102	1	1
04P1A09	05P1A09	MC*	89879102	2	1
21P2B27	20P1B08	MCCS*	89879100	1	1
25P2A13	23P2A27	MCK	89879100	2	2
26P2A13	25P2A13	MCK	89879100	1	1
25P2A07	21P1A31	MCNL	89879100	1	1
26P2A07	21P1B30	MCNM	89879100	2	2
27P2B20	24P1B20	MDEL	89879100	2	2
31P2A19	27P2B20	MDEL	89879100	1	1
22P1A03	23P2B30	MDS	89879100	1	1
23P2B03	24P1B01	MDSE	89879100	1	1
24P2B27	23P2A08	MDSO	89879100	1	1
24P1A13	23P2A02	MDS1	89879100	1	1
24P1A13	22P1B13	MDS1	89879100	2	2
23P1A28	24P2B04	MDS2	89879100	2	2
29P2A06	28P2B03	MDX0*	89879100	1	1
30P2A06	28P2A02	MDX1*	89879100	1	1
31P2A06	28P2A04	MDX2*	89879100	1	1
32P2A06	28P2B02	MDX3*	89879100	1	1
33P2A06	28P2B04	MDX4*	89879100	1	1
34P2A06	28P2B07	MDX5*	89879100	1	1
35P2A06	28P2A07	MDX6*	89879100	1	1
36P2A06	28P2A08	MDX7*	89879100	1	1
22P2A11	23P2B01	MD1*	89879100	1	1
23P2B01	24P2A11	MD1*	89879100	2	2
24P2B12	23P1B31	MD21*	89879100	2	2
23P1B03	22P1A07	MMRQ	89879100	2	2
13P2A15	11P2B31	MODESEL*	89879100	1	1
22P2B15	21P2B22	MPC	89879100	1	1
23P1A26	22P2B15	MPC	89879100	2	2
27P1A27	21P2A17	MPRY	89879100	2	2
31P2B04	27P1A27	MPRY	89879100	1	1
27P2B31	28P2B31	MPWR*	89879100	1	1
34P2B30	35P2B30	MPWR*	89879101	2	2
32P2B30	33P2B30	MPWR*	89879101	2	2
30P2B30	31P2B30	MPWR*	89879101	2	2
29P2B30	30P2B30	MPWR*	89879101	1	1
35P2B30	36P2B30	MPWR*	89879101	1	1
33P2B30	34P2B30	MPWR*	89879101	1	1
28P2B31	29P2B30	MPWR*	89879100	2	2
33P2B14	27P2A14	MSXA*	89879100	1	1
25P1B14	26P1B14	MTADD	89879100	1	1
24P1A17	25P1B14	MTADD	89879100	2	2
25P1B18	27P1B02	MXOL	89879100	2	2
24P1B16	25P1B18	MXOL	89879100	1	1
31P1B01	27P1B02	MXOL	89879100	1	1
24P1A25	26P1B18	MXOM	89879100	1	1
26P1B18	27P1A14	MXOM	89879100	2	2
31P1B13	27P1A14	MxOM	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
31P1B02	27P1B03	MX1L	89879100	1	1
24P1A16	25P1A19	MX1L	89879100	1	1
25P1A19	27P1B03	MX1L	89879100	2	2
26P1A19	27P1A15	MX1M	89879100	2	2
24P1A23	26P1A19	MX1M	89879100	1	1
31P1B14	27P1A15	MX1M	89879100	1	1
31P2B03	27P1A26	MX17	89879100	1	1
21P2A19	27P1A26	MX17	89879100	2	2
25P1B15	27P1A04	MX2L	89879100	2	2
31P1B04	27P1A04	MX2L	89879100	1	1
24P1A18	25P1B15	MX2L	89879100	1	1
24P1B14	26P1B15	MX2M	89879100	1	1
31P1B15	27P1B17	MX2M	89879100	1	1
26P1B15	27P1B17	MX2M	89879100	2	2
25P1A16	27P1A05	MX3L	89879100	2	2
31P1B06	27P1A06	MX3L	89879100	1	1
24P1A20	25P1A16	MX3L	89879100	1	1
24P1B15	26P1A16	MX3M	89879100	1	1
31P1A16	27P1B19	MX3M	89879100	1	1
26P1A16	27P1B19	MX3M	89879100	2	2
27P1B08	25P2A20	MX4L	89879100	2	2
31P1B08	27P1B08	MX4L	89879100	1	1
25P2A20	24P2B19	MX4L	89879100	1	1
26P2A20	24P2B05	MX4M	89879100	1	1
31P1B18	27P1B21	MX4M	89879100	1	1
27P1B21	26P2A20	MX4M	89879100	2	2
27P1A09	25P2B20	MX5L	89879100	2	2
31P1B09	27P1A09	MX5L	89879100	1	1
25P2B20	24P2B17	MX5L	89879100	1	1
26P2B20	24P2A08	MX5M	89879100	1	1
31P1A22	27P1A23	MX5M	89879100	1	1
27P1A23	26P2B20	MX5M	89879100	2	2
25P2A18	27P1A11	MX6L	89879100	2	2
31P1B12	27P1A11	MX6L	89879100	1	1
24P2A19	25P2A18	MX6L	89879100	1	1
31P1B21	27P1A22	MX6M	89879100	1	1
26P2A18	24P2B08	MX6M	89879100	1	1
27P1A22	26P2A18	MX6M	89879100	2	2
27P1B13	25P2B19	MX7L	89879100	2	2
25P2B19	24P2A16	MX7L	89879100	1	1
31P1A13	27P1B13	MX7L	89879100	1	1
31P1B17	27P1B20	MX7M	89879100	1	1
26P2B19	24P2A05	MX7M	89879100	1	1
27P1B20	26P2B19	MX7M	89879100	2	2
24P2A14	23P1B28	NO	89879100	2	2
10P2B01	10P1B28	NODROPOUT	89879104		
33P2B13	27P2B11	NORMAL	89879100	1	1
27P2B11	21P2A11	NORMAL	89879100	2	2
23P2B07	24P2B14	N41	89879100	2	2
22P1B05	23P2B07	N41	89879100	1	1
02P1A03	06P1A03	OA0*	89879103	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
06P1A03	07P1A03	0A0*	89879103	1	1
01P1A03	02P1A03	0A0*	89879103	1	1
15P1A03	13P1B29	0A0*	89879100	1	1
17P2B04	19P1A30	0A0*	89879100	1	1
25P2A05	20P2A20	0A0*	89879100	1	1
19P1A30	15P1A03	0A0*	89879100	2	2
20P2A20	17P2B04	0A0*	89879100	2	2
13P1B29	07P1A03	0A0*	89879100	2	2
13P1A30	07P1B01	0A1*	89879100	2	2
19P1B26	15P1B01	0A1*	89879100	2	2
20P2B20	17P2A02	0A1*	89879100	2	2
25P2A02	20P2B20	0A1*	89879100	1	1
15P1B01	13P1A30	0A1*	89879100	1	1
17P2A02	19P1B26	0A1*	89879100	1	1
06P1B01	07P1B01	0A1*	89879103	1	1
01P1B01	02P1B01	0A1*	89879103	1	1
02P1B01	06P1B01	0A1*	89879103	2	2
02P1B06	06P1B06	0A10*	89879103	2	2
06P1B06	07P1B06	0A10*	89879103	1	1
01P1B06	02P1B06	0A10*	89879103	1	1
26P1A30	20P2B25	0A10*	89879100	1	1
15P1B06	14P1B20	0A10*	89879100	1	1
17P2B22	19P1A14	0A10*	89879100	1	1
19P1A14	15P1B06	0A10*	89879100	2	2
20P2B26	17P2B27	0A10*	89879100	2	2
14P1B20	07P1B06	0A10*	89879100	2	2
14P1A20	07P1A05	0A11*	89879100	2	2
19P1B12	15P1A05	0A11*	89879100	2	2
20P2B28	17P2A20	0A11*	89879100	2	2
15P1A05	14P1A20	0A11*	89879100	1	1
17P2A20	19P1B12	0A11*	89879100	1	1
26P2B04	20P2B28	0A11*	89879100	1	1
06P1A05	07P1A05	0A11*	89879103	1	1
01P1A05	02P1A05	0A11*	89879103	1	1
02P1A05	06P1A05	0A11*	89879103	2	2
02P1A04	06P1A04	0A12*	89879103	2	2
06P1A04	07P1A04	0A12*	89879103	1	1
01P1A04	02P1A04	0A12*	89879103	1	1
15P1A04	14P1B19	0A12*	89879100	1	1
17P2A19	19P1B08	0A12*	89879100	1	1
19P1B08	15P1A04	0A12*	89879100	2	2
26P2A23	17P2A19	0A12*	89879100	2	2
14P1B19	07P1A04	0A12*	89879100	2	2
14P1A18	07P1B09	0A13*	89879100	2	2
19P1A07	15P1B09	0A13*	89879100	2	2
20P2A11	17P2B17	0A13*	89879100	2	2
15P1B09	14P1A18	0A13*	89879100	1	1
17P2B17	19P1A07	0A13*	89879100	1	1
06P1B09	07P1B09	0A13*	89879103	1	1
01P1B09	02P1B09	0A13*	89879103	1	1
02P1B09	06P1B09	0A13*	89879103	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
26P2B24	20P2A11	0A13*	89879100	1	1
02P1B10	06P1B10	0A14*	89879103	2	2
06P1B10	07P1B10	0A14*	89879103	1	1
01P1B10	02P1B10	0A14*	89879103	1	1
15P1B10	14P1B18	0A14*	89879100	1	1
17P2B16	19P1A01	0A14*	89879100	1	1
19P1A01	15P1B10	0A14*	89879100	2	2
26P2A22	17P2B16	0A14*	89879100	2	2
14P1B18	07P1B10	0A14*	89879100	2	2
14P1A19	07P1A11	0A15*	89879100	2	2
19P1B07	15P1A11	0A15*	89879100	2	2
26P2B22	17P2B18	0A15*	89879100	2	2
15P1A11	14P1A19	0A15*	89879100	1	1
17P2B18	19P1B07	0A15*	89879100	1	1
06P1A11	07P1A11	0A15*	89879103	1	1
01P1A11	02P1A11	0A15*	89879103	1	1
02P1A11	06P1A11	0A15*	89879103	2	2
02P1B02	06P1B02	0A2*	89879103	2	2
06P1B02	07P1B02	0A2*	89879103	1	1
01P1B02	02P1B02	0A2*	89879103	1	1
15P1B02	13P1A21	0A2*	89879100	1	1
17P2A01	19P1B24	0A2*	89879100	1	1
25P1A30	20P2B19	0A2*	89879100	1	1
19P1B24	15P1B02	0A2*	89879100	2	2
20P2B19	17P2A01	0A2*	89879100	2	2
13P1A21	07P1B02	0A2*	89879100	2	2
13P1B21	07P1A06	0A3*	89879100	2	2
19P1A26	15P1A06	0A3*	89879100	2	2
20P2A17	17P2B06	0A3*	89879100	2	2
25P2B04	20P2A17	0A3*	89879100	1	1
15P1A06	13P1B21	0A3*	89879100	1	1
17P2B06	19P1A26	0A3*	89879100	1	1
06P1A06	07P1A06	0A3*	89879103	1	1
01P1A06	02P1A06	0A3*	89879103	1	1
02P1A06	06P1A06	0A3*	89879103	2	2
02P1A07	06P1A07	0A4*	89879103	2	2
06P1A07	07P1A07	0A4*	89879103	1	1
01P1A07	02P1A07	0A4*	89879103	1	1
15P1A07	13P1A20	0A4*	89879100	1	1
17P2A11	19P1B18	0A4*	89879100	1	1
25P2A23	20P2A21	0A4*	89879100	1	1
19P1B18	15P1A07	0A4*	89879100	2	2
20P2A21	17P2A11	0A4*	89879100	2	2
13P1A20	07P1A07	0A4*	89879100	2	2
13P1B19	07P1A01	0A5*	89879100	2	2
19P1A19	15P1A01	0A5*	89879100	2	2
20P2B22	17P2B10	0A5*	89879100	2	2
25P2B24	20P2B22	0A5*	89879100	1	1
15P1A01	13P1B19	0A5*	89879100	1	1
17P2B10	19P1A19	0A5*	89879100	1	1
06P1A01	07P1A01	0A5*	89879103	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
01P1A01	02P1A01	0A5*	89879103	1	1
02P1A01	06P1A01	0A5*	89879103	2	2
02P1A02	06P1A02	0A6*	89879103	2	2
06P1A02	07P1A02	0A6*	89879103	1	1
01P1A02	02P1A02	0A6*	89879103	1	1
15P1A02	13P1A19	0A6*	89879100	1	1
17P2B09	19P1A17	0A6*	89879100	1	1
25P2A22	20P2B18	0A6*	89879100	1	1
19P1A17	15P1A02	0A6*	89879100	2	2
20P2B18	17P2B09	0A6*	89879100	2	2
13P1A19	07P1A02	0A6*	89879100	2	2
13P1B20	07P1B03	0A7*	89879100	2	2
19P1B16	15P1B03	0A7*	89879100	2	2
20P2A19	17P2B08	0A7*	89879100	2	2
25P2B22	20P2A19	0A7*	89879100	1	1
15P1B03	13P1B20	0A7*	89879100	1	1
17P2B08	19P1B16	0A7*	89879100	1	1
06P1B03	07P1B03	0A7*	89879103	1	1
01P1B03	02P1B03	0A7*	89879103	1	1
02P1B03	06P1B03	0A7*	89879103	2	2
02P1B04	06P1B04	0A8*	89879103	2	2
06P1B04	07P1B04	0A8*	89879103	1	1
01P1B04	02P1B04	0A8*	89879103	1	1
26P2A05	20P2B23	0A8*	89879100	1	1
15P1B04	14P1B29	0A8*	89879100	1	1
17P2A13	19P1A15	0A8*	89879100	1	1
19P1A15	15P1B04	0A8*	89879100	2	2
20P2B23	17P2A13	0A8*	89879100	2	2
14P1B29	07P1B04	0A8*	89879100	2	2
14P1B22	07P1B05	0A9*	89879100	2	2
19P1A13	15P1B05	0A9*	89879100	2	2
20P2B24	17P2A12	0A9*	89879100	2	2
15P1B05	14P1B22	0A9*	89879100	1	1
17P2A12	19P1A13	0A9*	89879100	1	1
26P2A02	20P2B24	0A9*	89879100	1	1
06P1B05	07P1B05	0A9*	89879103	1	1
01P1B05	02P1B05	0A9*	89879103	1	1
02P1B05	06P1B05	0A9*	89879103	2	2
22P1B10	24P2A01	0D*	89879100	2	2
21P1B13	23P2B19	0DD*	89879100	2	2
22P1B12	24P1B09	0DD*	89879100	2	2
21P1B13	22P1B12	0DD*	89879100	1	1
24P1A02	23P1B22	0DD2	89879100	1	1
23P1B22	22P1A28	0DD2	89879100	2	2
21P2B11	23P2B11	0DD2*	89879100	1	1
24P2B16	23P2A16	0I6*	89879100	1	1
17P2B05	16P2B03	0N CYL	89879100	1	1
19P2A22	17P2B05	0N CYL	89879100	2	2
23P1A27	22P1B14	0P	89879100	1	1
23P2A04	24P2B28	0PE*	89879100	1	1
23P1B23	20P1B23	0PIND	89879100	1	1

	FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
	23P2B06	24P1A06	OPO*	89879100	2	2
	22P1A19	20P1A22	OPST	89879100	1	1
	22P1A19	21P2B09	OPST	89879100	2	2
	22P1A06	23P2B24	OP20*	89879100	1	1
	23P1A07	27P2A23	OSC*	89879104		
	22P2A12	20P2A01	OVFL*	89879100	2	2
	22P2A12	21P1B10	OVFL*	89879100	1	1
	26P2B27	21P1B12	OVFW*	89879100	1	1
	10P1A31	09P1A31	O1*	89879100	2	2
	09P1A31	08P2A22	O1*	89879100	1	1
	24P1B30	22P2B16	O1*	89879100	2	2
	09P1B24	08P1A26	O12	89879100	1	1
	10P1B24	09P1B24	O12	89879100	2	2
	10P1A30	09P1A30	O2*	89879100	2	2
	09P1A30	08P2B26	O2*	89879100	1	1
	27P1B28	28P2A11	PAR	89879100	2	2
	13P2A18	11P2B17	PAR ERR.	89879100	1	1
	14P1B23	13P2A18	PAR ERR.	89879100	2	2
	28P1A13	27P2A22	PBC	89879100	2	2
	13P2B07	10P1A01	PC 16CC*	89879100	2	2
⟶	09P2B01	10P2A01	AS1*/BS0*		1	1
	26P1B13	25P1B13	PCK	89879100	1	1
	25P1B13	23P1B13	PCK	89879100	2	2
	21P2A22	20P1A26	PCL*	89879100	1	1
	10P1B01	09P1B01	PC2	89879100	1	1
	13P1B31	08P1A03	PE ENABLE	89879100	2	2
	14P2A01	08P2A18	PE EOP*	89879100	1	1
	13P1B30	08P2B09	PE LOST CAT	89879100	2	2
	11P1B29	08P2A05	PE PARERR*	89879100	2	2
	14P2B23	13P2B06	PE START	89879100	1	1
	12P1B25	08P1B02	PE START	89879104		
	13P2B06	08P1B02	PE START	89879100	2	2
	13P2B08	08P2B12	PE WORNING	89879100	2	2
	13P2A29	08P2A14	PECHARCLK	89879100	2	2
	13P2A30	08P1B13	PECLOCK*	89879100	2	2
	24P1A27	21P2A09	PEF*	89879100	2	2
	04P1A17	05P1A17	PEL*	89879102	2	1
	03P1A17	04P1A17	PEL*	89879102	1	1
	12P1B01	05P1A17	PEL*	89879100	2	2
	21P1B06	19P1A10	PEL*	89879100	2	2
	27P2B26	20P2A07	PEL*	89879100	2	2
	19P1A10	12P1B01	PEL*	89879100	1	1
	20P2A07	21P1B06	PEL*	89879100	1	1
	31P2A22	27P2B26	PEL*	89879100	1	1
	21P1A14	23P1A15	PH1	89879100	2	2
	22P2B29	23P1B08	PH2	89879100	1	1
	22P2B20	23P1A22	PH3	89879100	1	1
	21P2B05	22P2B20	PH3	89879100	2	2
	25P1A23	21P2A01	PLL	89879100	1	1
	26P1A23	21P1A21	PLM	89879100	1	1
	25P2A01	21P2B01	PML	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
26P2A01	21P2A02	PMM	89879100	2	2
19P2B10	15P2A20	POKM	89879100	2	2
08P2B24	12P1A06	POSTAMBLE	89879104		
14P2B20	08P1A27	PRBOT	89879100	1	1
11P1A03	10P2A28	PRDOUT 0	89879100	2	2
11P1A01	10P2A12	PRDOUT 1	89879100	2	2
11P1B06	09P2A28	PRDOUT 2	89879100	2	2
11P1B07	09P1A21	PRDOUT 3	89879100	2	2
11P1B03	09P2A12	PRDOUT 4	89879100	2	2
11P1B08	09P1B06	PRDOUT 6	89879100	2	2
11P1B09	10P1A21	PRDOUT 7	89879100	2	2
11P1B01	10P1B06	PRDOUT5	89879100	2	2
21P2B13	20P1B22	PRF(PFIND)	89879100	1	1
10P1B27	09P1B27	PRFB	89879100	2	2
09P1B27	08P1B23	PRFB	89879104		
21P1A18	20P1A11	PRGST	89879100	1	1
11P1A11	10P2B26	PRIN 0	89879100	2	2
11P1B12	10P2A19	PRIN 1	89879100	1	1
11P1A14	09P2B26	PRIN 2	89879100	2	2
11P1B15	09P1A23	PRIN 3	89879100	1	1
11P1B13	09P2A19	PRIN 4	89879100	2	2
11P1A13	10P1A12	PRIN 5	89879100	1	1
11P1A12	09P1A12	PRIN 6	89879100	2	2
11P1B14	10P1A23	PRIN 7	89879100	1	1
11P2B04	10P1A10	PRINP	89879100	1	1
14P2A13	12P1A02	PROT FAULT	89879100	1	1
13P2A25	12P2B15	PROTECTED	89879100	2	2
11P2B25	08P2A23	PRSTROBE	89879100	1	1
21P2A28	15P2B28	PRTAQ*	89879100	1	1
15P2B28	12P2A19	PRTAQ*	89879100	2	2
15P2B28	15P1A23	PRTAQ*	89879100	3	3
12P2A19	07P1A23	PRTAQ*	89879100	3	3
21P1A25	20P1B30	PRTBIT	89879100	1	1
27P1B30	21P2B24	PRTM*	89879100	2	2
02P1A23	06P1A23	PRTM*	89879103	2	2
06P1A23	07P1A23	PRTM*	89879103	1	1
01P1A23	02P1A23	PRTM*	89879103	1	1
31P2A09	27P1B30	PRTM*	89879100	1	1
33P2B12	27P2B01	PRTSW	89879100	1	1
21P2A14	20P1B09	PRTSW	89879100	1	1
27P2B01	21P2A14	PRTSW	89879100	2	2
09P2A21	08P2A26	PRTY FN B1*	89879100	2	2
10P2A21	08P2B29	PRTY GN A1*	89879100	2	2
10P2A08	08P2A28	PRTY GN A2*	89879100	1	1
10P1A13	08P2B28	PRTY GN A3*	89879100	2	2
10P1B02	08P2A27	PRTY GN A4*	89879100	1	1
10P1A25	08P2B27	PRTY GN A5*	89879100	2	2
09P2A08	08P2B30	PRTY GN B2*	89879100	2	2
09P1A13	08P2A30	PRTY GN B3*	89879100	2	2
09P1B02	08P2B16	PRTY GN B4*	89879100	2	2
24P1B06	21P2B25	PRY	89879100	1	1

	FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
	11P2A01	08P2A08	PSFM*	89879100	1	1
	25P1A12	26P1A12	PTADD	89879100	2	2
	22P2B24	24P1A19	PTADD	89879100	2	2
	24P1A19	25P1A12	PTADD	89879100	1	1
	19P2B24	16P2B12	PUR*	89879100	1	1
	11P1A16	10P1A05	PWDIN 0	89879100	2	2
	11P1A09	10P1A20	PWDIN 1	89879100	2	2
	11P1B16	09P1A05	PWDIN 2	89879100	2	2
	11P1B10	09P2B12	PWDIN 3	89879100	2	2
	11P1A15	09P1A20	PWDIN 4	89879100	2	2
	11P1B17	10P2A27	PWDIN 5	89879100	2	2
	11P1B19	09P2A27	PWDIN 6	89879100	2	2
	11P1A18	10P2B12	PWDIN 7	89879100	2	2
	11P1B18	10P2B03	PWDINP	89879100	2	2
	14P2A30	08P1A07	PWID	89879100	1	1
	11P2B09	10P1A02	PWOUT 0	89879100	1	1
	11P2B08	10P1B23	PWOUT 1	89879100	1	1
	11P2B13	09P1A02	PWOUT 2	89879100	1	1
	11P2A13	09P2B10	PWOUT 3	89879100	1	1
	11P2B20	09P1B23	PWOUT 4	89879100	1	1
	11P2B18	10P2B23	PWOUT 5	89879100	1	1
	11P2B24	09P2B23	PWOUT 6	89879100	1	1
	11P2B22	10P2B10	PWOUT 7	89879100	1	1
	11P2B23	10P2B08	PWOUTP	89879100	1	1
	11P2B26	08P1A10	PWRESET	89879100	1	1
	12P1A28	08P1A02	PWRQ	89879100	2	2
	12P1B12	08P1A13	PWRQSHIFTED	89879100	2	2
	28P2A14	27P2A17	P16	89879100	1	1
	22P2A21	20P1B25	P4M	89879100	1	1
	27P2A15	22P2A21	P4M	89879100	2	2
	25P1A14	26P1A14	QCK	89879100	2	2
	23P1A11	25P1A14	QCK	89879100	1	1
	20P2A05	19P1A28	Q0	89879100	1	1
	25P1B12	20P2A05	Q0	89879100	2	2
	24P2B02	25P2A06	QSX	89879100	2	2
	21P1B03	24P2B02	QSX	89879100	1	1
	25P2A06	26P2A06	QSX	89879100	1	1
	24P2B22	25P2A26	QTADD	89879100	1	1
	25P2A26	26P2A26	QTADD	89879100	2	2
	15P1A12	12P1B31	Q0	89879100	1	1
	19P1A28	15P1A12	Q0	89879100	2	2
	12P1B31	07P1A12	Q0	89879100	2	2
	06P1A12	07P1A12	Q0	89879103	1	1
	01P1A12	02P1A12	Q0	89879103	1	1
	02P1A12	06P1A12	Q0	89879103	2	2
	19P2B02	12P2B01	Q1	89879100	2	2
	15P1B12	07P1B12	Q1	89879100	2	2
	12P2B01	15P1B12	Q1	89879100	1	1
SEE BELOW	> 25P1A11	19P2B02	Q1	89879100	1	1
	12P2B22	15P1A17	Q10	89879100	1	1
	20P2B16	15P2A10	Q10	89879100	1	1
	> 02P1B12	06P1B12	Q1	89879100	2	2
	> 06P1B12	07P1B12	Q1	89879100	1	1
	> 01P1B12	02P1B12	Q1	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
15P1A17	07P1A17	Q10	89879100	2	2
15P2A10	12P2B22	Q10	89879100	2	2
26P1A08	20P2B16	Q10	89879100	2	2
02P1A17	06P1A17	Q10	89879103	2	2
06P1A17	07P1A17	Q10	89879103	1	1
01P1A17	02P1A17	Q10	89879103	1	1
02P1B17	06P1B17	Q11	89879103	2	2
06P1B17	07P1B17	Q11	89879103	1	1
01P1B17	02P1B17	Q11	89879103	1	1
15P1B17	07P1B17	Q11	89879100	2	2
26P1B09	15P1B17	Q11	89879100	1	1
26P2A24	15P1A18	Q12	89879100	1	1
15P1A18	07P1A18	Q12	89879100	2	2
02P1A18	06P1A18	Q12	89879103	2	2
06P1A18	07P1A18	Q12	89879103	1	1
01P1A18	02P1A18	Q12	89879103	1	1
02P1B18	06P1B18	Q13	89879103	2	2
06P1B18	07P1B18	Q13	89879103	1	1
01P1B18	02P1B18	Q13	89879103	1	1
15P1B18	07P1B18	Q13	89879100	2	2
26P2B28	15P1B18	Q13	89879100	1	1
26P2B25	15P1A19	Q14	89879100	1	1
15P1A19	07P1A19	Q14	89879100	2	2
02P1A19	06P1A19	Q14	89879103	2	2
06P1A19	07P1A19	Q14	89879103	1	1
01P1A19	02P1A19	Q14	89879103	1	1
02P1B19	06P1B19	Q15	89879103	2	2
06P1B19	07P1B19	Q15	89879103	1	1
01P1B19	02P1B19	Q15	89879103	1	1
24P1B28	26P2A28	Q15	89879100	1	1
15P1B19	07P1B19	Q15	89879100	2	2
26P2B01	15P1B19	Q15	89879100	1	1
21P1B09	24P1B28	Q15	89879100	2	2
19P2B01	15P1A13	Q2	89879100	1	1
15P1A13	07P1A13	Q2	89879100	2	2
25P1A08	19P2B01	Q2	89879100	2	2
02P1A13	06P1A13	Q2	89879103	2	2
06P1A13	07P1A13	Q2	89879103	1	1
01P1A13	02P1A13	Q2	89879103	1	1
06P1B13	07P1B13	Q3	89879103	1	1
01P1B13	02P1B13	Q3	89879103	1	1
02P1B13	06P1B13	Q3	89879103	2	2
15P1B13	07P1B13	Q3	89879100	2	2
25P1B09	15P1B13	Q3	89879100	1	1
26P1B08	25P1B08	Q30	89879100	2	2
25P1B08	21P1B27	Q30	89879100	1	1
02P1A14	06P1A14	Q4	89879103	2	2
06P1A14	07P1A14	Q4	89879103	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
01P1A14	02P1A14	Q4	89879103	1	1
15P1A14	C7P1A14	Q4	89879100	2	2
25P2A24	20P2B07	Q4	89879100	2	2
20P2B07	15P1A14	Q4	89879100	1	1
20P2B15	15P1B14	Q5	89879100	1	1
25P2B28	20P2B15	Q5	89879100	2	2
15P1B14	C7P1B14	Q5	89879100	2	2
06P1B14	07P1B14	Q5	89879103	1	1
01P1B14	02P1B14	Q5	89879103	1	1
02P1B14	06P1B14	Q5	89879103	2	2
02P1A15	06P1A15	Q6	89879103	2	2
06P1A15	07P1A15	Q6	89879103	1	1
01P1A15	02P1A15	Q6	89879103	1	1
15P1A15	07P1A15	Q6	89879100	2	2
25P2B25	20P2A14	Q6	89879100	2	2
20P2A14	15P1A15	Q6	89879100	1	1
12P2A24	15P1B15	Q7	89879100	1	1
20P2A06	15P2B09	Q7	89879100	1	1
25P2A28	20P2A06	Q7	89879100	2	2
15P1B15	C7P1B15	Q7	89879100	2	2
15P2B09	12P2A24	Q7	89879100	2	2
06P1B15	C7P1B15	Q7	89879103	1	1
01P1B15	02P1B15	Q7	89879103	1	1
02P1B15	06P1B15	Q7	89879103	2	2
02P1A16	06P1A16	Q8	89879103	2	2
06P1A16	07P1A16	Q8	89879103	1	1
01P1A16	02P1A16	Q8	89879103	1	1
15P1A16	07P1A16	Q8	89879100	2	2
15P2A09	12P2B23	Q8	89879100	2	2
26P1B12	20P2B14	Q8	89879100	2	2
20P2B14	15P2A09	Q8	89879100	1	1
12P2B23	15P1A16	Q8	89879100	1	1
12P2A23	15P1B16	Q9	89879100	1	1
20P2A16	15P2B10	Q9	89879100	1	1
26P1A11	20P2A16	Q9	89879100	2	2
15P1B16	07P1B16	Q9	89879100	2	2
15P2B10	12P2A23	Q9	89879100	2	2
06P1B16	07P1B16	Q9	89879103	1	1
01P1B16	02P1B16	Q9	89879103	1	1
02P1B16	06P1B16	Q9	89879103	2	2
19P2B07	17P2B07	R+C+CC	89879100	2	2
19P2B09	18P2A11	R+W+C	89879100	2	2
18P2A11	17P1A11	R+W+C	89879100	1	1
17P2A27	16P2B13	R+W+C+CC	89879100	1	1
19P2B27	17P2A27	R+W+C+CC	89879100	2	2
27P2A20	29P2B27	R/W	89879100	2	2
35P2B27	36P2B27	R/W	89879101	1	1
33P2B27	34P2B27	R/W	89879101	1	1
31P2B27	32P2B27	R/W	89879101	1	1
29P2B27	30P2B27	R/W	89879101	1	1
30P2B27	31P2B27	R/W	89879101	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
34P2B27	35P2B27	R/W	89879101	2	2
32P2B27	33P2B27	R/W	89879101	2	2
12P1A27	11P2A25	RDS*	89879100	1	1
14P1A02	13P1B02	RDTAPE 0	89879100	1	1
13P1B02	11P1A04	RDTAPE 0	89879100	2	2
13P1A03	11P1A02	RDTAPE 1	89879100	2	2
14P1B03	13P1A03	RDTAPE 1	89879100	1	1
14P1B01	13P1A01	RDTAPE 2	89879100	1	1
13P1A01	11P1A05	RDTAPE 2	89879100	2	2
13P1B01	11P1A06	RDTAPE 3	89879100	2	2
14P1A01	13P1B01	RDTAPE 3	89879100	1	1
14P1A06	13P1B06	RDTAPE 4	89879100	1	1
13P1B06	11P1B04	RDTAPE 4	89879100	2	2
13P1A07	11P1B02	RDTAPE 5	89879100	2	2
14P1B07	13P1A07	RDTAPE 5	89879100	1	1
14P1A04	13P1A04	RDTAPE 6	89879100	1	1
13P1A04	11P1A07	RDTAPE 6	89879100	2	2
13P1B04	11P1A08	RDTAPE 7	89879100	2	2
14P1B04	13P1B04	RDTAPE 7	89879100	1	1
17P1B30	16P1A06	READ	89879100	1	1
19P2A11	17P1B30	READ	89879100	2	2
16P1A06	15P2B06	READ	89879100	2	2
19P2B20	17P1A19	READ DATA	89879100	1	1
17P2B15	16P2B17	READ GATE*	89879100	1	1
15P1A21	12P1B29	READ*	89879100	1	1
20P2A04	19P1B02	READ*	89879100	1	1
12P1B29	07P1A21	READ*	89879100	2	2
19P1B02	15P1A21	READ*	89879100	2	2
22P2B02	20P2A04	READ*	89879100	2	2
02P1A21	06P1A21	READ*	89879103	2	2
06P1A21	07P1A21	READ*	89879103	1	1
01P1A21	02P1A21	READ*	89879103	1	1
13P2A17	12P2A13	READY	89879100	2	2
27P2A07	29P2A20	REF*	89879100	2	2
32P2A20	33P2A20	REF*	89879101	2	2
30P2A20	31P2A20	REF*	89879101	2	2
34P2A20	35P2A20	REF*	89879101	2	2
35P2A20	36P2A20	REF*	89879101	1	1
33P2A20	34P2A20	REF*	89879101	1	1
31P2A20	32P2A20	REF*	89879101	1	1
29P2A20	30P2A20	REF*	89879101	1	1
15P1B22	12P2A14	REJECT*	89879100	3	3
02P1B22	06P1B22	REJECT*	89879103	2	2
06P1B22	07P1B22	REJECT*	89879103	1	1
01P1B22	02P1B22	REJECT*	89879103	1	1
19P1B01	15P1B22	REJECT*	89879100	1	1
22P2A24	20P2B13	REJECT*	89879100	1	1
15P1B22	07P1B22	REJECT*	89879100	2	2
20P2B13	19P1B01	REJECT*	89879100	2	2
20P2B12	19P1A03	REPLY*	89879100	2	2
15P1A22	07P1A22	REPLY*	89879100	2	2

	FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
	22P2B25	20P2B12	REPLY*	89879100	1	1	
	19P1A03	15P1A22	REPLY*	89879100	1	1	
	02P1A22	06P1A22	REPLY*	89879103	2	2	
	06P1A22	07P1A22	REPLY*	89879103	1	1	
	01P1A22	02P1A22	REPLY*	89879103	1	1	
	15P1A22	12P2B14	REPLY*	89879100	3	3	
	14P2A29	13P2B17	REQ*	89879100	1	1	
	13P2B17	12P1A17	REQ*	89879100	2	2	
SEE BELOW >	18P1A11	16P1A05	REQUEST*	89879100	2	2	
	15P2B20	15P2B01	RESCTRBSY*	89879100	2	2	
	16P1A27	15P2B20	RESCTRBSY*	89879100	1	1	
	19P2B19	16P1A27	RESET CTR B	89879100	2	2	
	19P2B19	16P1A27	RESET CTR B	89879100	2	2	
	17P1B07	16P1A11	RESUME	89879100	2	2	
	13P2A11	12P2B18	RES1*	89879100	2	2	
	14P1A07	12P1B26	RES1,1*	89879100	2	2	
	13P2A28	12P1B19	RES2*	89879100	2	2	
	12P1B19	11P1A31	RES2*	89879100	1	1	
	14P2B05	13P2A28	RES2*	89879100	1	1	
	08P2B10	14P2B06	REV*	89879104			
	08P2B10	11P2B02	REV*	89879104			
	24P2B15	23P2A19	RE1F	89879100	1	1	
	23P2A26	24P2A27	RE18*	89879100	2	2	
	27P2B28	21P1B22	RGPWR	89879100	2	2	
	33P2A22	27P2B28	RGPWR	89879100	1	1	
	22P2A17	20P1A21	RIND	89879100	1	1	
	12P2A05	11P1B30	RMOT	89879100	1	1	
	14P2A25	12P2B05	RMOT*	89879100	1	1	
	13P1A06	12P2B05	RMOT*	89879100	2	2	
	20P2B04	23P2A29	RNI	89879100	2	2	
	21P1A17	22P1B20	RNI	89879100	2	2	
	20P2B04	21P1A17	RNI	89879100	1	1	
	22P2B04	24P1B08	RNI11*	89879100	1	1	
	22P2B04	23P2B27	RNI11*	89879100	2	2	
	22P2A06	23P2B28	RNI12*	89879100	2	2	
	23P2B28	24P2B30	RNI12*	89879100	1	1	
	23P2B26	24P2A29	RNI21*	89879100	1	1	
	22P1B26	23P2B26	RNI21*	89879100	2	2	
	23P2A25	24P1A05	RNI22*	89879100	1	1	
	24P1A08	22P2A22	RP	89879100	2	2	
	13P2A22	11P2B14	RWLD RWUNLD	89879100	1	1	
	12P2B31	11P2B29	RWLD*	89879100	1	1	
	14P2B15	13P2B26	RWLD*	89879100	1	1	
	13P2B26	12P2B31	RWLD*	89879100	2	2	
	14P2A22	11P2B28	RWUNLD*	89879100	1	1	
	27P2A25	28P2B27	RXA	89879100	2	2	
	24P1B27	23P2A12	R1	89879100	1	1	
	24P1B27	22P1A24	R1	89879100	2	2	
	24P1A28	22P1A23	R2	89879100	2	2	
	24P1A28	23P2B12	R2	89879100	1	1	
	21P2B06	22P1B19	R3	89879100	2	2	
	> 18P2B01	18P1A11	REQUEST*	89879100	3	3	LENGTH 8"

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
22P1B19	24P1A24	R3	89879100	1	1
21P2B06	23P2A28	R3	89879100	1	1
21P1A30	23P2B18	R4	89879100	1	1
22P1B22	24P1B23	R4	89879100	1	1
21P1A30	22P1B22	R4	89879100	2	2
12P1A19	05P1B21	S WRITE*	89879100	2	2
27P1B31	16P1B05	S WRITE*	89879100	2	2
16P1B05	12P1A19	S WRITE*	89879100	1	1
31P2B10	27P1B31	S WRITE*	89879100	1	1
04P1B21	05P1B21	S WRITE*	89879102	2	1
03P1B21	04P1B21	S WRITE*	89879102	1	1
17P2A26	19P1B22	SAMPLE CHEC	89879100	1	1
03P1B23	04P1B23	SA0	89879102	1	1
04P1B23	05P1B23	SA0	89879102	2	1
13P1B05	05P1B23	SA0	89879100	2	2
28P2A24	18P1A02	SA0	89879100	2	2
18P1A02	13P1B05	SA0	89879100	1	1
33P2A19	28P2A24	SA0	89879100	1	1
18P1B03	13P1A23	SA1	89879100	1	1
33P2B19	28P2B25	SA1	89879100	1	1
28P2B25	18P1B03	SA1	89879100	2	2
13P1A23	05P1B24	SA1	89879100	2	2
04P1B24	05P1B24	SA1	89879102	2	1
03P1B24	04P1B24	SA1	89879102	1	1
04P1A25	05P1A25	SA10	89879102	2	1
03P1A25	04P1A25	SA10	89879102	1	1
28P1A26	18P1B02	SA10	89879100	2	2
18P1B02	14P1B05	SA10	89879100	1	1
33P2B05	28P1A26	SA10	89879100	1	1
14P1B05	05P1A25	SA10	89879100	2	2
28P1B21	18P1A03	SA11	89879100	2	2
14P1A23	05P1A26	SA11	89879100	2	2
18P1A03	14P1A23	SA11	89879100	1	1
33P1A23	28P1B21	SA11	89879100	1	1
03P1A26	04P1A26	SA11	89879102	1	1
04P1A26	05P1A26	SA11	89879102	2	1
04P1A27	05P1A27	SA12	89879102	2	1
03P1A27	04P1A27	SA12	89879102	1	1
18P1B01	14P1A08	SA12	89879100	1	1
33P2B06	28P1B27	SA12	89879100	1	1
28P1B27	18P1B01	SA12	89879100	2	2
14P1A08	05P1A27	SA12	89879100	2	2
28P1A31	18P1A04	SA13	89879100	2	2
14P1A26	05P1A28	SA13	89879100	2	2
18P1A04	14P1A26	SA13	89879100	1	1
33P2B10	28P1A31	SA13	89879100	1	1
03P1A28	04P1A28	SA13	89879102	1	1
04P1A28	05P1A28	SA13	89879102	2	1
04P1A30	05P1A30	SA14	89879102	2	1
03P1A30	04P1A30	SA14	89879102	1	1
18P1B04	14P1B09	SA14	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
33P2B09	28P1A30	SA14	89879100	1	1
28P1A30	18P1B04	SA14	89879100	2	2
14P1B09	05P1A30	SA14	89879100	2	2
27P2A01	18P1A01	SA15	89879100	2	2
14P1B25	05P1A31	SA15	89879100	2	2
18P1A01	14P1B25	SA15	89879100	1	1
33P2A12	27P2A01	SA15	89879100	1	1
03P1A31	04P1A31	SA15	89879102	1	1
04P1A31	05P1A31	SA15	89879102	2	1
04P1B25	05P1B25	SA2	89879102	2	1
03P1B25	04P1B25	SA2	89879102	1	1
18P1B08	13P1A05	SA2	89879100	1	1
33P1B02	28P1B01	SA2	89879100	1	1
13P1A05	05P1B25	SA2	89879100	2	2
28P1B01	18P1B08	SA2	89879100	2	2
28P1A06	18P1A08	SA3	89879100	2	2
13P1B23	05P1B26	SA3	89879100	2	2
18P1A08	13P1B23	SA3	89879100	1	1
33P1A10	28P1A06	SA3	89879100	1	1
03P1B26	04P1B26	SA3	89879102	1	1
04P1B26	05P1B26	SA3	89879102	1	1
03P1B27	04P1B27	SA4	89879102	1	1
04P1B27	05P1B27	SA4	89879102	2	1
18P1A09	13P1B08	SA4	89879100	1	1
33P1A13	28P1B09	SA4	89879100	1	1
28P1B09	18P1A09	SA4	89879100	2	2
13P1B08	05P1B27	SA4	89879100	2	2
28P1A09	18P1B09	SA5	89879100	2	2
13P1A26	05P1B28	SA5	89879100	2	2
18P1B09	13P1A26	SA5	89879100	1	1
33P1B12	28P1A09	SA5	89879100	1	1
04P1B28	05P1B28	SA5	89879102	2	1
03P1B28	04P1B28	SA5	89879102	1	1
03P1B30	04P1B30	SA6	89879102	1	1
04P1B30	05P1B30	SA6	89879102	2	1
18P1B06	13P1A09	SA6	89879100	1	1
33P1B22	28P1A21	SA6	89879100	1	1
28P1A21	18P1B06	SA6	89879100	2	2
13P1A09	05P1B30	SA6	89879100	2	2
28P1B23	18P1A06	SA7	89879100	2	2
13P1B25	05P1B31	SA7	89879100	2	2
18P1A06	13P1B25	SA7	89879100	1	1
33P2B03	28P1B23	SA7	89879100	1	1
04P1B31	05P1B31	SA7	89879102	2	1
03P1B31	04P1B31	SA7	89879102	1	1
04P1A23	05P1A23	SA8	89879102	2	1
03P1A23	04P1A23	SA8	89879102	1	1
18P1A07	14P1A05	SA8	89879100	1	1
33P2A10	28P1B30	SA8	89879100	1	1
28P1B30	18P1A07	SA8	89879100	2	2
14P1A05	05P1A23	SA8	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
28P1B29	18P1B07	SA9	89879100	2	2	
14P1A22	05P1A24	SA9	89879100	2	2	
18P1B07	14P1A22	SA9	89879100	1	1	
33P2A09	28P1B29	SA9	89879100	1	1	
03P1A24	04P1A24	SA9	89879102	1	1	
04P1A24	05P1A24	SA9	89879102	2	1	
16P1A04	12P2B25	SCFCD(SCFIM	89879100	1	1	
~~12P2A26~~	~~05P1B19~~	~~SCFCM(PLS)~~	~~89879100~~	~~2~~	~~2~~	Removed by FCO CK676
19P1B27	15P2A24	SCOSE0	89879100	2	2	
19P2A07	15P2B24	SCOSE1	89879100	1	1	
19P1A23	15P2A25	SCOSE2	89879100	2	2	
19P1A22	15P2B25	SCOSE3	89879100	1	1	
16P1B01	12P2A27	SCROD(SCRIM	89879100	1	1	
~~12P2B28~~	~~05P1B15~~	~~SCRCM(PLS)~~	~~89879100~~	~~2~~	~~2~~	Removed by FCO CK676
28P1B03	27P1A01	SD0	89879100	2	2	
13P1A12	05P1A03	SD0	89879100	2	2	
27P1A01	13P1A12	SD0	89879100	1	1	
33P1B04	28P1B03	SD0	89879100	1	1	
18P2B28	13P1A12	SD0	89879100	3	3	
04P1A03	05P1A03	SD0	89879102	2	1	
03P1A03	04P1A03	SD0	89879102	1	1	
03P1B01	04P1B01	SD1	89879102	1	1	
04P1B01	05P1B01	SD1	89879102	2	1	
18P2A27	13P1A10	SD1	89879100	3	3	
27P1A03	13P1A10	SD1	89879100	1	1	
33P1B01	28P1A01	SD1	89879100	1	1	
28P1A01	27P1A03	SD1	89879100	2	2	
13P1A10	05P1B01	SD1	89879100	2	2	
14P1A10	05P1B06	SD10	89879100	2	2	
28P1B20	27P1B18	SD10	89879100	2	2	
27P1B18	14P1A10	SD10	89879100	1	1	
33P1A22	28P1B20	SD10	89879100	1	1	
18P2A30	14P1A10	SD10	89879100	3	3	
04P1B06	05P1B06	SD10	89879102	2	1	
03P1B06	04P1B06	SD10	89879102	1	1	
04P1A05	05P1A05	SD11	89879102	2	1	
03P1A05	04P1A05	SD11	89879102	1	1	
18P2B31	14P1A12	SD11	89879100	3	3	
27P1A18	14P1A12	SD11	89879100	1	1	
33P1A16	28P1A15	SD11	89879100	1	1	
28P1A15	27P1A18	SD11	89879100	2	2	
14P1A12	05P1A05	SD11	89879100	2	2	
28P1A23	27P1A20	SD12	89879100	2	2	
14P1B15	05P1A04	SD12	89879100	2	2	
27P1A20	14P1B15	SD12	89879100	1	1	
33P2B02	28P1A23	SD12	89879100	1	1	
18P2A28	14P1B15	SD12	89879100	3	3	
03P1A04	04P1A04	SD12	89879102	1	1	
04P1A04	05P1A04	SD12	89879102	2	1	
03P1B09	04P1B09	SD13	89879102	1	1	
04P1B09	05P1B09	SD13	89879102	2	1	

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
18P2B29	14P1B26	SD13	89879100	3	3
27P1B23	14P1B26	SD13	89879100	1	1
33P1B21	28P1A20	SD13	89879100	1	1
28P1A20	27P1B23	SD13	89879100	2	2
14P1B26	05P1B09	SD13	89879100	2	2
28P1A19	27P1B22	SD14	89879100	2	2
14P1A15	05P1B10	SD14	89879100	2	2
27P1B22	14P1A15	SD14	89879100	1	1
33P1B18	28P1A19	SD14	89879100	1	1
18P2A29	14P1A15	SD14	89879100	3	3
04P1B10	05P1B10	SD14	89879102	2	1
03P1B10	04P1B10	SD14	89879102	1	1
04P1A11	05P1A11	SD15	89879102	2	1
03P1A11	04P1A11	SD15	89879102	1	1
18P2B30	14P1A14	SD15	89879100	3	3
27P1A19	14P1A14	SD15	89879100	1	1
33P2B04	28P1A24	SD15	89879100	1	1
28P1A24	27P1A19	SD15	89879100	2	2
14P1A14	05P1A11	SD15	89879100	2	2
27P2A21	05P1A18	SD16	89879100	2	2
33P2A18	27P2A21	SD16	89879100	1	1
03P1A18	04P1A18	SD16	89879102	1	1
04P1A18	05P1A18	SD16	89879102	2	1
04P1A20	05P1A20	SD17	89879102	2	1
03P1A20	04P1A20	SD17	89879102	1	1
33P2B15	27P2A18	SD17	89879100	1	1
27P2A18	05P1A20	SD17	89879100	2	2
28P1B04	27P1A05	SD2	89879100	2	2
13P1B10	05P1B02	SD2	89879100	2	2
27P1A05	13P1B10	SD2	89879100	1	1
33P1B06	28P1B04	SD2	89879100	1	1
18P2B26	13P1B10	SD2	89879100	3	3
03P1B02	04P1B02	SD2	89879102	1	1
04P1B02	05P1B02	SD2	89879102	2	1
04P1A06	05P1A06	SD3	89879102	2	1
03P1A06	04P1A06	SD3	89879102	1	1
18P2A25	13P1B12	SD3	89879100	3	3
27P1B06	13P1B12	SD3	89879100	1	1
33P1B08	28P1A05	SD3	89879100	1	1
28P1A05	27P1B06	SD3	89879100	2	2
13P1B12	05P1A06	SD3	89879100	2	2
28P1B08	27P1A07	SD4	89879100	2	2
13P1B15	05P1A07	SD4	89879100	2	2
27P1A07	13P1B15	SD4	89879100	1	1
33P1A12	28P1B08	SD4	89879100	1	1
18P2A23	13P1B15	SD4	89879100	3	3
03P1A07	04P1A07	SD4	89879102	1	1
04P1A07	05P1A07	SD4	89879102	2	1
04P1A01	05P1A01	SD5	89879102	2	1
03P1A01	04P1A01	SD5	89879102	1	1
18P2B24	13P1B13	SD5	89879100	3	3

	FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
	28P1B07	27P1A08	SD5	89879100	2	2	
	13P1B13	05P1A01	SD5	89879100	2	2	
	27P1A08	13P1B13	SD5	89879100	1	1	
	33P1A11	28P1B07	SD5	89879100	1	1	
	27P1A10	13P1A16	SD6	89879100	1	1	
	33P1B10	28P1B06	SD6	89879100	1	1	
	28P1B06	27P1A10	SD6	89879100	2	2	
	13P1A16	05P1A02	SD6	89879100	2	2	
	18P2A24	13P1A16	SD6	89879100	3	3	
	03P1A02	04P1A02	SD6	89879102	1	1	
	04P1A02	05P1A02	SD6	89879102	2	1	
	03P1B03	04P1B03	SD7	89879102	1	1	
	04P1B03	05P1B03	SD7	89879102	2	1	
	18P2B25	13P1A15	SD7	89879100	3	3	
	28P1B05	27P1A12	SD7	89879100	2	2	
	13P1A15	05P1B03	SD7	89879100	2	2	
	27P1A12	13P1A15	SD7	89879100	1	1	
	33P1B09	28P1B05	SD7	89879100	1	1	
	27P1B14	14P1B12	SD8	89879100	1	1	
	33P1B15	28P1B14	SD8	89879100	1	1	
	28P1B14	27P1B14	SD8	89879100	2	2	
	14P1B12	05P1B04	SD8	89879100	2	2	
	18P2B27	14P1B12	SD8	89879100	3	3	
	04P1B04	05P1B04	SD8	89879102	2	1	
	03P1B04	04P1B04	SD8	89879102	1	1	
	03P1B05	04P1B05	SD9	89879102	1	1	
	04P1B05	05P1B05	SD9	89879102	2	1	
	18P2A26	14P1B10	SD9	89879100	3	3	
	28P1B18	27P1B16	SD9	89879100	2	2	
	14P1B10	05P1B05	SD9	89879100	2	2	
	27P1B16	14P1B10	SD9	89879100	1	1	
	33P1B17	28P1B18	SD9	89879100	1	1	
	26P1A22	26P1B22	SE	89879100	1	1	
	22P2A04	26P1A22	SE	89879100	2	2	
	19P1A16	15P2A02	SE.U.PRT.	89879100	2	2	
	18P2A12	17P1A25	SECTOR GATE	89879100	2	2	
SEE BELOW >	18P2A12	16P2B10	SECTOR GATE	89879100	1	1	
	14P1A25	13P1A25	SELA0	89879100	1	1	
	13P1A25	12P2B11	SELA0	89879100	2	2	
	13P1A27	12P2A11	SELA1	89879100	2	2	
	14P1A27	13P1A27	SELA1	89879100	1	1	
	19P1A04	18P1B05	SELD.UTPI10	89879100	1	1	
	18P1B05	15P2A01	SELD.UTPI10	89879100	2	2	
	14P2B02	11P2B07	SEOP*	89879100	1	1	
	16P2A06	15P2A26	SEOSC1*	89879100	1	1	
	16P2A04	15P2B26	SEOSC2*	89879100	1	1	
	16P2A02	15P2A27	SEOSC3*	89879100	1	1	
	16P2A01	15P2B27	SEOSC4*	89879100	1	1	
	19P2B29	16P1A25	SET ALARM*	89879100	1	1	
	19P2A14	16P1A30	SET CTR SEE	89879100	2	2	
>	19P2B15	17P1A12	SECTOR GATE	89879100	3	3	LENGTH 9"

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
17P1A12	16P1A18	SET NEED*	89879100	1	1
18P1A19	15P2B04	SET.ADDR.ER	89879100	2	2
25P1B22	22P2B05	SFL	89879100	1	1
08P1A20	11P2B10	SFM*	89879104		
08P1A20	14P2B18	SFM*	89879104		
23P2A14	25P1A22	SGL	89879100	1	1
21P2A13	23P2B22	SG1*	89879100	1	1
20P2B01	21P2A13	SG1*	89879100	2	2
23P2B13	22P2A16	SHADR	89879100	1	1
26P2B11	25P2B26	SHAL	89879100	1	1
26P2B26	25P2B05	SHAM	89879100	2	2
22P1B06	24P2B11	SHI	89879100	1	1
18P2B16	17P2A22	SHIFT CLOCK	89879100	2	2
18P2B05	17P1A31	SHIFT-BUUF1	89879100	2	2
17P1A31	16P1B09	SHIFT-BUUF1	89879100	1	1
24P1B19	25P1A17	SIL	89879100	2	2
22P2A09	26P1A17	SIM	89879100	1	1
22P2A30	21P1B04	SKT	89879100	1	1
21P1A07	20P1A10	SLK*	89879100	1	1
22P1B24	20P1B24	SLS	89879100	1	1
18P2A18	16P1A13	SMPX0	89879100	2	2
18P2B19	16P1B14	SMPX1	89879100	2	2
22P2B26	24P2A12	SO	89879100	2	2
25P2A08	26P2A08	SO	89879100	2	2
24P2A12	25P2A08	SO	89879100	1	1
33P1B13	28P1A12	SPBM*	89879100	1	1
28P1A12	22P1A25	SPBM*	89879100	2	2
12P2A18	05P1B14	SPI*	89879100	2	2
27P1B29	16P1A03	SPI*	89879100	2	2
16P1A03	12P2A18	SPI*	89879100	1	1
31P2A10	27P1B29	SPI*	89879100	1	1
04P1B14	05P1B14	SPI*	89879102	2	1
03P1B14	04P1B14	SPI*	89879102	1	1
04P1A15	05P1A15	SRQ*	89879102	2	1
03P1A15	04P1A15	SRQ*	89879102	1	1
16P1A01	12P1A20	SRQ*	89879100	1	1
33P2B20	27P2A28	SRQ*	89879100	1	1
12P1A20	05P1A15	SRQ*	89879100	2	2
27P2A28	16P1A01	SRQ*	89879100	2	2
12P1A14	05P1A13	SRSM*	89879100	2	2
27P2B18	16P1A10	SRSM*	89879100	2	2
16P1A10	12P1A14	SRSM*	89879100	1	1
33P2B16	27P2B18	SRSM*	89879100	1	1
03P1A13	04P1A13	SRSM*	89879102	1	1
04P1A13	05P1A13	SRSM*	89879102	2	1
03P1B12	04P1B12	SS*	89879102	1	1
04P1B12	05P1B12	SS*	89879102	2	1
33P2B17	27P2A19	SS*	89879100	1	1
16P1B03	12P1B22	SS*	89879100	1	1
12P1B22	05P1B12	SS*	89879100	2	2
27P2A19	16P1B03	SS*	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
23P1A19	21P1B15	SS1	89879100	2	2
14P2B13	12P1B02	STO.PAR.ERR	89879100	1	1
14P2B31	12P1A21	STOP DIST*	89879100	1	1
14P2B16	12P1B27	STOP*	89879100	1	1
21P1A16	20P1A31	STOPCS*	89879100	1	1
14P1A21	13P1B22	STRBUF*	89879100	1	1
13P1B22	12P2A09	STRBUF*	89879100	2	2
13P2B04	12P2B13	STRCC	89879100	2	2
13P2A10	12P2B09	STRINT	89879100	2	2
14P2B07	12P2A01	STRMF	89879100	1	1
29P2A07	27P2A12	STROBE*	89879100	2	2
30P2A07	31P2A07	STROBE*	89879101	2	2
34P2A07	35P2A07	STROBE*	89879101	2	2
32P2A07	33P2A07	STROBE*	89879101	2	2
35P2A07	36P2A07	STROBE*	89879101	1	1
33P2A07	34P2A07	STROBE*	89879101	1	1
31P2A07	32P2A07	STROBE*	89879101	1	1
29P2A07	30P2A07	STROBE*	89879101	1	1
13P2A07	12P2A15	STRUS	89879100	2	2
14P1A31	13P2A07	STRUS	89879100	1	1
12P1A13	11P2A05	STWCRC*	89879100	1	1
04P1B17	05P1B17	SVIO*	89879102	2	1
03P1B17	04P1B17	SVIO*	89879102	1	1
27P2B24	19P1A09	SVIO*	89879100	2	2
12P1A01	05P1B17	SVIO*	89879100	2	2
33P2B18	27P2B24	SVIO*	89879100	1	1
19P1A09	12P1A01	SVIO*	89879100	1	1
21P1B17	20P1A23	SWEEP*	89879100	1	1
28P2A20	27P2B08	SXA*	89879100	2	2
28P2B28	27P2A11	SXP*	89879100	2	2
26P2B09	25P2B09	S1	89879100	2	2
25P2B09	24P2A18	S1	89879100	1	1
18P2A17	17P1A04	S11	89879100	2	2
18P2A16	17P1B03	S15	89879100	2	2
26P1A26	25P1A26	S2	89879100	2	2
25P1A26	24P2A17	S2	89879100	1	1
25P1B25	24P2A13	S3	89879100	1	1
26P1B25	25P1B25	S3	89879100	2	2
16P1A20	15P2A21	T.E.D AUTOL	89879100	2	2
15P1A09	07P1A09	T.P.	89879100	2	2
21P2B28	15P1A09	T.P.	89879100	1	1
25P1B02	21P2A15	TAOL	89879100	2	2
26P1B02	21P2B16	TAOM	89879100	2	2
16P1A21	15P2B19	TAS EXT.	89879100	1	1
25P1A04	21P2B17	TA1L	89879100	1	1
26P1A04	21P2A17	TA1M	89879100	1	1
25P1B04	21P2B20	TA2L	89879100	2	2
26P1B04	21P2A21	TA2M	89879100	2	2
17P1B28	16P1A14	TD1	89879100	2	2
16P1A14	15P2B22	TD1	89879100	1	1
19P2A15	16P1A31	TD1*	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
16P1B20	15P2B29	TD2	89879100	1	1
18P2B10	17P1A20	TD2	89879100	1	1
17P1A20	16P1B20	TD2	89879100	2	2
19P2A16	16P1B26	TD2*	89879100	1	1
19P2B14	18P2B02	TD3	89879100	1	1
17P2A23	16P1A17	TD3	89879100	1	1
18P2B02	17P2A23	TD3	89879100	2	2
17P2B11	16P1A12	TD4	89879100	2	2
19P2A23	18P2B03	TD4	89879100	2	2
18P2B03	17P2B11	TD4	89879100	1	1
21P2A24	20P1A08	TMSW*	89879100	1	1
13P2B24	12P2A30	TM1	89879100	2	2
13P2B16	12P2B29	TM3	89879100	2	2
12P2B29	08P2B23	TM3	89879100	1	1
14P2A19	13P2B16	TM3	89879100	1	1
06P1A09	07P1A09	TP	89879103	1	1
01P1A09	02P1A09	TP	89879103	1	1
02P1A09	06P1A09	TP	89879103	2	2
14P1A03	13P1B03	TRANS*	89879100	1	1
13P1B03	12P1B07	TRANS*	89879100	2	2
14P2A28	13P2B28	TT READY	89879100	1	1
14P2B17	12P1B13	TTBUSY*	89879100	1	1
14P2A24	13P2A19	TTDENSTAT*	89879100	1	1
11P2B11	14P1B06	TTONLINE*	89879104		
14P2A23	13P2B19	TTREADY*	89879100	1	1
24P2A09	22P1A14	T3	89879100	1	1
24P2B06	22P1B16	T4	89879100	2	2
16P1B04	15P2A06	ULT.SRC.PRO	89879100	1	1
12P1A08	11P1A27	UPPER	89879100	2	2
14P1B02	12P1B03	UPPX1*	89879100	2	2
14P2A09	12P2B03	USA	89879100	1	1
14P2B09	13P2B27	US0	89879100	1	1
14P2B11	13P2A27	US1	89879100	1	1
16P2A14	15P2B11	US1*	89879100	1	1
16P2A09	15P2A11	US2*	89879100	1	1
16P2A08	15P2A04	US3*	89879100	1	1
16P2A07	15P2B08	US4*	89879100	1	1
21P2A31	20P1B01	VCC	89879104		
27P2A30	23P1A01	VCC2	89879100	1	1
23P1A06	21P2B15	VIO*	89879100	1	1
29P2A16	20P2B27	VSS	89879100	1	1
19P1A27	17P1A27	W.CKWD*	89879100	2	2
18P2A19	17P1B19	W+C	89879100	2	2
17P1B19	16P1A02	W+C	89879100	1	1
19P2A01	18P2A19	W+C	89879100	1	1
24P2A26	23P1A14	WA	89879100	2	2
19P2B22	17P2A28	WA-ADR	89879100	1	1
11P2B27	10P2A07	WCLK	89879100	1	1
09P2A07	08P1A01	WCLK	89879100	1	1
10P2A07	09P2A07	WCLK	89879100	2	2
13P2B09	12P1A12	WDS SHIFTED	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
27P1A30	24P1B12	WE*	89879100	2	2	
24P1B12	22P1B25	WE*	89879100	1	1	
31P2B06	27P1A30	WE*	89879100	1	1	
02P1A20	06P1A20	WEZ*	89879103	2	2	
06P1A20	07P1A20	WEZ*	89879103	1	1	
01P1A20	02P1A20	WEZ*	89879103	1	1	
12P2A25	07P1A20	WEZ*	89879100	2	2	LENGTH 10"
21P2B30	15P1A20	WEZ*	89879100	2	2	LENGTH 11"
21P2B30	12P2A25	WEZ*	89879100	3	3	LENGTH 7"
21P2B30	19P1A02	WEZ*	89879100	1	1	LENGTH 14"
25P2B29	21P2A07	WEZL*	89879100	1	1	
26P2B29	21P1A13	WEZM*	89879100	1	1	
26P2B29	20P2A15	WEZM*	89879100	2	2	
08P1A21	12P1B24	WFM	89879104			
12P1B24	10P2B16	WFM/TM*	89879100	2	2	
14P2B25	12P1B24	WFM/TM*	89879100	1	1	
10P2B16	11P2B01	WFM/TM*	89879100	1	1	
24P2B03	23P2B23	WM	89879100	1	1	
12P2B04	11P1A10	WMOT	89879100	2	2	
14P2B24	12P2B06	WMOT*	89879100	1	1	
24P1B04	23P1A13	WP	89879100	1	1	
24P1B29	23P1B12	WQ	89879100	1	1	
14P1A30	13P2A08	WRENABLE	89879100	2	2	
13P2A05	08P1B18	WREQUEST*	89879100	2	2	
14P2A17	13P2A05	WREQUEST*	89879100	1	1	
19P2B13	17P2B28	WRITE	89879100	2	2	
13P2A06	12P1B10	WRITE CLOCK	89879100	2	2	
13P2A06	11P2B19	WRITE CLOCK	89879100	1	1	
17P1B27	16P2B16	WRITE DATA*	89879100	1	1	
18P2A21	16P1B08	WRITE ENABL	89879100	2	2	
17P2B23	16P2B22	WRITE GATE*	89879100	1	1	
15P1B21	12P1B30	WRITE*	89879100	1	1	
20P2B06	19P2B31	WRITE*	89879100	1	1	
12P1B30	07P1B21	WRITE*	89879100	2	2	
19P2B31	15P1B21	WRITE*	89879100	2	2	
22P2B01	20P2B06	WRITE*	89879100	2	2	
02P1B21	06P1B21	WRITE*	89879103	2	2	
06P1B21	07P1B21	WRITE*	89879103	1	1	
01P1B21	02P1B21	WRITE*	89879103	1	1	
21P1A11	24P1A11	WRQ	89879100	1	1	
21P1A11	22P2A10	WRQ	89879100	2	2	
13P1A08	11P1A22	WRTAPE 0	89879100	2	2	
13P1A22	11P1A21	WRTAPE 1	89879100	2	2	
14P1B27	11P1A26	WRTAPE 10	89879100	2	2	
14P1A11	11P1B27	WRTAPE 11	89879100	2	2	
14P1B16	11P1B21	WRTAPE 12	89879100	2	2	
14P1A13	11P1B20	WRTAPE 13	89879100	2	2	
14P1A16	11P1B25	WRTAPE 14	89879100	2	2	
14P1A24	11P1B24	WRTAPE 15	89879100	2	2	
13P1B27	11P1B26	WRTAPE 2	89879100	2	2	
13P1A11	11P1A25	WRTAPE 3	89879100	2	2	

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
13P1B16	11P1A20	WRTAPE 4	89879100	2	2
13P1A14	11P1A19	WRTAPE 5	89879100	2	2
13P1A17	11P1A24	WRTAPE 6	89879100	2	2
13P1A24	11P1A23	WRTAPE 7	89879100	2	2
14P1B08	11P1B23	WRTAPE 8	89879100	2	2
14P1B21	11P1B22	WRTAPE 9	89879100	2	2
23P1B10	22P2A15	WXL	89879100	2	2
24P1A12	22P1B28	WXL1*	89879100	2	2
23P1B15	22P2A07	WXM	89879100	1	1
24P2B13	23P2A01	W9A*	89879100	2	2
22P2A05	25P1A18	XEZ	89879100	2	2
25P1A18	26P1A18	XEZ	89879100	1	1
25P2A17	21P1A03	XGQL	89879100	1	1
26P2A17	21P1A02	XGQM	89879100	1	1
25P1A15	23P1A10	XLCK	89879100	2	2
26P1A15	23P1B09	XMCK	89879100	1	1
26P2A19	23P1A02	XSEL7M	89879100	2	2
26P2B18	21P1B02	XSQM	89879100	2	2
26P1A09	25P1A09	XTADD	89879100	2	2
25P1A09	24P1A09	XTADD	89879100	1	1
24P2B31	25P2A25	XTAUGL	89879100	1	1
24P2A20	26P2A25	XTAUGM	89879100	2	2
24P1B22	23P1B26	X15	89879100	1	1
23P1B26	22P2B17	X15	89879100	2	2
24P1B22	21P1A08	X15	89879100	2	2
23P1A12	25P1A20	YCK	89879100	2	2
25P1A20	26P1A20	YCK	89879100	1	1
25P1B17	26P1B17	YTAUG	89879100	1	1
23P1A30	25P1B17	YTAUG	89879100	2	2
26P2A09	22P2B23	ZITSH	89879100	1	1
19P1B05	17P2A07	010	89879100	2	2
17P2A25	16P1B16	011	89879100	2	2
22P1B03	24P1B31	02*	89879100	1	1
23P2A30	24P2B01	03*	89879100	1	1
21P1B07	22P2B07	03*	89879100	1	1
22P2B07	24P2B01	03*	89879100	2	2
22P1A22	21P2B19	1E	89879100	2	2
28P2A28	29P2A30	1K0*	89879100	2	2
34P2A30	35P2A30	1K0*	89879101	2	2
32P2A30	33P2A30	1K0*	89879101	2	2
30P2A30	31P2A30	1K0*	89879101	2	2
29P2A30	30P2A30	1K0*	89879101	1	1
31P2A30	32P2A30	1K0*	89879101	1	1
35P2A30	36P2A30	1K0*	89879101	1	1
33P2A30	34P2A30	1K0*	89879101	1	1
35P2B29	36P2B29	1K1*	89879101	1	1
33P2B29	34P2B29	1K1*	89879101	1	1
31P2B29	32P2B29	1K1*	89879101	1	1
29P2B29	30P2B29	1K1*	89879101	1	1
30P2B29	31P2B29	1K1*	89879101	2	2
34P2B29	35P2B29	1K1*	89879101	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
32P2B29	33P2B29	1K1*	89879101	2	2
28P2B30	29P2B29	1K1*	89879100	2	2
28P2A26	29P2B24	1K2*	89879100	2	2
32P2B24	33P2B24	1K2*	89879101	2	2
30P2B24	31P2B24	1K2*	89879101	2	2
34P2B24	35P2B24	1K2*	89879101	2	2
35P2B24	36P2B24	1K2*	89879101	1	1
33P2B24	34P2B24	1K2*	89879101	1	1
31P2B24	32P2B24	1K2*	89879101	1	1
29P2B24	30P2B24	1K2*	89879101	1	1
35P2A24	36P2A24	1K3*	89879101	1	1
33P2A24	34P2A24	1K3*	89879101	1	1
31P2A24	32P2A24	1K3*	89879101	1	1
29P2A24	30P2A24	1K3*	89879101	1	1
30P2A24	31P2A24	1K3*	89879101	2	2
34P2A24	35P2A24	1K3*	89879101	2	2
32P2A24	33P2A24	1K3*	89879101	2	2
28P2A27	29P2A24	1K3*	89879100	2	2
17P1B31	16P1B12	16BITS.011	89879100	2	2
13P2B05	11P1B05	1600	89879100	2	2
11P1B05	12P1B18	1600	89879100	1	1
13P2B12	11P1A30	2FWC	89879100	2	2
27P2A06	26P2A29	32KW	89879100	2	2
23P2B08	22P2A02	32KW	89879100	2	2
21P1A12	05P1A21	32KW	89879100	2	2
03P1A21	04P1A21	32KW	89879102	1	1
04P1A21	05P1A21	32KW	89879102	2	1
22P2A02	21P1A17	32KW	89879100	3	3
21P1A12	20P1B04	32KW	89879100	1	1
26P2A29	23P2BC8	32KW	89879100	1	1
33P2A13	27P2A06	32KW	89879100	1	1
21P2B26	27P2B30	32M	89879100	1	1
12P2A29	11P2B05	4MHZ	89879100	1	1
13P2A24	08P2A21	75IPS	89879100	2	2
13P2A26	11P1A28	9T	89879100	2	2
14P2A21	13P2A26	9T	89879100	1	1
13P1B24	12P1A30	9T*	89879100	2	2

TABLE 9-4.b WIRE LIST AB 107/AB 108 BACKPLANE
(in card slot order)

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
01P1A01	02P1A01	0A5*	89879103	1	1
01P1A02	02P1A02	0A6*	89879103	1	1
01P1A03	02P1A03	0A0*	89879103	1	1
01P1A04	02P1A04	0A12*	89879103	1	1
01P1A05	02P1A05	0A11*	89879103	1	1
01P1A06	02P1A06	0A3*	89879103	1	1
01P1A07	02P1A07	0A4*	89879103	1	1
01P1A09	02P1A09	TP	89879103	1	1
01P1A11	02P1A11	0A15*	89879103	1	1
01P1A12	02P1A12	Q0	89879103	1	1
01P1A13	02P1A13	Q2	89879103	1	1
01P1A14	02P1A14	Q4	89879103	1	1
01P1A15	02P1A15	Q6	89879103	1	1
01P1A16	02P1A16	Q8	89879103	1	1
01P1A17	02P1A17	Q10	89879103	1	1
01P1A18	02P1A18	Q12	89879103	1	1
01P1A19	02P1A19	Q14	89879103	1	1
01P1A20	02P1A20	WEZ*	89879103	1	1
01P1A21	02P1A21	READ*	89879103	1	1
01P1A22	02P1A22	REPLY*	89879103	1	1
01P1A23	02P1A23	PRTM*	89879103	1	1
01P1B01	02P1B01	0A1*	89879103	1	1
01P1B02	02P1B02	0A2*	89879103	1	1
01P1B03	02P1B03	0A7*	89879103	1	1
01P1B04	02P1B04	0A8*	89879103	1	1
01P1B05	02P1B05	0A9*	89879103	1	1
01P1B06	02P1B06	0A10*	89879103	1	1
01P1B07	02P1B07	CHI*	89879103	1	1
01P1B09	02P1B09	0A13*	89879103	1	1
01P1B10	02P1B10	0A14*	89879103	1	1
01P1B12	02P1B12	Q1	89879103	1	1
01P1B13	02P1B13	Q3	89879103	1	1
01P1B14	02P1B14	Q5	89879103	1	1
01P1B15	02P1B15	Q7	89879103	1	1
01P1B16	02P1B16	Q9	89879103	1	1
01P1B17	02P1B17	Q11	89879103	1	1
01P1B18	02P1B18	Q13	89879103	1	1
01P1B19	02P1B19	Q15	89879103	1	1
01P1B21	02P1B21	WRITE*	89879103	1	1
01P1B22	02P1B22	REJECT*	89879103	1	1
01P1B23	02P1B23	MC*	89879103	1	1
01P1B23	03P1A09	MC*	89879100	2	2
02P1A01	01P1A01	0A5*	89879103	1	1
02P1A01	06P1A01	0A5*	89879103	2	2
02P1A02	06P1A02	0A6*	89879103	2	2
02P1A02	01P1A02	0A6*	89879103	1	1
02P1A03	01P1A03	0A0*	89879103	1	1
02P1A03	06P1A03	0A0*	89879103	2	2
02P1A04	01P1A04	0A12*	89879103	1	1
02P1A04	06P1A04	0A12*	89879103	2	2
02P1A05	01P1A05	0A11*	89879103	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
02P1A05	C6P1A05	OA11*	89879103	2	2
02P1A06	01P1A06	OA3*	89879103	1	1
02P1A06	C6P1AC6	OA3*	89879103	2	2
02P1A07	06P1A07	OA4*	89879103	2	2
02P1A07	01P1A07	OA4*	89879103	1	1
02P1A09	06P1A09	TP	89879103	2	2
02P1A09	01P1A09	TP	89879103	1	1
02P1A11	01P1A11	OA15*	89879103	1	1
02P1A11	C6P1A11	OA15*	89879103	2	2
02P1A12	01P1A12	Q0	89879103	1	1
02P1A12	06P1A12	Q0	89879103	2	2
02P1A13	C6P1A13	Q2	89879103	2	2
02P1A13	01P1A13	Q2	89879103	1	1
02P1A14	C1P1A14	Q4	89879103	1	1
02P1A14	C6P1A14	Q4	89879103	2	2
02P1A15	06P1A15	Q6	89879103	2	2
02P1A15	01P1A15	Q6	89879103	1	1
02P1A16	06P1A16	Q8	89879103	2	2
02P1A16	01P1A16	Q8	89879103	1	1
02P1A17	01P1A17	Q10	89879103	1	1
02P1A17	06P1A17	C10	89879103	2	2
02P1A18	01P1A18	Q12	89879103	1	1
02P1A18	06P1A18	Q12	89879103	2	2
02P1A19	06P1A19	C14	89879103	2	2
02P1A19	01P1A19	C14	89879103	1	1
02P1A20	06P1A20	WEZ*	89879103	2	2
02P1A20	01P1A20	WEZ*	89879103	1	1
02P1A21	06P1A21	READ*	89879103	2	2
02P1A21	01P1A21	READ*	89879103	1	1
02P1A22	01P1A22	REPLY*	89879103	1	1
02P1A22	C6P1A22	REPLY*	89879103	2	2
02P1A23	06P1A23	PRTM*	89879103	2	2
02P1A23	01P1A23	PRTM*	89879103	1	1
02P1B01	01P1B01	OA1*	89879103	1	1
02P1B01	06P1B01	OA1*	89879103	2	2
02P1B02	01P1B02	OA2*	89879103	1	1
02P1B02	06P1B02	OA2*	89879103	2	2
02P1B03	06P1B03	CA7*	89879103	2	2
02P1B03	01P1B03	OA7*	89879103	1	1
02P1B04	01P1B04	OA8*	89879103	1	1
02P1B04	06P1B04	OA8*	89879103	2	2
02P1B05	01P1B05	OA9*	89879103	1	1
02P1B05	06P1B05	CA9*	89879103	2	2
02P1B06	C6P1B06	OA10*	89879103	2	2
02P1B06	01P1B06	OA10*	89879103	1	1
02P1B07	01P1B07	CHI*	89879103	1	1
02P1B07	C6P1BC7	CHI*	89879103	2	2
02P1B09	01P1B09	OA13*	89879103	1	1
02P1B09	06P1B09	CA13*	89879103	2	2
02P1B10	06P1B10	OA14*	89879103	2	2
02P1B10	01P1B10	OA14*	89879103	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
02P1B12	01P1B12	Q4	89879103	1	1
02P1B12	06P1B12	Q1	89879103	2	2
02P1B13	06P1B13	Q3	89879103	2	2
02P1B13	01P1B13	Q3	89879103	1	1
02P1B14	06P1B14	Q5	89879103	2	2
02P1B14	01P1B14	Q5	89879103	1	1
02P1B15	C6P1B15	Q7	89879103	2	2
02P1B15	01P1B15	Q7	89879103	1	1
02P1B16	01P1B16	Q9	89879103	1	1
02P1B16	06P1B16	Q9	89879103	2	2
02P1B17	01P1B17	Q11	89879103	1	1
02P1B17	06P1B17	Q11	89879103	2	2
02P1B18	06P1B18	Q13	89879103	2	2
02P1B18	01P1B18	Q13	89879103	1	1
02P1B19	06P1B19	Q15	89879103	2	2
02P1B19	01P1B19	Q15	89879103	1	1
02P1B21	06P1B21	WRITE*	89879103	2	2
02P1B21	01P1B21	WRITE*	89879103	1	1
02P1B22	01P1B22	REJECT*	89879103	1	1
02P1B22	06P1B22	REJECT*	89879103	2	2
02P1B23	06P1B23	MC*	89879103	2	2
02P1B23	01P1B23	MC*	89879103	1	1
03P1A01	04P1A01	SD5	89879102	1	1
03P1A02	04P1A02	SD6	89879102	1	1
03P1A03	04P1A03	SD0	89879102	1	1
03P1A04	04P1A04	SD12	89879102	1	1
03P1A05	04P1A05	SD11	89879102	1	1
03P1A06	04P1A06	SD3	89879102	1	1
03P1A07	04P1A07	SD4	89879102	1	1
03P1A09	04P1A09	MC*	89879102	1	1
03P1A09	01P1B23	MC*	89879100	2	2
03P1A11	04P1A11	SD15	89879102	1	1
03P1A13	04P1A13	SRSM*	89879102	1	1
03P1A15	04P1A15	SRQ*	89879102	1	1
03P1A17	04P1A17	PEL*	89879102	1	1
03P1A18	04P1A18	SD16	89879102	1	1
03P1A20	04P1A20	SD17	89879102	1	1
03P1A21	04P1A21	32KW	89879102	1	1
03P1A23	04P1A23	SA8	89879102	1	1
03P1A24	04P1A24	SA9	89879102	1	1
03P1A25	04P1A25	SA10	89879102	1	1
03P1A26	04P1A26	SA11	89879102	1	1
03P1A27	04P1A27	SA12	89879102	1	1
03P1A28	04P1A28	SA13	89879102	1	1
03P1A30	04P1A30	SA14	89879102	1	1
03P1A31	04P1A31	SA15	89879102	1	1
03P1B01	04P1B01	SD1	89879102	1	1
03P1B02	04P1B02	SD2	89879102	1	1
03P1B03	04P1B03	SD7	89879102	1	1
03P1B04	04P1B04	SD8	89879102	1	1
03P1B05	04P1B05	SD9	89879102	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
03P1B06	04P1B06	SD10	89879102	1	1
03P1B09	C4P1B09	SD13	89879102	1	1
03P1B10	04P1B10	SD14	89879102	1	1
03P1B12	04P1B12	SS*	89879102	1	1
03P1B14	04P1B14	SPI*	89879102	1	1
03P1B17	04P1B17	SVIO*	89879102	1	1
03P1B18	04P1B18	AUTOLOAD	89879102	1	1
03P1B21	04P1B21	S WRITE*	89879102	1	1
03P1B23	04P1B23	SA0	89879102	1	1
03P1B24	04P1B24	SA1	89879102	1	1
03P1B25	04P1B25	SA2	89879102	1	1
03P1B26	04P1B26	SA3	89879102	1	1
03P1B27	C4P1B27	SA4	89879102	1	1
03P1B28	04P1B28	SA5	89879102	1	1
03P1B30	04P1B30	SA6	89879102	1	1
03P1B31	04P1B31	SA7	89879102	1	1
04P1A01	03P1A01	SD5	89879102	1	1
04P1A01	05P1A01	SD5	89879102	2	1
04P1A02	03P1A02	SD6	89879102	1	1
04P1A02	05P1A02	SD6	89879102	2	1
04P1A03	05P1A03	SD0	89879102	2	1
04P1A03	03P1A03	SD0	89879102	1	1
04P1A04	03P1A04	SD12	89879102	1	1
04P1A04	05P1A04	SD12	89879102	2	1
04P1A05	03P1A05	SD11	89879102	1	1
04P1A05	05P1A05	SD11	89879102	2	1
04P1A06	05P1A06	SD3	89879102	2	1
04P1A06	03P1A06	SD3	89879102	1	1
04P1A07	03P1A07	SD4	89879102	1	1
04P1A07	05P1A07	SD4	89879102	2	1
04P1A09	03P1A09	MC*	89879102	1	1
04P1A09	05P1A09	MC*	89879102	2	1
04P1A11	03P1A11	SD15	89879102	1	1
04P1A11	05P1A11	SD15	89879102	2	1
04P1A13	05P1A13	SRSM*	89879102	2	1
04P1A13	03P1A13	SRSM*	89879102	1	1
04P1A15	03P1A15	SRQ*	89879102	1	1
04P1A15	05P1A15	SRQ*	89879102	2	1
04P1A17	03P1A17	PEL*	89879102	1	1
04P1A17	05P1A17	PEL*	89879102	2	1
04P1A18	C5P1A18	SD16	89879102	2	1
04P1A18	03P1A18	SD16	89879102	1	1
04P1A20	05P1A20	SD17	89879102	2	1
04P1A20	03P1A20	SD17	89879102	1	1
04P1A21	03P1A21	32KW	89879102	1	1
04P1A21	05P1A21	32KW	89879102	2	1
04P1A23	05P1A23	SA8	89879102	2	1
04P1A23	03P1A23	SA8	89879102	1	1
04P1A24	05P1A24	SA9	89879102	2	1
04P1A24	03P1A24	SA9	89879102	1	1
04P1A25	05P1A25	SA10	89879102	2	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
04P1A25	03P1A25	SA10	89879102	1	1
04P1A26	05P1A26	SA11	89879102	2	1
04P1A26	03P1A26	SA11	89879102	1	1
04P1A27	05P1A27	SA12	89879102	2	1
04P1A27	03P1A27	SA12	89879102	1	1
04P1A28	03P1A28	SA13	89879102	1	1
04P1A28	05P1A28	SA13	89879102	2	1
04P1A30	05P1A30	SA14	89879102	2	1
04P1A30	03P1A30	SA14	89879102	1	1
04P1A31	03P1A31	SA15	89879102	1	1
04P1A31	05P1A31	SA15	89879102	2	1
04P1B01	03P1B01	SD1	89879102	1	1
04P1B01	05P1B01	SD1	89879102	2	1
04P1B02	05P1B02	SD2	89879102	2	1
04P1B02	03P1B02	SD2	89879102	1	1
04P1B03	05P1B03	SD7	89879102	2	1
04P1B03	03P1B03	SD7	89879102	1	1
04P1B04	03P1B04	SD8	89879102	1	1
04P1B04	05P1B04	SD8	89879102	2	1
04P1B05	05P1B05	SD9	89879102	2	1
04P1B05	03P1B05	SD9	89879102	1	1
04P1B06	05P1B06	SD10	89879102	2	1
04P1B06	03P1B06	SD10	89879102	1	1
04P1B09	05P1B09	SD13	89879102	2	1
04P1B09	03P1B09	SD13	89879102	1	1
04P1B10	03P1B10	SD14	89879102	1	1
04P1B10	05P1B10	SD14	89879102	2	1
04P1B12	05P1B12	SS*	89879102	2	1
04P1B12	03P1B12	SS*	89879102	1	1
04P1B14	03P1B14	SPI*	89879102	1	1
04P1B14	05P1B14	SPI*	89879102	2	1
04P1B17	05P1B17	SVIO*	89879102	2	1
04P1B17	03P1B17	SVIO*	89879102	1	1
04P1B18	05P1B18	AUTOLOAD	89879102	2	1
04P1B18	03P1B18	AUTOLOAD	89879102	1	1
04P1B21	05P1B21	S WRITE*	89879102	2	1
04P1B21	03P1B21	S WRITE*	89879102	1	1
04P1B23	03P1B23	SA0	89879102	1	1
04P1B23	05P1B23	SA0	89879102	2	1
04P1B24	05P1B24	SA1	89879102	2	1
04P1B24	03P1B24	SA1	89879102	1	1
04P1B25	05P1B25	SA2	89879102	2	1
04P1B25	03P1B25	SA2	89879102	1	1
04P1B26	03P1B26	SA3	89879102	1	1
04P1B26	05P1B26	SA3	89879102	1	1
04P1B27	03P1B27	SA4	89879102	1	1
04P1B27	05P1B27	SA4	89879102	2	1
04P1B28	05P1B28	SA5	89879102	2	1
04P1B28	03P1B28	SA5	89879102	1	1
04P1B30	05P1B30	SA6	89879102	2	1
04P1B30	03P1B30	SA6	89879102	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
04P1B31	05P1B31	SA7	89879102	2	1
04P1B31	03P1B31	SA7	89879102	1	1
05P1A01	04P1A01	SD5	89879102	1	2
05P1A01	13P1B13	SD5	89879100	2	2
05P1A02	13P1A16	SD6	89879100	2	2
05P1A02	04P1A02	SD6	89879102	1	2
05P1A03	04P1A03	SD0	89879102	1	2
05P1A03	13P1A12	SD0	89879100	2	2
05P1A04	14P1B15	SD12	89879100	2	2
05P1A04	04P1A04	SD12	89879102	1	2
05P1A05	04P1A05	SD11	89879102	1	2
05P1A05	14P1A12	SD11	89879100	2	2
05P1A06	13P1B12	SD3	89879100	2	2
05P1A06	04P1A06	SD3	89879102	1	2
05P1A07	04P1A07	SD4	89879102	1	2
05P1A07	13P1B15	SD4	89879100	2	2
05P1A09	04P1A09	MC*	89879102	1	2
05P1A11	04P1A11	SD15	89879102	1	2
05P1A11	14P1A14	SD15	89879100	2	2
05P1A13	12P1A14	SRSM*	89879100	2	2
05P1A13	04P1A13	SRSM*	89879102	1	2
05P1A15	04P1A15	SRQ*	89879102	1	2
05P1A15	12P1A20	SRQ*	89879100	2	2
05P1A17	12P1B01	PEL*	89879100	2	2
05P1A17	04P1A17	PEL*	89879102	1	2
05P1A18	04P1A18	SD16	89879102	1	2
05P1A18	27P2A21	SD16	89879100	2	2
05P1A20	27P2A18	SD17	89879100	2	2
05P1A20	04P1A20	SD17	89879102	1	2
05P1A21	04P1A21	32KW	89879102	1	2
05P1A21	21P1A12	32KW	89879100	2	2
05P1A23	14P1A05	SA8	89879100	2	2
05P1A23	04P1A23	SA8	89879102	1	2
05P1A24	04P1A24	SA9	89879102	1	2
05P1A24	14P1A22	SA9	89879100	2	2
05P1A25	14P1B05	SA10	89879100	2	2
05P1A25	04P1A25	SA10	89879102	1	2
05P1A26	04P1A26	SA11	89879102	1	2
05P1A26	14P1A23	SA11	89879100	2	2
05P1A27	14P1A08	SA12	89879100	2	2
05P1A27	04P1A27	SA12	89879102	1	2
05P1A28	04P1A28	SA13	89879102	1	2
05P1A28	14P1A26	SA13	89879100	2	2
05P1A30	14P1B09	SA14	89879100	2	2
05P1A30	04P1A30	SA14	89879102	1	2
05P1A31	04P1A31	SA15	89879102	1	2
05P1A31	14P1B25	SA15	89879100	2	2
05P1B01	13P1A10	SD1	89879100	2	2
05P1B01	04P1B01	SD1	89879102	1	2
05P1B02	04P1B02	SD2	89879102	1	2
05P1B02	13P1B10	SD2	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
05P1B03	13P1A15	SD7	89879100	2	2	
05P1B03	04P1B03	SD7	89879102	1	2	
05P1B04	04P1B04	SD8	89879102	1	2	
05P1B04	14P1B12	SD8	89879100	2	2	
05P1B05	14P1B10	SD9	89879100	2	2	
05P1B05	C4P1B05	SD9	89879102	1	2	
05P1B06	04P1B06	SD10	89879102	1	2	
05P1B06	14P1A10	SD10	89879100	2	2	
05P1B09	14P1B26	SD13	89879100	2	2	
05P1B09	04P1B09	SD13	89879102	1	2	
05P1B10	04P1B10	SD14	89879102	1	2	
05P1B10	14P1A15	SD14	89879100	2	2	
05P1B12	12P1B22	SS*	89879100	2	2	
05P1B12	04P1B12	SS*	89879102	1	2	
05P1B14	04P1B14	SPI*	89879102	1	2	
05P1B14	12P2A18	SPI*	89879100	2	2	
~~05P1B16~~	~~12P2B28~~	~~SCRFM(BUS)~~	~~89879100~~	~~2~~	~~2~~	Removed by FCO CK676
05P1B17	12P1A01	SVIO*	89879100	2	2	
05P1B17	04P1B17	SVIC*	89879102	1	2	
05P1B18	04P1B18	ALTOLCAD	89879102	1	2	
05P1B18	10P1B19	AUTOLOAD	89879100	3	3	
05P1B18	10P1B20	AUTOLOAD	89879100	2	2	
~~05P1B19~~	~~12P2A26~~	~~SCFFM(BLS)~~	~~89879100~~	~~2~~	~~2~~	Removed by FCO CK676
05P1B21	12P1A19	S WRITE*	89879100	2	2	
05P1B21	04P1B21	S WRITE*	89879102	1	2	
05P1B23	04P1B23	SA0	89879102	1	2	
05P1B23	13P1B05	SA0	89879100	2	2	
05P1B24	13P1A23	SA1	89879100	2	2	
05P1B24	04P1B24	SA1	89879102	1	2	
05P1B25	04P1B25	SA2	89879102	1	2	
05P1B25	13P1A05	SA2	89879100	2	2	
05P1B26	13P1B23	SA3	89879100	2	2	
05P1B26	04P1B26	SA3	89879102	1	1	
05P1B27	04P1B27	SA4	89879102	1	2	
05P1B27	13P1B08	SA4	89879100	2	2	
05P1B28	13P1A26	SA5	89879100	2	2	
05P1B28	04P1B28	SA5	89879102	1	2	
05P1B30	04P1B30	SA6	89879102	1	2	
05P1B30	13P1A09	SA6	89879100	2	2	
05P1B31	13P1B25	SA7	89879100	2	2	
05P1B31	04P1B31	SA7	89879102	1	2	
06P1A01	07P1A01	DA5*	89879103	1	1	
06P1A01	02P1A01	DA5*	89879103	2	2	
06P1A02	07P1A02	DA6*	89879103	1	1	
06P1A02	02P1A02	DA6*	89879103	2	2	
06P1A03	07P1A03	DA0*	89879103	1	1	
06P1A03	02P1A03	DA0*	89879103	2	2	
06P1A04	02P1A04	DA12*	89879103	2	2	
06P1A04	07P1A04	DA12*	89879103	1	1	
06P1A05	02P1A05	DA11*	89879103	2	2	
06P1A05	C7P1A05	DA11*	89879103	1	1	

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
06P1A06	07P1A06	0A3*	89879103	1	1
06P1A06	02P1AC6	0A3*	89879103	2	2
06P1A07	C7P1A07	0A4*	89879103	1	1
06P1A07	02P1A07	0A4*	89879103	2	2
06P1A09	C7P1A09	TP	89879103	1	1
06P1A09	02P1A09	TP	89879103	2	2
06P1A11	C7P1A11	0A15*	89879103	1	1
06P1A11	02P1A11	0A15*	89879103	2	2
06P1A12	02P1A12	Q0	89879103	2	2
06P1A12	C7P1A12	QC	89879103	1	1
06P1A13	07P1A13	Q2	89879103	1	1
06P1A13	02P1A13	Q2	89879103	2	2
06P1A14	02P1A14	Q4	89879103	2	2
06P1A14	07P1A14	Q4	89879103	1	1
06P1A15	C7P1A15	Q6	89879103	1	1
06P1A15	02P1A15	Q6	89879103	2	2
06P1A16	07P1A16	Q8	89879103	1	1
06P1A16	02P1A16	Q8	89879103	2	2
06P1A17	02P1A17	Q10	89879103	2	2
06P1A17	07P1A17	Q10	89879103	1	1
06P1A18	C7P1A18	Q12	89879103	1	1
06P1A18	02P1A18	Q12	89879103	2	2
06P1A19	02P1A19	Q14	89879103	2	2
06P1A19	07P1A19	Q14	89879103	1	1
06P1A20	02P1A20	WEZ*	89879103	2	2
06P1A20	07P1A20	WEZ*	89879103	1	1
06P1A21	C7P1A21	READ*	89879103	1	1
06P1A21	02P1A21	READ*	89879103	2	2
06P1A22	02P1A22	REPLY*	89879103	2	2
06P1A22	C7P1A22	REPLY*	89879103	1	1
06P1A23	07P1A23	PRTM*	89879103	1	1
06P1A23	02P1A23	PRTM*	89879103	2	2
06P1B01	07P1B01	0A1*	89879103	1	1
06P1B01	02P1B01	0A1*	89879103	2	2
06P1B02	02P1B02	0A2*	89879103	2	2
06P1B02	07P1B02	0A2*	89879103	1	1
06P1B03	02P1B03	0A7*	89879103	2	2
06P1B03	07P1B03	0A7*	89879103	1	1
06P1B04	02P1B04	0A8*	89879103	2	2
06P1B04	07P1B04	0A8*	89879103	1	1
06P1B05	02P1B05	0A9*	89879103	2	2
06P1B05	07P1B05	0A9*	89879103	1	1
06P1B06	C7P1B06	0A10*	89879103	1	1
06P1B06	02P1B06	0A10*	89879103	2	2
06P1B07	02P1B07	CHI*	89879103	2	2
06P1B07	07P1B07	CHI*	89879103	1	1
06P1B09	C7P1B09	0A13*	89879103	1	1
06P1B09	02P1B09	0A13*	89879103	2	2
06P1B10	C7P1B10	0A14*	89879103	1	1
06P1B10	02P1B10	0A14*	89879103	2	2
06P1B12	02P1B12	Q4	89879103	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
06P1B12	07P1B12	Q1	89879103	1	1
06P1B13	07P1B13	Q3	89879103	1	1
06P1B13	02P1B13	Q3	89879103	2	2
06P1B14	02P1B14	Q5	89879103	2	2
06P1B14	07P1B14	Q5	89879103	1	1
06P1B15	02P1B15	Q7	89879103	2	2
06P1B15	07P1B15	Q7	89879103	1	1
06P1B16	07P1B16	Q9	89879103	1	1
06P1B16	02P1B16	Q9	89879103	2	2
06P1B17	07P1B17	Q11	89879103	1	1
06P1B17	02P1B17	Q11	89879103	2	2
06P1B18	02P1B18	Q13	89879103	2	2
06P1B18	07P1B18	Q13	89879103	1	1
06P1B19	07P1B19	Q15	89879103	1	1
06P1B19	02P1B19	Q15	89879103	2	2
06P1B21	02P1B21	WRITE*	89879103	2	2
06P1B21	07P1B21	WRITE*	89879103	1	1
06P1B22	02P1B22	REJECT*	89879103	2	2
06P1B22	07P1B22	REJECT*	89879103	1	1
06P1B23	02P1B23	MC*	89879103	2	2
06P1B23	07P1B23	MC*	89879103	1	1
07P1A01	06P1A01	DA5*	89879103	1	1
07P1A01	13P1B19	DA5*	89879100	2	2
07P1A02	13P1A19	DA6*	89879100	2	2
07P1A02	06P1A02	DA6*	89879103	1	1
07P1A03	06P1A03	DA0*	89879103	1	1
07P1A03	13P1B29	DA0*	89879100	2	2
07P1A04	14P1B19	DA12*	89879100	2	2
07P1A04	06P1A04	DA12*	89879103	1	1
07P1A05	06P1A05	DA11*	89879103	1	1
07P1A05	14P1A20	DA11*	89879100	2	2
07P1A06	13P1B21	DA3*	89879100	2	2
07P1A06	06P1A06	DA3*	89879103	1	1
07P1A07	06P1A07	DA4*	89879103	1	1
07P1A07	13P1A20	DA4*	89879100	2	2
07P1A09	15P1A09	T.P.	89879100	2	2
07P1A09	06P1A09	TP	89879103	1	1
07P1A11	06P1A11	DA15*	89879103	1	1
07P1A11	14P1A19	DA15*	89879100	2	2
07P1A12	12P1B31	Q0	89879100	2	2
07P1A12	06P1A12	Q0	89879103	1	1
07P1A13	06P1A13	Q2	89879103	1	1
07P1A13	15P1A13	Q2	89879100	2	2
07P1A14	15P1A14	Q4	89879100	2	2
07P1A14	06P1A14	Q4	89879103	1	1
07P1A15	06P1A15	Q6	89879103	1	1
07P1A15	15P1A15	Q6	89879100	2	2
07P1A16	15P1A16	Q8	89879100	2	2
07P1A16	06P1A16	Q8	89879103	1	1
07P1A17	06P1A17	Q10	89879103	1	1
07P1A17	15P1A17	Q10	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
07P1A18	15P1A18	Q12	89879100	2	2
07P1A18	06P1A18	Q12	89879103	1	1
C7P1A19	06P1A19	Q14	89879103	1	1
07P1A19	15P1A19	Q14	89879100	2	2
07P1A20	12P2A25	WEZ*	89879100	2	2
07P1A20	06P1A20	WEZ*	89879103	1	1
07P1A21	06P1A21	READ*	89879103	1	1
07P1A21	12P1B29	READ*	89879100	2	2
07P1A22	15P1A22	REPLY*	89879100	2	2
07P1A22	06P1A22	REPLY*	89879103	1	1
07P1A23	06P1A23	PRTM*	89879103	1	1
07P1A23	12P2A19	PRTAQ*	89879100	3	3
07P1B01	06P1B01	DA1*	89879103	1	1
C7P1B01	13P1A30	DA1*	89879100	2	2
07P1B02	13P1A21	DA2*	89879100	2	2
07P1B02	06P1B02	DA2*	89879103	1	1
07P1B03	06P1B03	DA7*	89879103	1	1
07P1B03	13P1B20	DA7*	89879100	2	2
07P1B04	14P1B29	DA8*	89879100	2	2
07P1B04	C6P1B04	DA8*	89879103	1	1
07P1B05	C6P1B05	DA9*	89879103	1	1
07P1B05	14P1B22	DA9*	89879100	2	2
07P1B06	14P1B20	DA10*	89879100	2	2
07P1B06	06P1B06	DA10*	89879103	1	1
07P1B07	06P1B07	CHI*	89879103	1	1
07P1B07	12P1B21	CHI*	89879100	2	2
07P1B09	14P1A18	DA13*	89879100	2	2
07P1B09	06P1B09	DA13*	89879103	1	1
07P1B10	06P1B10	DA14*	89879103	1	1
07P1B10	14P1B18	DA14*	89879100	2	2
07P1B12	15P1B12	Q1	89879100	2	2
07P1B12	06P1B12	Q4	89879103	1	1
07P1B13	06P1B13	Q3	89879103	1	1
07P1B13	15P1B13	Q3	89879100	2	2
07P1B14	15P1B14	Q5	89879100	2	2
07P1B14	06P1B14	Q5	89879103	1	1
07P1B15	C6P1B15	Q7	89879103	1	1
07P1B15	15P1B15	Q7	89879100	2	2
07P1B16	15P1B16	Q9	89879100	2	2
07P1B16	06P1B16	Q9	89879103	1	1
07P1B17	06P1B17	Q11	89879103	1	1
07P1B17	15P1B17	Q11	89879100	2	2
07P1B18	15P1B18	Q13	89879100	2	2
07P1B18	06P1B18	Q13	89879103	1	1
07P1B19	06P1B19	Q15	89879103	1	1
07P1B19	15P1B19	Q15	89879100	2	2
07P1B21	12P1B30	WRITE*	89879100	2	2
07P1B21	06P1B21	WRITE*	89879103	1	1
07P1B22	06P1B22	REJECT*	89879103	1	1
07P1B22	15P1B22	REJECT*	89879100	2	2
07P1B23	15P1B23	MC*	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
07P1B23	06P1B23	MC*	89879103	1	1
08P1A01	09P2A07	WCLK	89879100	1	1
08P1A02	12P1A28	PWRQ	89879100	2	2
08P1A03	13P1B31	PE FNABLE	89879100	2	2
08P1A06	09P1A17	ABONE	89879100	2	2
08P1A07	14P2A30	PWID	89879100	1	1
08P1A10	11P2B26	PWRESET	89879100	1	1
08P1A11	09P2A06	AB CLOCKOUT	89879100	2	2
08P1A12	09P2A22	AB TOG	89879100	2	2
08P1A13	12P1B12	PWRQSHIFTED	89879100	2	2
08P1A14	09P1B30	AB RENABLE*	89879100	2	2
08P1A15	12P1B09	BUFF2FL*WMO	89879100	1	1
08P1A17	10P2A05	AWRES(1-4)	89879100	1	1
08P1A19	09P2A26	AB DATA	89879100	2	2
08P1A20	11P2B10	SFM*	89879104		
08P1A20	14P2B18	SFM*	89879104		
08P1A21	12P1B24	WFM	89879104		
08P1A22	09P1A11	AB LOZ	89879100	1	1
08P1A23	10P2A10	ANOENV(2)	89879100	1	1
08P1A24	14P2B14	ID ABORT*	89879100	1	1
08P1A26	09P1B24	012	89879100	1	1
08P1A27	14P2B20	PRBOT	89879100	1	1
08P1A28	09P2A05	B WRES(1-4)	89879100	2	2
08P1A30	09P2A25	B NOENV(1)	89879100	2	2
08P1A31	10P1A24	A POSTAMBLE	89879100	2	2
08P1B02	12P1B25	PE START	89879104		
08P1B02	13P2B06	PE START	89879100	2	2
08P1B12	09P2B09	ABWRES(5)	89879100	1	1
08P1B13	13P2A30	PECLOCK*	89879100	2	2
08P1B18	13P2A05	WREQUEST*	89879100	2	2
08P1B22	12P2B17	GC128	89879104		
08P1B23	09P1B27	PRFB	89879104		
08P1B25	10P1A16	ANOENV(3)	89879100	2	2
08P1B26	10P1A26	AENV(5)	89879100	2	2
08P1B27	10P1B25	ANOENV(5)	89879100	2	2
08P1B29	09P1A28	AB DOT	89879100	2	2
08P1B30	10P2B07	A POSTAMBLE	89879100	1	1
08P1B31	09P2B07	B POSTABLEF	89879100	2	2
08P2A01	10P2A25	A NOENV(1)	89879100	2	2
08P2A02	10P2A09	AENV(2)	89879100	2	2
08P2A04	10P1B03	AENV(4)	89879100	1	1
08P2A05	11P1B29	PE PARERR*	89879100	2	2
08P2A07	10P1B26	A.SKEWOVF G	89879100	2	2
08P2A08	11P2A01	PSFM*	89879100	1	1
08P2A09	09P1A18	AB PRESET	89879100	2	2
08P2A10	09P2B30	B READY F	89879100	2	2
08P2A11	10P2B30	A READY F	89879100	1	1
08P2A12	10P1A07	ANODROPOUT(	89879100	1	1
08P2A13	10P1A27	ASYNC(4)	89879100	1	1
08P2A14	13P2A29	PECHARCLK	89879100	2	2
08P2A15	10P2A02	AC2	89879100	1	1
08P2A16	09P1A04	AB DEN	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
08P2A17	10P2B02	AC1*	89879100	2	2
08P2A18	14P2A01	PE EOP*	89879100	1	1
08P2A19	10P2BC5	ACNEG*	89879100	1	1
08P2A21	13P2A24	75IPS	89879100	2	2
08P2A22	09P1A31	01*	89879100	1	1
08P2A23	11P2B25	PRSTROBE	89879100	1	1
08P2A24	13P2A21	AL2	89879100	2	2
08P2A26	09P2A21	PRTY EN B1*	89879100	2	2
08P2A27	10P1B02	PRTY GN A4*	89879100	1	1
08P2A28	10P2A08	PRTY GN A2*	89879100	1	1
08P2A30	09P1A13	PRTY GN B3*	89879100	2	2
08P2B01	09P1A03	B NOENV(4)	89879100	2	2
08P2B02	09P1A16	B NOENV(3)	89879100	2	2
08P2B03	09P2A10	B NOENV(2)	89879100	2	2
08P2B04	10P1A03	ANOENV(4)	89879100	1	1
08P2B05	10P2A24	AENV(1)	89879100	1	1
08P2B06	09P2A13	AB PARITY	89879100	1	1
08P2B07	09P2B06	B SKEWOVF F	89879100	2	2
08P2B08	10P2B06	A.SKEWOVF F	89879100	1	1
08P2B09	13P1B30	PE LOST CAT	89879100	2	2
08P2B10	11P2B02	REV*	89879104		
08P2B10	14P2B06	REV*	89879104		
08P2B11	10P2A04	A READY G	89879100	2	2
08P2B12	13P2B08	PE WORNING	89879100	2	2
08P2B13	10P2A11	ASYNC(2)	89879104		
08P2B14	09P2A01	BS1*	89879100	2	2
08P2B15	09P2A02	BC2	89879100	2	2
08P2B16	09P1B02	PRTY GN B4*	89879100	2	2
08P2B17	09P2B02	BC1*	89879100	2	2
08P2B19	10P2A29	ACNEF*	89879100	2	2
08P2B20	09P2A29	BCNEF*	89879100	2	2
08P2B23	12P2B29	TM3	89879100	1	1
08P2B24	12P1A06	POSTAMBLE	89879104		
08P2B26	09P1A30	02*	89879100	1	1
08P2B27	10P1A25	PRTY GN A5*	89879100	2	2
08P2B28	10P1A13	PRTY GN A3*	89879100	2	2
08P2B29	10P2A21	PRTY GN A1*	89879100	2	2
08P2B30	C9P2A08	PRTY GN B2*	89879100	2	2
09P1A01	09P1B11	GND	89879104		
09P1A02	11P2B13	PWOUT 2	89879100	1	1
09P1A03	08P2B01	B NOENV(4)	89879100	2	2
09P1A04	10P1A04	AB DEN	89879100	2	2
09P1A04	08P2A16	AB DEN	89879100	1	1
09P1A05	11P1B16	PWDIN 2	89879100	2	2
09P1A11	08P1A22	AB LOZ	89879100	1	1
09P1A11	10P1A11	AB LOZ	89879100	2	2
09P1A12	11P1A12	PRIN 6	89879100	2	2
09P1A13	08P2A30	PRTY GN B3*	89879100	2	2
09P1A16	08P2B02	B NOENV(3)	89879100	2	2
09P1A17	10P1A17	ABCNE	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
09P1A17	C8P1A06	ABCNE	89879100	2	2	
09P1A18	10P1A18	AB PRESET	89879100	1	1	
09P1A18	C8P2A09	AB PRESET	89879100	2	2	
09P1A20	11P1A15	PWDIN 4	89879100	2	2	
09P1A21	11P1B07	PRDOUT 3	89879100	2	2	
09P1A23	11P1B15	PRIN 3	89879100	1	1	
09P1A28	10P1A28	AB DOT	89879100	1	1	
09P1A28	08P1B29	AB DOT	89879100	2	2	
09P1A30	C8P2B26	D2*	89879100	1	1	
09P1A30	10P1A30	D2*	89879100	2	2	
09P1A31	10P1A31	D1*	89879100	2	2	
09P1A31	08P2A22	D1*	89879100	1	1	
09P1B01	10P1B01	PC2	89879100	1	1	
09P1B02	08P2B16	PRTY GN B4*	89879100	2	2	
09P1B06	11P1B08	PRDOUT 6	89879100	2	2	
09P1B11	09P1A01	GND	89879104			
09P1B23	11P2B20	PWOUT 4	89879100	1	1	
09P1B24	08P1A26	D12	89879100	1	1	
09P1B24	10P1B24	D12	89879100	2	2	
09P1B27	C8P1B23	PRFB	89879104			
09P1B27	10P1B27	PRFB	89879100	2	2	
09P1B30	08P1A14	AB RENABLE*	89879100	2	2	
09P1B30	10P1B30	AB RENABLE*	89879100	1	1	
09P2A01	08P2B14	BS1*	89879100	2	2	
09P2A02	C8P2B15	BC2	89879100	2	2	
09P2A05	C8P1A28	B WRES(1-4)	89879100	2	2	
09P2A06	10P2A06	AB CLOCKOUT	89879100	1	1	
09P2A06	08P1A11	AB CLOCKOUT	89879100	2	2	
09P2A07	C8P1A01	WCLK	89879100	1	1	
09P2A07	10P2A07	WCLK	89879100	2	2	
09P2A08	C8P2B30	PRTY GN B2*	89879100	2	2	
09P2A10	08P2B03	B NOENV(2)	89879100	2	2	
09P2A12	11P1B03	PRDOUT 4	89879100	2	2	
09P2A13	C8P2B06	AB PARITY	89879100	1	1	
09P2A13	10P2A13	AB PARITY	89879100	2	2	
09P2A19	11P1B13	PRIN 4	89879100	2	2	
09P2A21	08P2A26	PRTY EN B1*	89879100	2	2	
09P2A22	10P2A22	AB TOG	89879100	1	1	
09P2A22	08P1A12	AB TOG	89879100	2	2	
09P2A25	08P1A30	B NOENV(1)	89879100	2	2	
09P2A26	10P2A26	AB DATA	89879100	1	1	
09P2A26	08P1A19	AB DATA	89879100	2	2	
09P2A27	11P1B19	PWDIN 6	89879100	2	2	
09P2A28	11P1B06	PRDOUT 2	89879100	2	2	
09P2A29	C8P2B20	BCNEF*	89879100	2	2	
09P2B01	10P2A01	BS0*		1	1	←
09P2B02	08P2B17	BC1*	89879100	2	2	
09P2B06	C8P2B07	B SKEWCVF F	89879100	2	2	
09P2B07	08P1B31	B POSTABLEF	89879100	2	2	
09P2B09	08P1B12	ABWRES(5)	89879100	1	1	
09P2B09	10P2B09	ABWRES(5)	89879100	2	2	

	FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
	09P2B10	11P2A13	PWOUT 3	89879100	1	1
	09P2B12	11P1B10	PWDIN 3	89879100	2	2
	09P2B23	11P2B24	PWOUT 6	89879100	1	1
	09P2B26	11P1A14	PRIN 2	89879100	2	2
	09P2B30	C8P2A10	B READY F	89879100	2	2
→	10P2A01	09P2B01	AS1*		1	1
	10P1A01	13P2B07	PC 1600*	89879100	2	2
	10P1A02	11P2B09	PWOUT 0	89879100	1	1
	10P1A03	08P2B04	ANDENV(4)	89879100	1	1
	10P1A04	09P1A04	AB DEN	89879100	2	2
	10P1A05	11P1A16	PWDIN 0	89879100	2	2
	10P1A07	08P2A12	ANODROPOUT(	89879100	1	1
	10P1A10	11P2B04	PRINP	89879100	1	1
	10P1A11	09P1A11	AB LOZ	89879100	2	2
	10P1A12	11P1A13	PRIN 5	89879100	1	1
	10P1A13	C8P2B28	PRTY GN A3*	89879100	2	2
	10P1A16	08P1B25	ANDENV(3)	89879100	2	2
	10P1A17	09P1A17	ABCNE	89879100	1	1
	10P1A18	09P1A18	AB PRESET	89879100	1	1
	10P1A20	11P1A09	PWDIN 1	89879100	2	2
	10P1A21	11P1B09	PRDOUT 7	89879100	2	2
	10P1A23	11P1B14	PRIN 7	89879100	1	1
	10P1A24	08P1A31	A PCSTAMBLE	89879100	2	2
	10P1A25	08P2B27	PRTY GN A5*	89879100	2	2
	10P1A26	08P1B26	AENV(5)	89879100	2	2
	10P1A27	08P2A13	ASYNC(4)	89879100	1	1
	10P1A28	09P1A28	AB DOT	89879100	1	1
	10P1A30	09P1A30	02*	89879100	2	2
	10P1A31	09P1A31	01*	89879100	2	2
	10P1B01	09P1B01	PC2	89879100	1	1
	10P1B02	08P2A27	PRTY GN A4*	89879100	1	1
	10P1B03	08P2A04	AENV(4)	89879100	1	1
	10P1B06	11P1B01	PRDOUT5	89879100	2	2
	10P1B19	20P1A01	AUTOLOAD	89879100	1	1
	10P1B19	05P1B18	AUTOLOAD	89879100	3	3
	10P1B20	16P2B08	AUTOLOAD	89879100	1	1
	10P1B20	05P1B18	AUTOLOAD	89879100	2	2
	10P1B23	11P2B08	PWOUT 1	89879100	1	1
	10P1B24	09P1B24	012	89879100	2	2
	10P1B25	08P1B27	ANDENV(5)	89879100	2	2
	10P1B26	08P2A07	A.SKEWDVF G	89879100	2	2
	10P1B27	09P1B27	PRFB	89879100	2	2
	10P1B28	10P2B01	NDDROPOUT	89879104		
	10P1B30	09P1B30	AB RENABLE*	89879100	1	1
	10P2A02	08P2A15	AC2	89879100	1	1
	10P2A04	08P2B11	A READY G	89879100	2	2
	10P2A05	08P1A17	AWRES(1-4)	89879100	1	1
	10P2A06	09P2A06	AB CLOCKOUT	89879100	1	1
	10P2A07	11P2B27	WCLK	89879100	1	1
	10P2A07	09P2A07	WCLK	89879100	2	2
	10P2A08	C8P2A28	PRTY GN A2*	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
10P2A09	08P2A02	AENV(2)	89879100	2	2
10P2A10	08P1A23	ANDENV(2)	89879100	1	1
10P2A11	08P2B13	ASYNC(2)	89879104		
10P2A12	11P1A01	PRDOUT 1	89879100	2	2
10P2A13	09P2A13	AB PARITY	89879100	2	2
10P2A19	11P1B12	PRIN 1	89879100	1	1
10P2A21	08P2B29	PRTY GN A1*	89879100	2	2
10P2A22	09P2A22	AB TOG	89879100	1	1
10P2A24	08P2B05	AENV(1)	89879100	1	1
10P2A25	08P2A01	A NOENV(1)	89879100	2	2
10P2A26	09P2A26	AB DATA	89879100	1	1
10P2A27	11P1B17	PWDIN 5	89879100	2	2
10P2A28	11P1A03	PRDOUT 0	89879100	2	2
10P2A29	08P2B19	ACNEF*	89879100	2	2
10P2B01	10P1B28	NODROPOUT	89879104		
10P2B02	08P2A17	AC1*	89879100	2	2
10P2B03	11P1B18	PWDINP	89879100	2	2
10P2B05	08P2A19	ACNEG*	89879100	1	1
10P2B06	08P2B08	A.SKEWOVF F	89879100	1	1
10P2B07	08P1B30	A POSTAMBLE	89879100	1	1
10P2B08	11P2B23	PWOUTP	89879100	1	1
10P2B09	09P2B09	ABWRES(5)	89879100	2	2
10P2B10	11P2B22	PWOUT 7	89879100	1	1
10P2B12	11P1A18	PWDIN 7	89879100	2	2
10P2B16	11P2B01	WFM/TM*	89879100	1	1
10P2B16	12P1B24	WFM/TM*	89879100	2	2
10P2B23	11P2B18	PWOUT 5	89879100	1	1
10P2B26	11P1A11	PRIN 0	89879100	2	2
10P2B30	08P2A11	A READY F	89879100	1	1
11P1A01	10P2A12	PRDOUT 1	89879100	2	2
11P1A02	13P1A03	RDTAPE 1	89879100	2	2
11P1A03	10P2A28	PRDOUT 0	89879100	2	2
11P1A04	13P1B02	RDTAPE 0	89879100	2	2
11P1A05	13P1A01	RDTAPE 2	89879100	2	2
11P1A06	13P1B01	RDTAPE 3	89879100	2	2
11P1A07	13P1A04	RDTAPE 6	89879100	2	2
11P1A08	13P1B04	RDTAPE 7	89879100	2	2
11P1A09	10P1A20	PWDIN 1	89879100	2	2
11P1A10	12P2B04	WMOT	89879100	2	2
11P1A11	10P2B26	PRIN 0	89879100	2	2
11P1A12	09P1A12	PRIN 6	89879100	2	2
11P1A13	10P1A12	PRIN 5	89879100	1	1
11P1A14	09P2B26	PRIN 2	89879100	2	2
11P1A15	09P1A20	PWDIN 4	89879100	2	2
11P1A16	10P1A05	PWDIN 0	89879100	2	2
11P1A17	13P2A14	BCD	89879100	2	2
11P1A18	10P2B12	PWDIN 7	89879100	2	2
11P1A19	13P1A14	WRTAPE 5	89879100	2	2
11P1A20	13P1B16	WRTAPE 4	89879100	2	2
11P1A21	13P1A22	WRTAPE 1	89879100	2	2
11P1A22	13P1A08	WRTAPE 0	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
11P1A23	13P1A24	WRTAPE 7	89879100	2	2
11P1A24	13P1A17	WRTAPE 6	89879100	2	2
11P1A25	13P1A11	WRTAPE 3	89879100	2	2
11P1A26	14P1B27	WRTAPE 10	89879100	2	2
11P1A27	12P1A08	UPPER	89879100	2	2
11P1A28	13P2A26	9T	89879100	2	2
11P1A30	13P2B12	2FWC	89879100	2	2
11P1A31	12P1B19	RES2*	89879100	1	1
11P1B01	10P1B06	PRDOUT5	89879100	2	2
11P1B02	13P1A07	RDTAPE 5	89879100	2	2
11P1B03	09P2A12	PRDOUT 4	89879100	2	2
11P1B04	13P1B06	RDTAPE 4	89879100	2	2
11P1B05	13P2B05	1600	89879100	2	2
11P1B05	12P1B18	1600	89879100	1	1
11P1B06	09P2A28	PRDOUT 2	89879100	2	2
11P1B07	09P1A21	PRDOUT 3	89879100	2	2
11P1B08	09P1B06	PRDOUT 6	89879100	2	2
11P1B09	10P1A21	PRDOUT 7	89879100	2	2
11P1B10	09P2B12	PWDIN 3	89879100	2	2
11P1B12	10P2A19	PRIN 1	89879100	1	1
11P1B13	09P2A19	PRIN 4	89879100	2	2
11P1B14	10P1A23	PRIN 7	89879100	1	1
11P1B15	09P1A23	PRIN 3	89879100	1	1
11P1B16	09P1A05	PWDIN 2	89879100	2	2
11P1B17	10P2A27	PWDIN 5	89879100	2	2
11P1B18	10P2B03	PWDINP	89879100	2	2
11P1B19	09P2A27	PWDIN 6	89879100	2	2
11P1B20	14P1A13	WRTAPE 13	89879100	2	2
11P1B21	14P1B16	WRTAPE 12	89879100	2	2
11P1B22	14P1B21	WRTAPE 9	89879100	2	2
11P1B23	14P1B08	WRTAPE 8	89879100	2	2
11P1B24	14P1A24	WRTAPE 15	89879100	2	2
11P1B25	14P1A16	WRTAPE 14	89879100	2	2
11P1B26	13P1B27	WRTAPE 2	89879100	2	2
11P1B27	14P1A11	WRTAPE 11	89879100	2	2
11P1B28	14P2B03	FILL	89879100	1	1
11P1B29	08P2A05	PE PARERR*	89879100	2	2
11P1B30	12P2A05	RMOT	89879100	1	1
11P1B31	12P1B06	A/D	89879100	1	1
11P2A01	08P2A08	PSFM*	89879100	1	1
11P2A05	12P1A13	STWCRC*	89879100	1	1
11P2A13	09P2B10	PWOUT 3	89879100	1	1
11P2A18	12P1A26	LRCC STATE	89879100	1	1
11P2A25	12P1A27	RDS*	89879100	1	1
11P2B01	10P2B16	WFM/TM*	89879100	1	1
11P2B02	08P2B10	REV*	89879104		
11P2B03	12P2A08	EOP	89879100	1	1
11P2B04	10P1A10	PRINP	89879100	1	1
11P2B05	12P2A29	4MHZ	89879100	1	1
11P2B07	14P2B02	SEOP*	89879100	1	1
11P2B08	10P1B23	PWOUT 1	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
11P2B09	10P1A02	PWOUT 0	89879100	1	1
11P2B10	08P1A20	SFM*	89879104		
11P2B11	14P1B06	TTONLINE*	89879104		
11P2B12	12P1B05	ISTSP	89879100	1	1
11P2B13	09P1A02	PWOUT 2	89879100	1	1
11P2B14	13P2A22	RWLD RWUNLD	89879100	1	1
11P2B15	13P2B18	FM/TM	89879100	1	1
11P2B16	12P1A24	EORS	89879100	1	1
11P2B17	13P2A18	PAR ERR.	89879100	1	1
11P2B18	10P2B23	PWOUT 5	89879100	1	1
11P2B19	13P2A06	WRITE CLOCK	89879100	1	1
11P2B20	09P1B23	PWOUT 4	89879100	1	1
11P2B22	10P2B10	PWOUT 7	89879100	1	1
11P2B23	10P2B08	PWOUTP	89879100	1	1
11P2B24	09P2B23	PWOUT 6	89879100	1	1
11P2B25	08P2A23	PRSTROBE	89879100	1	1
11P2B26	08P1A10	PWRESET	89879100	1	1
11P2B27	10P2A07	WCLK	89879100	1	1
11P2B28	14P2A22	RWUNLD*	89879100	1	1
11P2B29	12P2B31	RWLD*	89879100	1	1
11P2B30	12P1A31	CRCC STATE*	89879100	1	1
11P2B31	13P2A15	MODESEL*	89879100	1	1
12P1A01	19P1A09	SVIO*	89879100	1	1
12P1A01	05P1B17	SVIO*	89879100	2	2
12P1A02	14P2A13	PROT FAULT	89879100	1	1
12P1A03	13P2B14	DATA	89879100	2	2
12P1A04	13P1A02	LOWX1*	89879100	2	2
12P1A05	13P2A02	CLR LOWER*	89879100	2	2
12P1A06	08P2B24	POSTAMBLE	89879104		
12P1A08	11P1A27	UPPER	89879100	2	2
12P1A09	14P1B13	LAST WORD	89879100	2	2
12P1A10	14P2A14	LOCKOUT*	89879100	1	1
12P1A11	13P2B10	EARLY WDS	89879100	2	2
12P1A12	13P2B09	WDS SHIFTED	89879100	2	2
12P1A13	11P2A05	STWCRC*	89879100	1	1
12P1A14	05P1A13	SRSM*	89879100	2	2
12P1A14	16P1A10	SRSM*	89879100	1	1
12P1A16	13P2A23	LOST DATA*	89879100	2	2
12P1A17	13P2B17	REQ*	89879100	2	2
12P1A19	05P1B21	S WRITE*	89879100	2	2
12P1A19	16P1B05	S WRITE*	89879100	1	1
12P1A20	16P1A01	SRQ*	89879100	1	1
12P1A20	05P1A15	SRQ*	89879100	2	2
12P1A21	14P2B31	STOP DIST*	89879100	1	1
12P1A23	13P2A20	DSA WREN*	89879100	2	2
12P1A24	11P2B16	EORS	89879100	1	1
12P1A25	13P1A31	EOG*	89879100	2	2
12P1A26	11P2A18	LRCC STATE	89879100	1	1
12P1A27	11P2A25	RDS*	89879100	1	1
12P1A28	08P1A02	PWRQ	89879100	2	2
12P1A30	13P1B24	9T*	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
12P1A31	11P2B30	CRCC STATE*	89879100	1	1
12P1B01	05P1A17	PEL*	89879100	2	2
12P1B01	19P1A10	PEL*	89879100	1	1
12P1B02	14P2B13	STO.PAR.ERR	89879100	1	1
12P1B03	14P1B02	UPPX1*	89879100	2	2
12P1B04	13P2A12	LOST DATA	89879100	2	2
12P1B05	11P2B12	ISTSP	89879100	1	1
12P1B06	11P1B31	A/D	89879100	1	1
12P1B06	13P2B13	A/D	89879100	2	2
12P1B07	13P1B03	TRANS*	89879100	2	2
12P1B08	13P1B18	INCCA*	89879100	2	2
12P1B09	08P1A15	BUFF2FL*WMO	89879100	1	1
12P1B10	13P2A06	WRITE CLOCK	89879100	2	2
12P1B12	08P1A13	PWRQSHIFTED	89879100	2	2
12P1B13	14P2B17	TTBUSY*	89879100	1	1
12P1B16	13P2B22	ALL	89879100	2	2
12P1B18	11P1B05	1600	89879100	1	1
12P1B19	11P1A31	RES2*	89879100	1	1
12P1B19	13P2A28	RES2*	89879100	2	2
12P1B20	13P1B14	BUF I/O*	89879100	2	2
12P1B21	07P1B07	CHI*	89879100	2	2
12P1B21	15P1B07	CHI*	89879100	1	1
12P1B22	16P1B03	SS*	89879100	1	1
12P1B22	05P1B12	SS*	89879100	2	2
12P1B24	10P2B16	WFM/TM*	89879100	2	2
12P1B24	14P2B25	WFM/TM*	89879100	1	1
12P1B24	08P1A21	WFM	89879104		
12P1B25	08P1B02	PE START	89879104		
12P1B26	14P1A07	RES1.1*	89879100	2	2
12P1B27	14P2B16	STOP*	89879100	1	1
12P1B28	13P2B20	ENA*	89879100	2	2
12P1B29	07P1A21	READ*	89879100	2	2
12P1B29	15P1A21	READ*	89879100	1	1
12P1B30	15P1B21	WRITE*	89879100	1	1
12P1B30	07P1B21	WRITE*	89879100	2	2
12P1B31	07P1A12	QC	89879100	2	2
12P1B31	15P1A12	QC	89879100	1	1
12P2A01	14P2B07	STRMF	89879100	1	1
12P2A02	13P2A01	CONTACT*	89879100	2	2
12P2A04	14P2B22	LEGMF	89879100	1	1
12P2A05	11P1B30	RMOT	89879100	1	1
12P2A06	14P1A28	CONTACT	89879100	2	2
12P2A07	14P2B10	LEGCF	89879100	1	1
12P2A08	13P2A13	EOP	89879100	2	2
12P2A08	11P2B03	EOP	89879100	1	1
12P2A09	13P1B22	STRBUF*	89879100	2	2
12P2A11	13P1A27	SELA1	89879100	2	2
12P2A12	13P2B02	LEGUS	89879100	2	2
12P2A13	13P2A17	READY	89879100	2	2
12P2A14	15P1B22	REJECT*	89879100	3	3
12P2A15	13P2A07	STRUS	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
12P2A17	14P1B24	FM/TM	89879100	1	1	
12P2A18	05P1B14	SPI*	89879100	2	2	
12P2A18	16P1A03	SPI*	89879100	1	1	
12P2A19	07P1A23	PRTAQ*	89879100	3	3	
12P2A19	15P2B28	PRTAQ*	89879100	2	2	
12P2A23	15P2B10	Q9	89879100	2	2	
12P2A23	15P1B16	Q9	89879100	1	1	
12P2A24	15P1B15	Q7	89879100	1	1	
12P2A24	15P2B09	Q7	89879100	2	2	
12P2A25	07P1A20	WEZ*	89879100	2	2	LENGTH 10"
12P2A25	21P2B30	WEZ*	89879100	3	3	LENGTH 7"
12P2A26	05P1B19	SCFCM(BUS)	89879100	2	2	
12P2A27	16P1B01	SCROD(SCRIM	89879100	1	1	
12P2A29	11P2B05	4MHZ	89879100	1	1	
12P2A30	13P2B24	TM1	89879100	2	2	
12P2B01	19P2B02	Q1	89879100	2	2	
12P2B01	15P1B12	Q1	89879100	1	1	
12P2B02	13P2A09	MC*	89879100	2	2	
12P2B03	14P2A09	USA	89879100	1	1	
12P2B04	11P1A10	WMOT	89879100	2	2	
12P2B05	14P2A25	RMOT*	89879100	1	1	
12P2B05	13P1A06	RMOT*	89879100	2	2	
12P2B06	14P2B24	WMOT*	89879100	1	1	
12P2B07	13P1A18	A7	89879100	2	2	
12P2B07	14P2B08	A7	89879100	1	1	
12P2B09	13P2A10	STRINT	89879100	2	2	
12P2B10	13P1B28	BUSY	89879100	2	2	
12P2B10	14P2A07	BUSY	89879100	1	1	
12P2B11	13P1A25	SELA0	89879100	2	2	
12P2B12	14P1B31	LEGCC	89879100	2	2	
12P2B13	13P2B04	STRCC	89879100	2	2	
12P2B14	15P1A22	REPLY*	89879100	3	3	
12P2B15	13P2A25	PROTECTED	89879100	2	2	
12P2B16	13P2B15	INT	89879100	2	2	
12P2B17	14P2B26	GC128	89879100	1	1	
12P2B17	08P1B22	GC128	89879104			
12P2B18	13P2A11	RES1*	89879100	2	2	
12P2B19	13P1B09	LDLWA*	89879100	2	2	
12P2B22	15P2A10	Q10	89879100	2	2	
12P2B22	15P1A17	Q10	89879100	1	1	
12P2B23	15P1A16	Q8	89879100	1	1	
12P2B23	15P2A09	Q8	89879100	2	2	
12P2B25	16P1A04	SCFOD(SCFIM	89879100	1	1	
12P2B28	05P1B16	SCRCM(BUS)	89879100	2	2	
12P2B29	13P2B16	TM3	89879100	2	2	
12P2B29	08P2B23	TM3	89879100	1	1	
12P2B31	13P2B26	RWLD*	89879100	2	2	
12P2B31	11P2B29	RWLD*	89879100	1	1	
13P1A01	14P1B01	RDTAPE 2	89879100	1	1	
13P1A01	11P1A05	RDTAPE 2	89879100	2	2	
13P1A02	12P1A04	LOWX1*	89879100	2	2	

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
13P1A03	11P1A02	RDTAPE 1	89879100	2	2
13P1A03	14P1B03	RDTAPE 1	89879100	1	1
13P1A04	11P1A07	RDTAPE 6	89879100	2	2
13P1A04	14P1A04	RDTAPE 6	89879100	1	1
13P1A05	18P1B08	SA2	89879100	1	1
13P1A05	05P1B25	SA2	89879100	2	2
13P1A06	12P2B05	RMDT*	89879100	2	2
13P1A07	11P1B02	RDTAPE 5	89879100	2	2
13P1A07	14P1B07	RDTAPE 5	89879100	1	1
13P1A08	11P1A22	WRTAPE 0	89879100	2	2
13P1A09	05P1B30	SA6	89879100	2	2
13P1A09	18P1B06	SA6	89879100	1	1
13P1A10	27P1A03	SD1	89879100	1	1
13P1A10	05P1B01	SD1	89879100	2	2
13P1A10	18P2A27	SD1	89879100	3	3
13P1A11	11P1A25	WRTAPE 3	89879100	2	2
13P1A12	18P2B28	SD0	89879100	3	3
13P1A12	05P1A03	SD0	89879100	2	2
13P1A12	27P1A01	SD0	89879100	1	1
13P1A13	14P1B17	A=B	89879100	2	2
13P1A14	11P1A19	WRTAPE 5	89879100	2	2
13P1A15	27P1A12	SD7	89879100	1	1
13P1A15	05P1B03	SD7	89879100	2	2
13P1A15	18P2B25	SD7	89879100	3	3
13P1A16	18P2A24	SD6	89879100	3	3
13P1A16	05P1A02	SD6	89879100	2	2
13P1A16	27P1A10	SD6	89879100	1	1
13P1A17	11P1A24	WRTAPE 6	89879100	2	2
13P1A18	12P2B07	A7	89879100	2	2
13P1A19	07P1A02	OA6*	89879100	2	2
13P1A19	15P1A02	OA6*	89879100	1	1
13P1A20	15P1A07	OA4*	89879100	1	1
13P1A20	07P1A07	OA4*	89879100	2	2
13P1A21	07P1B02	OA2*	89879100	2	2
13P1A21	15P1B02	OA2*	89879100	1	1
13P1A22	11P1A21	WRTAPE 1	89879100	2	2
13P1A23	05P1B24	SA1	89879100	2	2
13P1A23	18P1B03	SA1	89879100	1	1
13P1A24	11P1A23	WRTAPE 7	89879100	2	2
13P1A25	12P2B11	SELA0	89879100	2	2
13P1A25	14P1A25	SELA0	89879100	1	1
13P1A26	18P1B09	SA5	89879100	1	1
13P1A26	05P1B28	SA5	89879100	2	2
13P1A27	12P2A11	SELA1	89879100	2	2
13P1A27	14P1A27	SELA1	89879100	1	1
13P1A30	07P1B01	OA1*	89879100	2	2
13P1A30	15P1B01	OA1*	89879100	1	1
13P1A31	14P2A27	ECG*	89879100	1	1
13P1A31	12P1A25	ECG*	89879100	2	2
13P1B01	11P1A06	RDTAPE 3	89879100	2	2
13P1B01	14P1A01	RDTAPE 3	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
13P1B02	11P1A04	RDTAPE 0	89879100	2	2
13P1B02	14P1A02	RDTAPE 0	89879100	1	1
13P1B03	12P1BC7	TRANS*	89879100	2	2
13P1B03	14P1A03	TRANS*	89879100	1	1
13P1B04	14P1B04	RDTAPE 7	89879100	1	1
13P1B04	11P1A08	RDTAPE 7	89879100	2	2
13P1B05	18P1A02	SA0	89879100	1	1
13P1B05	05P1B23	SA0	89879100	2	2
13P1B06	11P1B04	RDTAPE 4	89879100	2	2
13P1B06	14P1A06	RDTAPE 4	89879100	1	1
13P1B08	18P1A09	SA4	89879100	1	1
13P1B08	05P1B27	SA4	89879100	2	2
13P1B09	12P2B19	LDLWA*	89879100	2	2
13P1B09	14P1A09	LDLWA*	89879100	1	1
13P1B10	27P1A05	SD2	89879100	1	1
13P1B10	05P1B02	SD2	89879100	2	2
13P1B10	18P2B26	SD2	89879100	3	3
13P1B12	18P2A25	SD3	89879100	3	3
13P1B12	05P1A06	SD3	89879100	2	2
13P1B12	27P1B06	SD3	89879100	1	1
13P1B13	27P1A08	SD5	89879100	1	1
13P1B13	05P1A01	SD5	89879100	2	2
13P1B13	18P2B24	SD5	89879100	3	3
13P1B14	12P1B20	BUF I/O*	89879100	2	2
13P1B14	14P1B14	BUF I/O*	89879100	1	1
13P1B15	27P1A07	SD4	89879100	1	1
13P1B15	18P2A23	SD4	89879100	3	3
13P1B15	05P1A07	SD4	89879100	2	2
13P1B16	11P1A20	WRTAPE 4	89879100	2	2
13P1B17	14P1A17	CARCURAD*	89879100	2	2
13P1B18	12P1B08	INCCA*	89879100	2	2
13P1B19	07P1A01	OA5*	89879100	2	2
13P1B19	15P1A01	OA5*	89879100	1	1
13P1B20	15P1B03	OA7*	89879100	1	1
13P1B20	07P1B03	OA7*	89879100	2	2
13P1B21	07P1A06	OA3*	89879100	2	2
13P1B21	15P1A06	OA3*	89879100	1	1
13P1B22	12P2A09	STRBUF*	89879100	2	2
13P1B22	14P1A21	STRBUF*	89879100	1	1
13P1B23	18P1A08	SA3	89879100	1	1
13P1B23	05P1B26	SA3	89879100	2	2
13P1B24	12P1A30	9T*	89879100	2	2
13P1B25	18P1A06	SA7	89879100	1	1
13P1B25	05P1B31	SA7	89879100	2	2
13P1B27	11P1B26	WRTAPE 2	89879100	2	2
13P1B28	12P2B10	BUSY	89879100	2	2
13P1B29	07P1A03	OA0*	89879100	2	2
13P1B29	15P1A03	OA0*	89879100	1	1
13P1B30	08P2B09	PE LOST CAT	89879100	2	2
13P1B31	08P1A03	PE ENABLE	89879100	2	2
13P2A01	12P2A02	CONTACT*	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
13P2A02	12P1A05	CLR LOWER*	89879100	2	2
13P2A05	08P1B18	WREQUEST*	89879100	2	2
13P2A05	14P2A17	WREQUEST*	89879100	1	1
13P2A06	11P2B19	WRITE CLOCK	89879100	1	1
13P2A06	12P1B10	WRITE CLOCK	89879100	2	2
13P2A07	12P2A15	STRUS	89879100	2	2
13P2A07	14P1A31	STRUS	89879100	1	1
13P2A08	14P1A30	WRENABLE	89879100	2	2
13P2A09	12P2B02	MC*	89879100	2	2
13P2A09	14P2A04	MC*	89879100	1	1
13P2A10	12P2B09	STRINT	89879100	2	2
13P2A11	12P2B18	RESI*	89879100	2	2
13P2A12	12P1B04	LOST DATA	89879100	2	2
13P2A13	14P2B01	EOP	89879100	1	1
13P2A13	12P2A08	EOP	89879100	2	2
13P2A14	11P1A17	BCD	89879100	2	2
13P2A15	11P2B31	MODESEL*	89879100	1	1
13P2A17	12P2A13	READY	89879100	2	2
13P2A18	14P1B23	PAR ERR.	89879100	2	2
13P2A18	11P2B17	PAR ERR.	89879100	1	1
13P2A19	14P2A24	TTDENSTAT*	89879100	1	1
13P2A20	12P1A23	DSA WREN*	89879100	2	2
13P2A20	14P2B30	DSA WREN*	89879100	1	1
13P2A21	08P2A24	AL2	89879100	2	2
13P2A22	11P2B14	RWLD RWUNLD	89879100	1	1
13P2A23	12P1A16	LOST DATA*	89879100	2	2
13P2A24	08P2A21	75IPS	89879100	2	2
13P2A25	12P2B15	PROTECTED	89879100	2	2
13P2A26	11P1A28	9T	89879100	2	2
13P2A26	14P2A21	9T	89879100	1	1
13P2A27	14P2B11	US1	89879100	1	1
13P2A28	14P2B05	RES2*	89879100	1	1
13P2A28	12P1B19	RES2*	89879100	2	2
13P2A29	08P2A14	PECHARCLK	89879100	2	2
13P2A30	08P1B13	PECLOCK*	89879100	2	2
13P2B01	14P2B19	BOT	89879100	1	1
13P2B02	12P2A12	LEGLS	89879100	2	2
13P2B03	14P1B30	ILLUSCODE	89879100	2	2
13P2B04	12P2B13	STRCC	89879100	2	2
13P2B05	11P1B05	1600	89879100	2	2
13P2B06	14P2B23	PE START	89879100	1	1
13P2B06	08P1B02	PE START	89879100	2	2
13P2B07	10P1A01	PC 1600*	89879100	2	2
13P2B08	08P2B12	PE WORNING	89879100	2	2
13P2B09	12P1A12	WDS SHIFTED	89879100	2	2
13P2B10	12P1A11	EARLY WDS	89879100	2	2
13P2B11	21P2A27	MC*	89879100	3	3
13P2B12	11P1A30	2FWC	89879100	2	2
13P2B13	12P1B06	A/D	89879100	2	2
13P2B13	14P2B12	A/D	89879100	1	1
13P2B14	12P1A03	DATA	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
13P2B15	12P2B16	INT	89879100	2	2
13P2B16	12P2B29	TM3	89879100	2	2
13P2B16	14P2A19	TM3	89879100	1	1
13P2B17	14P2A29	REQ*	89879100	1	1
13P2B17	12P1A17	REQ*	89879100	2	2
13P2B18	14P1B24	FM/TM	89879100	2	2
13P2B18	11P2B15	FM/TM	89879100	1	1
13P2B19	14P2A23	TTREADY*	89879100	1	1
13P2B20	12P1B28	ENA*	89879100	2	2
13P2B20	14P2B29	ENA*	89879100	1	1
13P2B22	12P1B16	AL1	89879100	2	2
13P2B23	14P2B27	EOT*	89879100	1	1
13P2B24	12P2A30	TM1	89879100	2	2
13P2B25	14P2B28	GAP CLOCK	89879100	1	1
13P2B26	14P2B15	RWLD*	89879100	1	1
13P2B26	12P2B31	RWLD*	89879100	2	2
13P2B27	14P2B09	USO	89879100	1	1
13P2B28	14P2A28	TT READY	89879100	1	1
14P1A01	13P1B01	RDTAPE 3	89879100	1	1
14P1A02	13P1B02	RDTAPE 0	89879100	1	1
14P1A03	13P1B03	TRANS*	89879100	1	1
14P1A04	13P1A04	RDTAPE 6	89879100	1	1
14P1A05	18P1A07	SA8	89879100	1	1
14P1A05	05P1A23	SA8	89879100	2	2
14P1A06	13P1B06	RDTAPE 4	89879100	1	1
14P1A07	12P1B26	RES1.1*	89879100	2	2
14P1A08	18P1B01	SA12	89879100	1	1
14P1A08	05P1A27	SA12	89879100	2	2
14P1A09	13P1B09	LDLWA*	89879100	1	1
14P1A10	18P2A30	SD10	89879100	3	3
14P1A10	05P1B06	SD10	89879100	2	2
14P1A10	27P1B18	SD10	89879100	1	1
14P1A11	11P1B27	WRTAPE 11	89879100	2	2
14P1A12	27P1A18	SD11	89879100	1	1
14P1A12	05P1A05	SD11	89879100	2	2
14P1A12	18P2B31	SD11	89879100	3	3
14P1A13	11P1B20	WRTAPE 13	89879100	2	2
14P1A14	27P1A19	SD15	89879100	1	1
14P1A14	18P2B30	SD15	89879100	3	3
14P1A14	05P1A11	SD15	89879100	2	2
14P1A15	05P1B10	SD14	89879100	2	2
14P1A15	18P2A29	SD14	89879100	3	3
14P1A15	27P1B27	SD14	89879100	1	1
14P1A16	11P1B25	WRTAPE 14	89879100	2	2
14P1A17	13P1B17	CARCURAD*	89879100	2	2
14P1A18	07P1B09	OA13*	89879100	2	2
14P1A18	15P1B09	OA13*	89879100	1	1
14P1A19	15P1A11	OA15*	89879100	1	1
14P1A19	07P1A11	OA15*	89879100	2	2
14P1A20	07P1A05	OA11*	89879100	2	2
14P1A20	15P1A05	OA11*	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
14P1A21	13P1B22	STRBUF*	89879100	1	1
14P1A22	18P1B07	SA9	89879100	1	1
14P1A22	05P1A24	SA9	89879100	2	2
14P1A23	05P1A26	SA11	89879100	2	2
14P1A23	18P1A03	SA11	89879100	1	1
14P1A24	11P1B24	WRTAPE 15	89879100	2	2
14P1A25	13P1A25	SELA0	89879100	1	1
14P1A26	18P1A04	SA13	89879100	1	1
14P1A26	05P1A28	SA13	89879100	2	2
14P1A27	13P1A27	SELA1	89879100	1	1
14P1A28	12P2A06	CONTACT	89879100	2	2
14P1A30	13P2A08	WRENABLE	89879100	2	2
14P1A31	13P2A07	STRUS	89879100	1	1
14P1B01	13P1A01	RDTAPE 2	89879100	1	1
14P1B02	12P1B03	UPPX1*	89879100	2	2
14P1B03	13P1A03	RDTAPE 1	89879100	1	1
14P1B04	13P1B04	RDTAPE 7	89879100	1	1
14P1B05	18P1B02	SA10	89879100	1	1
14P1B05	05P1A25	SA10	89879100	2	2
14P1B06	11P2B11	TTONLINE*	89879104		
14P1B07	13P1A07	RDTAPE 5	89879100	1	1
14P1B08	11P1B23	WRTAPE 8	89879100	2	2
14P1B09	18P1B04	SA14	89879100	1	1
14P1B09	05P1A30	SA14	89879100	2	2
14P1B10	18P2A26	SD9	89879100	3	3
14P1B10	05P1B05	SD9	89879100	2	2
14P1B10	27P1B16	SD9	89879100	1	1
14P1B12	27P1B14	SD8	89879100	1	1
14P1B12	05P1B04	SD8	89879100	2	2
14P1B12	18P2B27	SD8	89879100	3	3
14P1B13	12P1A09	LAST WORD	89879100	2	2
14P1B14	13P1B14	BUF I/O*	89879100	1	1
14P1B15	27P1A20	SD12	89879100	1	1
14P1B15	18P2A28	SD12	89879100	3	3
14P1B15	05P1A04	SD12	89879100	2	2
14P1B16	11P1B21	WRTAPE 12	89879100	2	2
14P1B17	13P1A13	A=B	89879100	2	2
14P1B18	07P1B10	OA14*	89879100	2	2
14P1B18	15P1B10	OA14*	89879100	1	1
14P1B19	15P1A04	OA12*	89879100	1	1
14P1B19	07P1A04	OA12*	89879100	2	2
14P1B20	07P1B06	OA10*	89879100	2	2
14P1B20	15P1B06	OA10*	89879100	1	1
14P1B21	11P1B22	WRTAPE 9	89879100	2	2
14P1B22	07P1B05	OA9*	89879100	2	2
14P1B22	15P1B05	OA9*	89879100	1	1
14P1B23	13P2A18	PAR ERR.	89879100	2	2
14P1B24	13P2B18	FM/TM	89879100	2	2
14P1B24	12P2A17	FM/TM	89879100	1	1
14P1B25	18P1A01	SA15	89879100	1	1
14P1B25	05P1A31	SA15	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
14P1B26	18P2B29	SD13	89879100	3	3
14P1B26	05P1B09	SD13	89879100	2	2
14P1B26	27P1B23	SD13	89879100	1	1
14P1B27	11P1A26	WRTAPE 1C	89879100	2	2
14P1B29	07P1B04	OA8*	89879100	2	2
14P1B29	15P1B04	OA8*	89879100	1	1
14P1B30	13P2B03	ILLLSCODE	89879100	2	2
14P1B31	12P2B12	LEGCC	89879100	2	2
14P2A01	08P2A18	PE EOP*	89879100	1	1
14P2A04	13P2A09	MC*	89879100	1	1
14P2A07	12P2B10	BUSY	89879100	1	1
14P2A09	12P2B03	USA	89879100	1	1
14P2A13	12P1A02	PROT FAULT	89879100	1	1
14P2A14	12P1A10	LCCKOUT*	89879100	1	1
14P2A17	13P2A05	WREQUEST*	89879100	1	1
14P2A19	13P2B16	TM3	89879100	1	1
14P2A21	13P2A26	9T	89879100	1	1
14P2A22	11P2B28	RWUNLD*	89879100	1	1
14P2A23	13P2B19	TTREADY*	89879100	1	1
14P2A24	13P2A19	TTDENSTAT*	89879100	1	1
14P2A25	12P2B05	RMOT*	89879100	1	1
14P2A27	13P1A31	EOG*	89879100	1	1
14P2A28	13P2B28	TT READY	89879100	1	1
14P2A29	13P2B17	REQ*	89879100	1	1
14P2A30	08P1A07	PWID	89879100	1	1
14P2B01	13P2A13	EOP	89879100	1	1
14P2B02	11P2B07	SEOP*	89879100	1	1
14P2B03	11P1B28	FILL	89879100	1	1
14P2B05	13P2A28	RES2*	89879100	1	1
14P2B06	08P2B10	REV*	89879104		
14P2B07	12P2A01	STRMF	89879100	1	1
14P2B08	12P2B07	A7	89879100	1	1
14P2B09	13P2B27	USO	89879100	1	1
14P2B10	12P2A07	LEGCF	89879100	1	1
14P2B11	13P2A27	US1	89879100	1	1
14P2B12	13P2B13	A/D	89879100	1	1
14P2B13	12P1B02	STO.PAR.ERR	89879100	1	1
14P2B14	08P1A24	IC ABORT*	89879100	1	1
14P2B15	13P2B26	RWLD*	89879100	1	1
14P2B16	12P1B27	STOP*	89879100	1	1
14P2B17	12P1B13	TTBUSY*	89879100	1	1
14P2B18	08P1A20	SFM*	89879104		
14P2B19	13P2B01	BOT	89879100	1	1
14P2B20	08P1A27	PRBOT	89879100	1	1
14P2B22	12P2A04	LEGMF	89879100	1	1
14P2B23	13P2B06	PE START	89879100	1	1
14P2B24	12P2B06	WMOT*	89879100	1	1
14P2B25	12P1B24	WFM/TM*	89879100	1	1
14P2B26	12P2B17	GC128	89879100	1	1
14P2B27	13P2B23	EOT*	89879100	1	1
14P2B28	13P2B25	GAP CLCCK	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
14P2B29	13P2B20	ENA*	89879100	1	1
14P2B30	13P2A20	DSA WREN*	89879100	1	1
14P2B31	12P1A21	STOP DIST*	89879100	1	1
15P1A01	19P1A19	0A5*	89879100	2	2
15P1A01	13P1B19	0A5*	89879100	1	1
15P1A02	13P1A19	0A6*	89879100	1	1
15P1A02	19P1A17	0A6*	89879100	2	2
15P1A03	19P1A30	0A0*	89879100	2	2
15P1A03	13P1B29	0A0*	89879100	1	1
15P1A04	14P1B19	0A12*	89879100	1	1
15P1A04	19P1B08	0A12*	89879100	2	2
15P1A05	19P1B12	0A11*	89879100	2	2
15P1A05	14P1A20	0A11*	89879100	1	1
15P1A06	13P1B21	0A3*	89879100	1	1
15P1A06	19P1A26	0A3*	89879100	2	2
15P1A07	19P1B18	0A4*	89879100	2	2
15P1A07	13P1A20	0A4*	89879100	1	1
15P1A09	21P2B28	T.P.	89879100	1	1
15P1A09	07P1A09	T.P.	89879100	2	2
15P1A11	19P1B07	0A15*	89879100	2	2
15P1A11	14P1A19	0A15*	89879100	1	1
15P1A12	12P1B31	Q0	89879100	1	1
15P1A12	19P1A28	Q0	89879100	2	2
15P1A13	07P1A13	Q2	89879100	2	2
15P1A13	19P2B01	Q2	89879100	1	1
15P1A14	20P2B07	Q4	89879100	1	1
15P1A14	C7P1A14	Q4	89879100	2	2
15P1A15	07P1A15	Q6	89879100	2	2
15P1A15	20P2A14	Q6	89879100	1	1
15P1A16	12P2B23	Q8	89879100	1	1
15P1A16	07P1A16	Q8	89879100	2	2
15P1A17	07P1A17	Q10	89879100	2	2
15P1A17	12P2B22	Q10	89879100	1	1
15P1A18	26P2A24	Q12	89879100	1	1
15P1A18	C7P1A18	Q12	89879100	2	2
15P1A19	C7P1A19	Q14	89879100	2	2
15P1A19	26P2B25	Q14	89879100	1	1
15P1A20	21P2B30	WEZ*	89879100	2	2
15P1A21	19P1B02	READ*	89879100	2	2
15P1A21	12P1B29	READ*	89879100	1	1
15P1A22	19P1A03	REPLY*	89879100	1	1
15P1A22	07P1A22	REPLY*	89879100	2	2
15P1A22	12P2B14	REPLY*	89879100	3	3
15P1A23	15P2B28	PRTAQ*	89879100	3	3
15P1A31	16P1A08	BL=0	89879104		
15P1B01	19P1B26	0A1*	89879100	2	2
15P1B01	13P1A30	0A1*	89879100	1	1
15P1B02	13P1A21	0A2*	89879100	1	1
15P1B02	19P1B24	0A2*	89879100	2	2
15P1B03	19P1B16	0A7*	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
15P1B03	13P1B20	DA7*	89879100	1	1
15P1B04	14P1B29	DA8*	89879100	1	1
15P1B04	19P1A15	DA8*	89879100	2	2
15P1B05	19P1A13	DA9*	89879100	2	2
15P1B05	14P1B22	DA9*	89879100	1	1
15P1B06	14P1B20	DA10*	89879100	1	1
15P1B06	19P1A14	DA10*	89879100	2	2
15P1B07	20P2B25	CHI*	89879100	2	2
15P1B07	12P1B21	CHI*	89879100	1	1
15P1B09	14P1A18	DA13*	89879100	1	1
15P1B09	19P1A07	DA13*	89879100	2	2
15P1B10	19P1A01	DA14*	89879100	2	2
15P1B10	14P1B18	DA14*	89879100	1	1
15P1B12	12P2B01	Q1	89879100	1	1
15P1B12	C7P1B12	Q1	89879100	2	2
15P1B13	07P1B13	Q3	89879100	2	2
15P1B13	25P1B09	Q3	89879100	1	1
15P1B14	20P2B15	Q5	89879100	1	1
15P1B14	07P1B14	Q5	89879100	2	2
15P1B15	07P1B15	Q7	89879100	2	2
15P1B15	12P2A24	Q7	89879100	1	1
15P1B16	12P2A23	Q9	89879100	1	1
15P1B16	07P1B16	Q9	89879100	2	2
15P1B17	07P1B17	Q11	89879100	2	2
15P1B17	26P1B09	Q11	89879100	1	1
15P1B18	26P2B28	Q13	89879100	1	1
15P1B18	07P1B18	Q13	89879100	2	2
15P1B19	07P1B19	Q15	89879100	2	2
15P1B19	26P2B01	Q15	89879100	1	1
15P1B21	12P1B30	WRITE*	89879100	1	1
15P1B21	19P2B31	WRITE*	89879100	2	2
15P1B22	07P1B22	REJECT*	89879100	2	2
15P1B22	12P2A14	REJECT*	89879100	3	3
15P1B22	19P1B01	REJECT*	89879100	1	1
15P1B23	16P2B07	MC*	89879100	1	1
15P1B23	07P1B23	MC*	89879100	2	2
15P1B23	25P1B20	MC*	89879100	3	3
15P2A01	18P1B05	SELD.UTPI10	89879100	2	2
15P2A02	19P1A16	SE.U.PRT.	89879100	2	2
15P2A04	16P2A08	US3*	89879100	1	1
15P2A05	19P2A24	DF-GATED	89879100	2	2
15P2A06	16P1B04	ULT.SRC.PRO	89879100	1	1
15P2A07	19P2A30	BUSY RR*	89879100	1	1
15P2A08	18P2A22	CA6	89879100	2	2
15P2A09	12P2B23	Q8	89879100	2	2
15P2A09	20P2B14	Q8	89879100	1	1
15P2A10	20P2B15	Q10	89879100	1	1
15P2A10	12P2B22	Q10	89879100	2	2
15P2A11	16P2A09	US2*	89879100	1	1
15P2A12	17P2A17	A13	89879100	2	2
15P2A13	17P2B20	A11	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
15P2A14	17P2A04	A0	89879100	2	2
15P2A15	17P2B13	A9	89879100	2	2
15P2A16	17P2A21	A10	89879100	2	2
15P2A17	18P2B06	CA65M*	89879100	2	2
15P2A18	16P1B31	A/Q CLEAR	89879100	2	2
15P2A19	19P1B03	ECU.NUM.MAT	89879100	1	1
15P2A20	19P2B10	PCKM	89879100	2	2
15P2A21	16P1A20	T.E.D ALTOL	89879100	2	2
15P2A22	17P2B02	A2	89879100	2	2
15P2A23	17P2A06	A3	89879100	1	1
15P2A24	19P1B27	SCOSE0	89879100	2	2
15P2A25	19P1A23	SCOSE2	89879100	2	2
15P2A26	16P2A06	SEOSC1*	89879100	1	1
15P2A27	16P2A02	SEOSC3*	89879100	1	1
15P2A28	16P1B21	AOAF+MC*	89879100	2	2
15P2A29	19P1B09	ADDR ERR	89879100	1	1
15P2B01	15P2B20	RESCTRBSY*	89879100	2	2
15P2B02	16P2B04	LA DIFF=0*	89879100	1	1
15P2B03	16P1B29	EOPMCT BSY*	89879100	1	1
15P2B04	18P1A19	SET.ADDR.ER	89879100	2	2
15P2B05	17P2B14	A8	89879100	2	2
15P2B06	16P1A06	READ	89879100	2	2
15P2B07	19P2A28	LA	89879100	2	2
15P2B08	16P2A07	US4*	89879100	1	1
15P2B09	20P2A06	Q7	89879100	1	1
15P2B09	12P2A24	Q7	89879100	2	2
15P2B10	12P2A23	Q9	89879100	2	2
15P2B10	20P2A16	Q9	89879100	1	1
15P2B11	16P2A14	US1*	89879100	1	1
15P2B12	17P2A16	A14	89879100	2	2
15P2B13	17P2B19	A12	89879100	2	2
15P2B14	17P2A15	A15	89879100	2	2
15P2B15	17P2B03	A1	89879100	1	1
15P2B16	17P2A08	A7	89879100	2	2
15P2B17	17P2B12	A4	89879100	2	2
15P2B18	16P1A19	MC	89879100	2	2
15P2B19	16P1A21	TAS EXT.	89879100	1	1
15P2B20	16P1A27	RESCTRBSY*	89879100	1	1
15P2B20	15P2B01	RESCTRBSY*	89879100	2	2
15P2B22	16P1A14	TD1	89879100	1	1
15P2B23	16P1B23	INCR TA	89879100	1	1
15P2B24	19P2A07	SCOSE1	89879100	1	1
15P2B25	19P1A22	SCOSE3	89879100	1	1
15P2B26	16P2A04	SEOSC2*	89879100	1	1
15P2B27	16P2A01	SEOSC4*	89879100	1	1
15P2B28	21P2A28	PRTAQ*	89879100	1	1
15P2B28	12P2A19	PRTAQ*	89879100	2	2
15P2B28	15P1A23	PRTAQ*	89879100	3	3
15P2B29	16P1B20	TD2	89879100	1	1
15P2B30	16P1B22	ADDR.ERR*	89879100	1	1
15P2B31	16P1A26	CTRLR BUSY	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
16P1A01	12P1A20	SRQ*	89879100	1	1
16P1A01	27P2A28	SRQ*	89879100	2	2
16P1A02	17P1B19	W+C	89879100	1	1
16P1A03	27P1B29	SPI*	89879100	2	2
16P1A03	12P2A18	SPI*	89879100	1	1
16P1A04	12P2B25	SCFOD(SCFIM	89879100	1	1
16P1A05	18P1A11	REQUEST*	89879100	2	2
16P1A06	15P2B04	READ	89879100	2	2
16P1A06	17P1B30	READ	89879100	1	1
16P1A07	18P2B04	DSA-BUFF1*	89879100	2	2
16P1A08	17P1A14	BL=0	89879100	1	1
16P1A08	15P1A31	BL=0	89879104		
16P1A09	17P1B10	CAL-SHIFT*	89879100	2	2
16P1A10	12P1A14	SRSM*	89879100	1	1
16P1A10	27P2B18	SRSM*	89879100	2	2
16P1A11	17P1B07	RESUME	89879100	2	2
16P1A12	17P2B11	TD4	89879100	2	2
16P1A13	18P2A18	SMPX0	89879100	2	2
16P1A14	17P1B28	TD1	89879100	2	2
16P1A14	15P2B22	TD1	89879100	1	1
16P1A15	18P2B23	BUFF1BUFF2*	89879100	1	1
16P1A16	17P1B15	BUFF1-BUFF2	89879100	2	2
16P1A17	17P2A23	TD3	89879100	1	1
16P1A18	17P1A12	SET NEED*	89879100	1	1
16P1A19	17P1A22	MC	89879100	1	1
16P1A19	15P2B18	MC	89879100	2	2
16P1A20	15P2A21	T.E.D AUTOL	89879100	2	2
16P1A21	15P2B19	TAS EXT.	89879100	1	1
16P1A22	19P2A18	LOST DATA	89879100	1	1
16P1A23	18P2A07	BL>CYL	89879100	2	2
16P1A25	19P2B29	SET ALARM*	89879100	1	1
16P1A26	15P2B31	CTRLR BUSY	89879100	1	1
16P1A26	19P2A08	CTRLR BUSY	89879100	2	2
16P1A27	19P2B19	RESET CTR B	89879100	2	2
15P1A27	19P2B19	RESET CTR B	89879100	2	2
16P1A27	15P2B20	RESCTRBSY*	89879100	1	1
16P1A28	19P1B30	DOF-LA-AUTO	89879100	2	2
16P1A30	19P2A14	SET CTR SEE	89879100	2	2
16P1A31	19P2A15	TD1*	89879100	1	1
16P1B01	12P2A27	SCRODISCRIM	89879100	1	1
16P1B03	12P1B22	SS*	89879100	1	1
16P1B03	27P2A19	SS*	89879100	2	2
16P1B04	15P2A06	ULT.SRC.PRO	89879100	1	1
16P1B05	27P1B31	S WRITE*	89879100	2	2
16P1B05	12P1A19	S WRITE*	89879100	1	1
15P1B07	19P1A24	DSA CONNECT	89879100	2	2
16P1B08	18P2A21	WRITE ENABL	89879100	2	2
16P1B09	17P1A31	SHIFT-BUUF1	89879100	1	1
16P1B10	17P2A14	INHIBIT NEE	89879100	1	1
16P1B12	17P1B31	16BITS.CLL	89879100	2	2
16P1B13	17P1A24	CAU SHIFT*	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
16P1B14	18P2B19	SMPX1	89879100	2	2
16P1B15	17P1B18	BUFF2 FULL*	89879100	1	1
16P1B16	17P2A25	011	89879100	2	2
16P1B19	18P2A15	LOAD SHIFT*	89879100	2	2
16P1B20	17P1A20	TD2	89879100	2	2
16P1B20	15P2B29	TD2	89879100	1	1
16P1B21	17P1B09	AOAF+MC*	89879100	1	1
16P1B21	15P2A28	AOAF+MC*	89879100	2	2
16P1B22	15P2B30	ADDR.ERR*	89879100	1	1
16P1B23	15P2B23	INCR TA	89879100	1	1
16P1B23	18P1A31	INCR TA	89879100	2	2
16P1B24	19P2B25	ADDRESS ECP	89879100	1	1
16P1B25	17P1A06	EOS	89879100	1	1
16P1B26	19P2A16	TD2*	89879100	1	1
16P1B27	19P1B28	INIT C	89879100	2	2
16P1B28	18P2B20	MC*	89879100	1	1
16P1B29	15P2B03	EOPMCT BSY*	89879100	1	1
16P1B29	19P1B31	EOPMCT BSY*	89879100	2	2
16P1B30	19P1A20	EOP	89879100	2	2
16P1B31	15P2A18	A/Q CLEAR	89879100	2	2
16P2A01	15P2B27	SEOSC4*	89879100	1	1
16P2A02	15P2A27	SEOSC3*	89879100	1	1
16P2A04	15P2B26	SEOSC2*	89879100	1	1
16P2A06	15P2A26	SEOSC1*	89879100	1	1
16P2A07	15P2B08	US4*	89879100	1	1
16P2A08	15P2A04	US3*	89879100	1	1
16P2A09	15P2A11	US2*	89879100	1	1
16P2A14	15P2B11	US1*	89879100	1	1
16P2B01	19P2A28	LA	89879100	1	1
16P2B02	18P2B07	ARCUR-CA*	89879100	1	1
16P2B03	17P2B05	ON CYL	89879100	1	1
16P2B04	15P2B02	LA DIFF=0*	89879100	1	1
16P2B05	19P2B06	CLEAR CONTR	89879100	1	1
16P2B06	17P1B29	AUTOLOAD2*	89879100	1	1
16P2B07	15P1B23	MC*	89879100	1	1
16P2B08	10P1B20	AUTOLOAD	89879100	1	1
16P2B09	19P2A17	INDEX GATED	89879100	1	1
16P2B10	18P2A12	SECTOR GATE	89879100	1	1
16P2B11	19P2A20	DRIVE RD*	89879100	1	1
16P2B12	19P2B24	PUR*	89879100	1	1
16P2B13	17P2A27	R+W+C+CC	89879100	1	1
16P2B14	18P2A04	CA19*	89879100	1	1
16P2B15	18P1A05	CA20*	89879100	1	1
16P2B16	17P1B27	WRITE DATA*	89879100	1	1
16P2B17	17P2B15	READ GATE*	89879100	1	1
16P2B18	18P2A09	CA7*	89879100	1	1
16P2B19	18P2B06	CA65M*	89879100	1	1
16P2B20	18P2A08	CA13*	89879100	1	1
16P2B22	17P2B23	WRITE GATE*	89879100	1	1
16P2B23	19P2B23	DRIVE FAULT	89879100	1	1
16P2B24	19P2A25	DRIVE SE*	89879100	1	1

	FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
	16P2B25	18P2B09	CA1J*	89879100	1	1	
	16P2B26	19P2B11	LA CLEAR*	89879100	1	1	
	16P2B27	18P2B11	CA12*	89879100	1	1	
	16P2B28	18P2A10	CA15*	89879100	1	1	
	16P2B29	18P2A05	CA17*	89879100	1	1	
	16P2B30	18P2A01	CA18*	89879100	1	1	
	16P2B31	18P2B08	CA16*	89879100	1	1	
	17P1A04	18P2A17	S11	89879100	2	2	
	17P1A06	16P1B25	EOS	89879100	1	1	
	17P1A08	18P1B28	CWA-COUNT*	89879100	2	2	
	17P1A09	19P2A06	LBL*	89879100	2	2	
	17P1A10	19P1B17	D.NO.COMP.	89879100	1	1	
	17P1A11	18P2A11	R+W+C	89879100	1	1	
	17P1A12	16P1A18	SET NEED*	89879100	1	1	
	17P1A14	16P1A08	BL=0	89879100	1	1	
	17P1A15	19P2A09	DOF-LA	89879100	1	1	
	17P1A16	18P1B31	DOF	89879100	2	2	
	17P1A17	19P2A21	INIT	89879100	2	2	
	17P1A18	19P2A13	CLEAR CKWD*	89879100	1	1	
	17P1A19	19P2B20	READ DATA	89879100	1	1	
	17P1A20	18P2B10	TD2	89879100	1	1	
	17P1A20	16P1B20	TD2	89879100	2	2	
	17P1A22	18P1B25	MC	89879100	2	2	
	17P1A22	16P1A19	MC	89879100	1	1	
	17P1A24	16P1B13	CAU SHIFT*	89879100	1	1	
SEE BELOW >	17P1A24	19P2A29	CAU SHIFT*	89879100	2	2	
	17P1A25	18P2A12	SECTOR GATE	89879100	2	2	
	17P1A27	19P1A27	W.CKWD*	89879100	2	2	
	17P1A28	19P1B23	INPUT CKWD	89879100	2	2	
	17P1A30	18P1A13	BL-BORROW*	89879100	1	1	
	17P1A31	16P1B09	SHIFT-BUUF1	89879100	1	1	
	17P1A31	18P2B05	SHIFT-BUUF1	89879100	2	2	
	17P1B03	18P2A16	S15	89879100	2	2	
	17P1B06	19P1B29	CKWD SHIFT	89879100	2	2	
	17P1B07	16P1A11	RESUME	89879100	2	2	
	17P1B09	19P2B03	AOAF+MC*	89879100	2	2	
	17P1B09	16P1B21	AOAF+MC*	89879100	1	1	
	17P1B10	16P1A09	CAL-SHIFT*	89879100	2	2	
	17P1B14	18P2B13	DATA	89879100	2	2	
	17P1B15	16P1A16	BUFF1-BUFF2	89879100	2	2	
	17P1B16	19P2A12	COMPARE	89879100	2	2	
	17P1B17	18P1A27	BL-LOAD*	89879100	2	2	
	17P1B18	16P1B15	BUFF2 FULL*	89879100	1	1	
	17P1B19	16P1A02	W+C	89879100	1	1	
	17P1B19	18P2A19	W+C	89879100	2	2	
	17P1B22	18P2B17	CLEAR-SHIFT	89879100	1	1	
	17P1B24	19P2A05	CKWD11	89879100	2	2	
	17P1B27	16P2B16	WRITE DATA*	89879100	1	1	
	17P1B28	16P1A14	TD1	89879100	2	2	
>	17P1A25	19P2B15	SECTOR GATE	89879100	3	3	LENGTH 9"

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
17P1B29	19P2B12	AUTOLOAD2*	89879100	2	2
17P1B29	16P2B06	AUTOLOAD2*	89879100	1	1
17P1B30	16P1A06	READ	89879100	1	1
17P1B30	19P2A11	READ	89879100	2	2
17P1B31	16P1B12	16BITS.011	89879100	2	2
17P2A01	20P2B19	0A2*	89879100	2	2
17P2A01	19P1B24	0A2*	89879100	1	1
17P2A02	19P1B26	0A1*	89879100	1	1
17P2A02	20P2B20	0A1*	89879100	2	2
17P2A04	15P2A14	A0	89879100	2	2
17P2A04	18P1A25	A0	89879100	1	1
17P2A05	19P2B16	ADDRESS*	89879100	1	1
17P2A06	15P2A23	A3	89879100	1	1
17P2A06	18P1B26	A3	89879100	2	2
17P2A07	19P1B05	010	89879100	2	2
17P2A08	15P2B16	A7	89879100	2	2
17P2A08	18P1B19	A7	89879100	1	1
17P2A09	18P1A24	A6	89879100	2	2
17P2A10	18P1B18	A5	89879100	1	1
17P2A11	19P1B18	0A4*	89879100	1	1
17P2A11	20P2A21	0A4*	89879100	2	2
17P2A12	20P2B24	0A9*	89879100	2	2
17P2A12	19P1A13	0A9*	89879100	1	1
17P2A13	19P1A15	0A8*	89879100	1	1
17P2A13	20P2B23	0A8*	89879100	2	2
17P2A14	16P1B10	INHIBIT NEE	89879100	1	1
17P2A15	18P1B13	A15	89879100	1	1
17P2A15	15P2B14	A15	89879100	2	2
17P2A16	15P2B12	A14	89879100	2	2
17P2A16	18P1B27	A14	89879100	1	1
17P2A17	18P1A28	A13	89879100	1	1
17P2A17	15P2A17	A13	89879100	2	2
17P2A18	19P1A05	ADDR.CKWD=0	89879100	2	2
17P2A19	26P2A23	0A12*	89879100	2	2
17P2A19	19P1B08	0A12*	89879100	1	1
17P2A20	19P1B17	0A11*	89879100	1	1
17P2A20	20P2B28	0A11*	89879100	2	2
17P2A21	15P2A16	A10	89879100	2	2
17P2A21	18P1B20	A10	89879100	1	1
17P2A22	18P2B16	SHIFT CLOCK	89879100	2	2
17P2A23	18P2B07	TD3	89879100	2	2
17P2A23	16P1A17	TD3	89879100	1	1
17P2A24	19P1A25	LOAD CKWD I	89879100	1	1
17P2A25	16P1B16	011	89879100	2	2
17P2A26	19P1B22	SAMPLE CHEC	89879100	1	1
17P2A27	19P2B27	R+W+C+CC	89879100	2	2
17P2A27	16P2B13	R+W+C+CC	89879100	1	1
17P2A28	19P2B22	WA-ADR	89879100	1	1
17P2B01	18P2A07	INCR.SECTOR	89879100	2	2
17P2B02	15P2A22	A2	89879100	2	2
17P2B02	18P1A26	A2	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
17P2B03	15P2B15	A1	89879100	1	1
17P2B03	18P1B29	A1	89879100	2	2
17P2B04	20P2A20	OA0*	89879100	2	2
17P2B04	19P1A30	OA0*	89879100	1	1
17P2B05	16P2B03	ON CYL	89879100	1	1
17P2B05	19P2A22	ON CYL	89879100	2	2
17P2B06	20P2A17	OA3*	89879100	2	2
17P2B06	19P1A26	OA3*	89879100	1	1
17P2B07	19P2B07	R+C+CC	89879100	2	2
17P2B08	20P2A19	OA7*	89879100	2	2
17P2B08	19P1B16	OA7*	89879100	1	1
17P2B09	19P1A17	OA6*	89879100	1	1
17P2B09	20P2B18	OA6*	89879100	2	2
17P2B10	20P2B22	OA5*	89879100	2	2
17P2B10	19P1A19	OA5*	89879100	1	1
17P2B11	18P2B03	TD4	89879100	1	1
17P2B11	16P1A17	TD4	89879100	2	2
17P2B12	15P2B17	A4	89879100	2	2
17P2B12	18P1A23	A4	89879100	1	1
17P2B13	18P1A20	A9	89879100	1	1
17P2B13	15P2A15	A9	89879100	2	2
17P2B14	15P2B05	A8	89879100	2	2
17P2B14	18P1B23	A8	89879100	1	1
17P2B15	16P2B17	READ GATE*	89879100	1	1
17P2B16	19P1A01	OA14*	89879100	1	1
17P2B16	26P2A22	OA14*	89879100	2	2
17P2B17	20P2A11	OA13*	89879100	2	2
17P2B17	19P1A07	OA13*	89879100	1	1
17P2B18	19P1B07	OA15*	89879100	1	1
17P2B18	26P2B22	OA15*	89879100	2	2
17P2B19	15P2B13	A12	89879100	2	2
17P2B19	18P1A30	A12	89879100	1	1
17P2B20	18P1B24	A11	89879100	1	1
17P2B20	15P2A13	A11	89879100	2	2
17P2B22	20P2B26	OA10*	89879100	2	2
17P2B22	19P1A14	OA10*	89879100	1	1
17P2B23	16P2B22	WRITE GATE*	89879100	1	1
17P2B24	19P2B30	ADDRESS 12*	89879100	1	1
17P2B28	19P2B13	WRITE	89879100	2	2
18P1A01	14P1B25	SA15	89879100	1	1
18P1A01	27P2A01	SA15	89879100	2	2
18P1A02	28P2A24	SA0	89879100	2	2
18P1A02	13P1B05	SA0	89879100	1	1
18P1A03	14P1A23	SA11	89879100	1	1
18P1A03	28P1B21	SA11	89879100	2	2
18P1A04	28P1A31	SA13	89879100	2	2
18P1A04	14P1A26	SA13	89879100	1	1
18P1A05	16P2B15	CA20*	89879100	1	1
18P1A06	13P1B25	SA7	89879100	1	1
18P1A06	28P1B23	SA7	89879100	2	2
18P1A07	28P1B30	SA8	89879100	2	2

	FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
	18P1A07	14P1A05	SA8	89879100	1	1	
	18P1A08	13P1B23	SA3	89879100	1	1	
	18P1A08	28P1A06	SA3	89879100	2	2	
	18P1A09	28P1B09	SA4	89879100	2	2	
	18P1A09	13P1B08	SA4	89879100	1	1	
	18P1A10	19P1B10	CACWA9	89879100	1	1	
SEE BELOW >	18P1A11	16P1A05	REQUEST*	89879100	2	2	
	18P1A12	19P1B13	CACWA10	89879100	2	2	
	18P1A13	17P1A30	BL-BORROW*	89879100	1	1	
	18P1A14	19P2B04	ARCUR CWA*	89879100	2	2	
	18P1A15	19P1A31	CACWA0	89879100	2	2	
	18P1A16	19P1A11	CACWA12	89879100	2	2	
	18P1A17	19P1B20	CACWA3	89879100	1	1	
	18P1A18	19P1B04	CACWA15	89879100	1	1	
	18P1A19	15P2B04	SET.ADDR.ER	89879100	2	2	
	18P1A20	17P2B13	A9	89879100	1	1	
	18P1A21	19P1A21	CACWA4	89879100	2	2	
	18P1A22	19P1A18	CACWA6	89879100	2	2	
	18P1A23	19P2A27	A4	89879100	2	2	
	18P1A23	17P2B12	A4	89879100	1	1	
	18P1A24	17P2A09	A6	89879100	2	2	
	18P1A25	17P2A04	A0	89879100	1	1	
	18P1A26	17P2B02	A2	89879100	1	1	
	18P1A26	19P2A19	A2	89879100	2	2	
	18P1A27	17P1B17	BL-LOAD*	89879100	2	2	
	18P1A28	17P2A17	A13	89879100	1	1	
	18P1A30	17P2B19	A12	89879100	1	1	
	18P1A31	19P2A26	INCR TA	89879100	1	1	
	18P1A31	16P1B23	INCR TA	89879100	2	2	
	18P1B01	14P1A08	SA12	89879100	1	1	
	18P1B01	28P1B27	SA12	89879100	2	2	
	18P1B02	28P1A26	SA10	89879100	2	2	
	18P1B02	14P1B05	SA10	89879100	1	1	
	18P1B03	13P1A23	SA1	89879100	1	1	
	18P1B03	28P2B25	SA1	89879100	2	2	
	18P1B04	28P1A30	SA14	89879100	2	2	
	18P1B04	14P1B09	SA14	89879100	1	1	
	18P1B05	15P2A01	SELD.UTPI10	89879100	2	2	
	18P1B05	19P1A04	SELD.UTPI10	89879100	1	1	
	18P1B06	13P1A09	SA6	89879100	1	1	
	18P1B06	28P1A21	SA6	89879100	2	2	
	18P1B07	28P1B29	SA9	89879100	2	2	
	18P1B07	14P1A22	SA9	89879100	1	1	
	18P1B08	13P1A05	SA2	89879100	1	1	
	18P1B08	28P1B01	SA2	89879100	2	2	
	18P1B09	28P1A09	SA5	89879100	2	2	
	18P1B09	13P1A26	SA5	89879100	1	1	
	18P1B10	19P1B14	CACWA8	89879100	2	2	
	18P1B12	19P1A12	CACWA11	89879100	1	1	
	18P1B13	17P2A15	A15	89879100	1	1	
	18P1B14	19P2A04	CACWA1	89879100	1	1	
	>18P1A11	18P2B01	REQUEST*	89879100	3	3	LENGTH 8"

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
18P1B15	19P1A08	CACWA13	89879100	1	1	
18P1B16	19P1B21	CACWA2	89879100	2	2	
18P1B17	19P1A06	CACWA14	89879100	2	2	
18P1B18	17P2A10	A5	89879100	1	1	
18P1B19	17P2A08	A7	89879100	1	1	
18P1B20	17P2A21	A10	89879100	1	1	
18P1B21	19P1B19	CACWA5	89879100	1	1	
18P1B22	19P1B15	CACWA7	89879100	1	1	
18P1B23	17P2B14	A8	89879100	1	1	
18P1B24	17P2B20	A11	89879100	1	1	
18P1B25	17P1A22	MC	89879100	2	2	
18P1B26	17P2A06	A3	89879100	2	2	
18P1B26	19P2B28	A3	89879100	1	1	
18P1B27	17P2A16	A14	89879100	1	1	
18P1B28	19P1B25	CWA-COUNT*	89879100	1	1	
18P1B28	17P1A08	CWA-COUNT*	89879100	2	2	
18P1B29	17P2B03	A1	89879100	2	2	
18P1B29	19P2A10	A1	89879100	1	1	
18P1B30	19P2B17	ADDT INDEX*	89879100	2	2	
18P1B31	17P1A16	DOF	89879100	2	2	
18P1B31	19P2B08	DOF	89879100	1	1	
18P2A01	16P2B30	CA18*	89879100	1	1	
18P2A02	17P2B01	INCR.SECTOR	89879100	2	2	
18P2A04	16P2B14	CA19*	89879100	1	1	
18P2A05	16P2B29	CA17*	89879100	1	1	
18P2A06	19P2B05	CARST*	89879100	1	1	
18P2A07	16P1A23	BL>CYL	89879100	2	2	
18P2A08	16P2B20	CA13*	89879100	1	1	
18P2A09	16P2B18	CA7*	89879100	1	1	
18P2A10	16P2B28	CA15*	89879100	1	1	
18P2A11	17P1A11	R+W+C	89879100	1	1	
18P2A11	19P2B09	R+W+C	89879100	2	2	
18P2A12	17P1A25	SECTOR GATE	89879100	2	2	
18P2A12	16P2B10	SECTOR GATE	89879100	1	1	
18P2A15	16P1B19	LOAD SHIFT*	89879100	2	2	
18P2A16	17P1B03	S15	89879100	2	2	
18P2A17	17P1A04	S11	89879100	2	2	
18P2A18	16P1A13	SMPX0	89879100	2	2	
18P2A19	17P1B19	W+C	89879100	2	2	
18P2A19	19P2A01	W+C	89879100	1	1	
18P2A21	16P1B08	WRITE ENABL	89879100	2	2	
18P2A22	15P2A08	CA6	89879100	2	2	
18P2A23	13P1B15	SD4	89879100	3	3	
18P2A24	13P1A16	SD6	89879100	3	3	
18P2A25	13P1B12	SD3	89879100	3	3	
18P2A26	14P1B10	SD9	89879100	3	3	
18P2A27	13P1A10	SD1	89879100	3	3	
18P2A28	14P1B15	SD12	89879100	3	3	
18P2A29	14P1A15	SD14	89879100	3	3	
18P2A30	14P1A10	SD10	89879100	3	3	
18P2B01	18P1A11	REQUEST*	89879100	3	3	LENGTH 8"

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
18P2B02	17P2A23	TD3	89879100	2	2	
18P2B02	19P2B14	TD3	89879100	1	1	
18P2B03	17P2B11	TD4	89879100	1	1	
18P2B03	19P2A23	TD4	89879100	2	2	
18P2B04	16P1A07	DSA-BUFF1*	89879100	2	2	
18P2B05	17P1A31	SHIFT-BUUF1	89879100	2	2	
18P2B06	15P2A17	CA65M*	89879100	2	2	
18P2B06	16P2B19	CA65M*	89879100	1	1	
18P2B07	16P2B02	ARCUR-CA*	89879100	1	1	
18P2B08	16P2B31	CA16*	89879100	1	1	
18P2B09	16P2B25	CA1J*	89879100	1	1	
18P2B10	17P1A20	TD2	89879100	1	1	
18P2B11	16P2B27	CA12*	89879100	1	1	
18P2B13	17P1B14	DATA	89879100	2	2	
18P2B16	17P2A22	SHIFT CLOCK	89879100	2	2	
18P2B17	17P1B22	CLEAR-SHIFT	89879100	1	1	
18P2B19	16P1B14	SMPX1	89879100	2	2	
18P2B20	19P2B26	MC*	89879100	2	2	
18P2B20	16P1B28	MC*	89879100	1	1	
18P2B23	16P1A15	BUFF1BUFF2*	89879100	1	1	
18P2B24	13P1B13	SD5	89879100	3	3	
18P2B25	13P1A15	SD7	89879100	3	3	
18P2B26	13P1B10	SD2	89879100	3	3	
18P2B27	14P1B12	SD8	89879100	3	3	
18P2B28	13P1A12	SD0	89879100	3	3	
18P2B29	14P1B26	SD13	89879100	3	3	
18P2B30	14P1A14	SD15	89879100	3	3	
18P2B31	14P1A12	SD11	89879100	3	3	
19P1A01	15P1B10	OA14*	89879100	2	2	
19P1A01	17P2B16	OA14*	89879100	1	1	
19P1A02	21P2B30	WEZ*	89879100	1	1	LENGTH 14"
19P1A03	15P1A22	REPLY*	89879100	1	1	
19P1A03	20P2B12	REPLY*	89879100	2	2	
19P1A04	18P1B05	SELD.UTPI10	89879100	1	1	
19P1A05	17P2A18	ADDR.CKWD=0	89879100	2	2	
19P1A06	18P1B17	CACWA14	89879100	2	2	
19P1A07	15P1B09	OA13*	89879100	2	2	
19P1A07	17P2B17	OA13*	89879100	1	1	
19P1A08	18P1B15	CACWA13	89879100	1	1	
19P1A09	27P2B24	SVIO*	89879100	2	2	
19P1A09	12P1A01	SVIO*	89879100	1	1	
19P1A10	12P1B01	PEL*	89879100	1	1	
19P1A10	21P1B06	PEL*	89879100	2	2	
19P1A11	18P1A16	CACWA12	89879100	2	2	
19P1A12	18P1B12	CACWA11	89879100	1	1	
19P1A13	17P2A12	OA9*	89879100	1	1	
19P1A13	15P1B05	OA9*	89879100	2	2	
19P1A14	15P1B06	OA10*	89879100	2	2	
19P1A14	17P2B22	OA10*	89879100	1	1	
19P1A15	17P2A13	OA8*	89879100	1	1	
19P1A15	15P1B04	OA8*	89879100	2	2	

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
19P1A16	15P2A02	SE.U.PRT.	89879100	2	2
19P1A17	15P1A02	OA6*	89879100	2	2
19P1A17	17P2B09	OA6*	89879100	1	1
19P1A18	18P1A22	CACWA6	89879100	2	2
19P1A19	15P1A01	OA5*	89879100	2	2
19P1A19	17P2B10	OA5*	89879100	1	1
19P1A20	16P1B30	EOP	89879100	2	2
19P1A21	18P1A21	CACWA4	89879100	2	2
19P1A22	15P2B25	SCOSE3	89879100	1	1
19P1A23	15P2A25	SCOSE2	89879100	2	2
19P1A24	16P1B07	DSA CONNECT	89879100	2	2
19P1A25	17P2A24	LOAD CKWD I	89879100	1	1
19P1A26	17P2B06	OA3*	89879100	1	1
19P1A26	15P1A06	OA3*	89879100	2	2
19P1A27	17P1A27	W.CKWD*	89879100	2	2
19P1A28	15P1A12	Q0	89879100	2	2
19P1A28	20P2A05	Q0	89879100	1	1
19P1A30	17P2B04	OA0*	89879100	1	1
19P1A30	15P1A03	OA0*	89879100	2	2
19P1A31	18P1A15	CACWA0	89879100	2	2
19P1B01	20P2B13	REJECT*	89879100	2	2
19P1B01	15P1B22	REJECT*	89879100	1	1
19P1B02	20P2A04	READ*	89879100	1	1
19P1B02	15P1A21	READ*	89879100	2	2
19P1B03	15P2A19	ECU.NUM.MAT	89879100	1	1
19P1B04	18P1A18	CACWA15	89879100	1	1
19P1B05	17P2A07	Q10	89879100	2	2
19P1B07	15P1A11	OA15*	89879100	2	2
19P1B07	17P2B18	OA15*	89879100	1	1
19P1B08	17P2A19	OA12*	89879100	1	1
19P1B08	15P1A04	OA12*	89879100	2	2
19P1B09	15P2A29	ADDR ERR	89879100	1	1
19P1B10	18P1A10	CACWA9	89879100	1	1
19P1B12	17P2A20	OA11*	89879100	1	1
19P1B12	15P1A05	OA11*	89879100	2	2
19P1B13	18P1A12	CACWA10	89879100	2	2
19P1B14	18P1B10	CACWA8	89879100	2	2
19P1B15	18P1B22	CACWA7	89879100	1	1
19P1B16	17P2B08	OA7*	89879100	1	1
19P1B16	15P1B03	OA7*	89879100	2	2
19P1B17	17P1A10	D.NO.COMP.	89879100	1	1
19P1B18	17P2A11	OA4*	89879100	1	1
19P1B18	15P1A07	OA4*	89879100	2	2
19P1B19	18P1B21	CACWA5	89879100	1	1
19P1B20	18P1A17	CACWA3	89879100	1	1
19P1B21	18P1B16	CACWA2	89879100	2	2
19P1B22	17P2A26	SAMPLE CHEC	89879100	1	1
19P1B23	17P1A28	INPUT CKWD	89879100	2	2
19P1B24	15P1B02	OA2*	89879100	2	2
19P1B24	17P2A01	OA2*	89879100	1	1
19P1B25	18P1B28	CWA-COUNT*	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
19P1B26	15P1B01	DA1*	89879100	2	2
19P1B26	17P2A02	DA1*	89879100	1	1
19P1B27	15P2A24	SCOSE0	89879100	2	2
19P1B28	16P1B27	INIT Q	89879100	2	2
19P1B29	17P1B06	CKWD SHIFT	89879100	2	2
19P1B30	16P1A28	DOF-LA-AUTO	89879100	2	2
19P1B31	16P1B29	EQPMCT BSY*	89879100	2	2
19P2A01	18P2A19	W+C	89879100	1	1
19P2A04	18P1B14	CACWA1	89879100	1	1
19P2A05	17P1B24	CKWD11	89879100	2	2
19P2A06	17P1A09	LBL*	89879100	2	2
19P2A07	15P2B24	SCOSE1	89879100	1	1
19P2A08	16P1A26	CTRLR BUSY	89879100	2	2
19P2A09	17P1A15	DOF-LA	89879100	1	1
19P2A10	18P1B29	A1	89879100	1	1
19P2A11	17P1B30	READ	89879100	2	2
19P2A12	17P1B16	COMPARE	89879100	2	2
19P2A13	17P1A18	CLEAR CKWD*	89879100	1	1
19P2A14	16P1A30	SET CTR SEE	89879100	2	2
19P2A15	16P1A31	TD1*	89879100	1	1
19P2A16	16P1B26	TD2*	89879100	1	1
19P2A17	16P2B09	INDEX GATED	89879100	1	1
19P2A18	16P1A22	LOST DATA	89879100	1	1
19P2A19	18P1A26	A2	89879100	2	2
19P2A20	16P2B11	DRIVE RD*	89879100	1	1
19P2A21	17P1A17	INIT	89879100	2	2
19P2A22	17P2B05	ON CYL	89879100	2	2
19P2A23	18P2B03	TD4	89879100	2	2
19P2A24	15P2A05	DF-GATED	89879100	2	2
19P2A25	16P2B24	DRIVE SE*	89879100	1	1
19P2A26	18P1A31	INCR TA	89879100	1	1
19P2A27	18P1A23	A4	89879100	2	2
19P2A28	15P2B07	LA	89879100	2	2
19P2A28	16P2B01	LA	89879100	1	1
19P2A29	17P1A24	CAU SHIFT*	89879100	2	2
19P2A30	15P2A07	BUSY RR*	89879100	1	1
19P2B01	15P1A13	Q2	89879100	1	1
19P2B01	25P1A08	Q2	89879100	2	2
19P2B02	12P2B01	Q1	89879100	2	2
19P2B02	25P1A11	Q1	89879100	1	1
19P2B03	17P1B09	AOAF+MC*	89879100	2	2
19P2B04	18P1A14	ARCUR CWA*	89879100	2	2
19P2B05	18P2A06	CARST*	89879100	1	1
19P2B06	16P2B05	CLEAR CONTR	89879100	1	1
19P2B07	17P2B07	R+C+CC	89879100	2	2
19P2B08	18P1B31	DOF	89879100	1	1
19P2B09	18P2A11	R+W+C	89879100	2	2
19P2B10	15P2A20	PCKM	89879100	2	2
19P2B11	16P2B26	LA CLEAR*	89879100	1	1
19P2B12	17P1B29	AUTOLOAD2*	89879100	2	2
19P2B13	17P2B28	WRITE	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
19P2B14	18P2B02	TD3	89879100	1	1	
19P2B15	17P1A25	SECTOR GATE	89879100	3	3	LENGTH 9"
19P2B16	17P2A05	ADDRESS*	89879100	1	1	
19P2B17	18P1B30	ADDT INDEX*	89879100	2	2	
19P2B19	16P1A27	RESET CTR B	89879100	2	2	
19P2B19	16P1A27	RESET CTR B	89879100	2	2	
19P2B20	17P1A19	READ DATA	89879100	1	1	
19P2B22	17P2A28	WA-ADR	89879100	1	1	
19P2B23	16P2B23	DRIVE FAULT	89879100	1	1	
19P2B24	16P2B17	PUR*	89879100	1	1	
19P2B25	16P1B24	ADDRESS ECP	89879100	1	1	
19P2B26	18P2B20	MC*	89879100	2	2	
19P2B27	17P2A27	R+W+C+CC	89879100	2	2	
19P2B28	18P1B26	A3	89879100	1	1	
19P2B29	16P1A25	SET ALARM*	89879100	1	1	
19P2B30	17P2B24	ADDRESS 12*	89879100	1	1	
19P2B31	20P2B06	WRITE*	89879100	1	1	
19P2B31	15P1B21	WRITE*	89879100	2	2	
20P1A01	10P1B19	AUTOLOAD	89879100	1	1	
20P1A02	21P2B31	BEA	89879100	1	1	
20P1A03	26P2A11	CNS5M*	89879100	1	1	
20P1A04	26P2B13	CNS6M*	89879100	1	1	
20P1A06	25P2A11	CNS5L*	89879100	1	1	
20P1A07	25P2B12	CNS4L*	89879100	1	1	
20P1A08	21P2A24	TMSW*	89879100	1	1	
20P1A09	21P2A08	AUTRSW*	89879100	1	1	
20P1A10	21P1A07	SLK*	89879100	1	1	
20P1A11	21P1A18	PRGST	89879100	1	1	
20P1A13	25P2B14	CNS7L*	89879100	1	1	
20P1A14	26P1B31	CNSCM*	89879100	1	1	
20P1A15	26P1B28	CNS3M*	89879100	1	1	
20P1A18	25P1B29	CNS2L*	89879100	1	1	
20P1A20	25P1B28	CNS3L*	89879100	1	1	
20P1A21	22P2A17	RIND	89879100	1	1	
20P1A22	22P1A19	OPST	89879100	1	1	
20P1A23	21P1B17	SWEEP*	89879100	1	1	
20P1A24	21P1B18	ENTER*	89879100	1	1	
20P1A25	24P1B03	CSP*	89879100	1	1	
20P1A26	21P2A22	PCL*	89879100	1	1	
20P1A27	24P2A10	CSQ*	89879100	1	1	
20P1A28	30P1B23	CCPE*	89879100	1	1	
20P1A30	21P1B16	INT.SW*	89879100	1	1	
20P1A31	21P1A16	STOPCS*	89879100	1	1	
20P1B01	21P2A31	VCC	89879104			
20P1B03	26P2B12	CNS4M*	89879100	1	1	
20P1B04	21P1A12	32KW	89879100	1	1	
20P1B05	26P2B14	CNS7M*	89879100	1	1	
20P1B07	25P1A28	CLREG*	89879100	1	1	
20P1B08	21P2B27	MCCS*	89879100	1	1	
20P1B09	21P2A14	PRTSW	89879100	1	1	
20P1B10	23P1A04	CSPR	89879100	1	1	

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
20P1B12	24P2A04	CSM*	89879100	1	1
20P1B13	25P2B13	CNS6L*	89879100	1	1
20P1B14	26P1B29	CNS2M*	89879100	1	1
20P1B15	26P1A31	CNS1M*	89879100	1	1
20P1B17	25P1B31	CNSOL*	89879100	1	1
20P1B19	25P1A31	CNS1L*	89879100	1	1
20P1B22	21P2B13	PRF(PFIND)	89879100	1	1
20P1B23	23P1B23	OPIND	89879100	1	1
20P1B24	22P1B24	SLS	89879100	1	1
20P1B25	22P2A21	P4M	89879100	1	1
20P1B26	21P2A30	BEAC	89879100	1	1
20P1B27	24P2B20	CSA*	89879100	1	1
20P1B28	21P2A04	GOCSW*	89879100	1	1
20P1B29	23P1B29	CSY*	89879100	1	1
20P1B30	21P1A25	PRTBIT	89879100	1	1
20P1B31	22P1A31	CSX*	89879100	1	1
20P2A01	22P2A12	OVFL*	89879100	2	2
20P2A04	22P2B02	READ*	89879100	2	2
20P2A04	19P1B02	READ*	89879100	1	1
20P2A05	19P1A28	Q0	89879100	1	1
20P2A05	25P1B12	Q0	89879100	2	2
20P2A06	25P2A28	Q7	89879100	2	2
20P2A06	15P2B09	Q7	89879100	1	1
20P2A07	27P2B26	PEL*	89879100	2	2
20P2A07	21P1B06	PEL*	89879100	1	1
20P2A11	17P2B17	OA13*	89879100	2	2
20P2A11	26P2B24	OA13*	89879100	1	1
20P2A12	25P1B10	INT1L*	89879100	1	1
20P2A14	15P1A15	Q6	89879100	1	1
20P2A14	25P2B25	Q6	89879100	2	2
20P2A15	26P2B29	WEZM*	89879100	2	2
20P2A16	26P1A11	Q9	89879100	2	2
20P2A16	15P2B10	Q9	89879100	1	1
20P2A17	25P2B04	OA3*	89879100	1	1
20P2A17	17P2B06	OA3*	89879100	2	2
20P2A18	22P2A08	INDIND*	89879100	2	2
20P2A19	17P2B08	OA7*	89879100	2	2
20P2A19	25P2B22	OA7*	89879100	1	1
20P2A20	25P2A05	OA0*	89879100	1	1
20P2A20	17P2B04	OA0*	89879100	2	2
20P2A21	17P2A11	OA4*	89879100	2	2
20P2A21	25P2A23	OA4*	89879100	1	1
20P2A23	20P2A24	-12V	89879100	1	1
20P2A24	20P2A23	-12V	89879100	1	1
20P2B01	21P2A13	SG1*	89879100	2	2
20P2B02	21P2A05	GOCS	89879100	2	2
20P2B02	23P1B21	GOCS	89879100	1	1
20P2B03	22P2B18	FINT	89879100	2	2
20P2B04	23P2A29	RNI	89879100	2	2
20P2B04	21P1A17	RNI	89879100	1	1
20P2B05	21P1B25	CRQ*	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
20P2B06	19P2B31	WRITE*	89379100	1	1
20P2B06	22P2B01	WRITE*	89879100	2	2
20P2B07	25P2A24	Q4	89879100	2	2
20P2B07	15P1A14	Q4	89879100	1	1
20P2B08	25P1B20	MC*	89879100	1	1
20P2B08	21P2A27	MC*	89879100	2	2
20P2B12	19P1A03	REPLY*	89879100	2	2
20P2B12	22P2B25	REPLY*	89879100	1	1
20P2B13	22P2A24	REJECT*	89879100	1	1
20P2B13	19P1B01	REJECT*	89879100	2	2
20P2B14	26P1B12	Q8	89879100	2	2
20P2B14	15P2A09	Q8	89879100	1	1
20P2B15	15P1B14	Q5	89879100	1	1
20P2B15	25P2B28	Q5	89879100	2	2
20P2B16	26P1A08	Q10	89879100	2	2
20P2B16	15P2A10	Q10	89879100	1	1
20P2B18	25P2A22	DA6*	89879100	1	1
20P2B18	17P2B09	DA6*	89879100	2	2
20P2B19	17P2A01	DA2*	89879100	2	2
20P2B19	25P1A30	DA2*	89879100	1	1
20P2B20	25P2A02	DA1*	89879100	1	1
20P2B20	17P2A02	DA1*	89879100	2	2
20P2B22	17P2B10	DA5*	89879100	2	2
20P2B22	25P2B24	DA5*	89879100	1	1
20P2B23	26P2A05	DA8*	89879100	1	1
20P2B23	17P2A13	DA8*	89879100	2	2
20P2B24	17P2A12	DA9*	89879100	2	2
20P2B24	26P2A02	DA9*	89879100	1	1
20P2B25	23P2B31	CHI*	89879100	1	1
20P2B25	15P1B07	CHI*	89879100	2	2
20P2B26	17P2B22	DA10*	89879100	2	2
20P2B26	26P1A30	DA10*	89879100	1	1
20P2B27	29P2A16	VSS	89879100	1	1
20P2B28	26P2B04	DA11*	89879100	1	1
20P2B28	17P2A20	DA11*	89879100	2	2
21P1A01	23P2A10	I5	89879100	2	2
21P1A02	26P2A17	XGCM	89879100	1	1
21P1A03	25P2A17	XGOL	89879100	1	1
21P1A05	22P1A01	I7*	89879100	1	1
21P1A06	24P1B21	DBB	89879100	1	1
21P1A07	20P1A10	SLK*	89879100	1	1
21P1A08	24P1B22	X15	89879100	2	2
21P1A09	22P1A27	F1E1	89879100	2	2
21P1A10	22P2B19	KOVF	89879100	1	1
21P1A11	24P1A11	WRQ	89879100	1	1
21P1A11	22P2A10	WRQ	89879100	2	2
21P1A12	05P1A21	32KW	89879100	2	2
21P1A12	22P2A02	32KW	89879100	3	3
21P1A12	20P1B04	32KW	89879100	1	1
21P1A13	26P2B29	WEZM*	89879100	1	1
21P1A14	23P1A15	PH1	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
21P1A15	24P1B02	ENI	89879100	2	2
21P1A15	23P2B15	ENI	89879100	1	1
21P1A16	20P1A31	STOPCS*	89879100	1	1
21P1A17	20P2B04	RNI	89879100	1	1
21P1A17	22P1B20	RNI	89879100	2	2
21P1A18	20P1A11	PRGST	89879100	1	1
21P1A19	22P2B18	EINT	89879100	1	1
21P1A20	23P1A09	IRCK	89879100	2	2
21P1A21	26P1A23	PLM	89879100	1	1
21P1A22	25P1A02	GSL*	89879100	2	2
21P1A23	25P1B25	LCNL	89879100	2	2
21P1A24	25P2A12	GSM*	89879100	2	2
21P1A24	26P1A02	GSM*	89879100	1	1
21P1A25	20P1B30	PRTBIT	89879100	1	1
21P1A26	26P1B16	AM	89879100	1	1
21P1A27	24P1A03	FS*	89879100	1	1
21P1A28	23P1A20	KENI1*	89879100	1	1
21P1A30	23P2B18	R4	89879100	1	1
21P1A30	22P1B22	R4	89879100	2	2
21P1A31	25P2A07	MCNL	89879100	1	1
21P1B01	23P1B24	I4	89879100	1	1
21P1B02	26P2B18	XSQM	89879100	2	2
21P1B03	24P2B07	QSX	89879100	1	1
21P1B04	22P2A30	SKT	89879100	1	1
21P1B05	23P2B10	I6	89879100	2	2
21P1B06	20P2A07	PEL*	89879100	1	1
21P1B06	19P1A10	PEL*	89879100	2	2
21P1B07	22P2B07	Q3*	89879100	1	1
21P1B08	22P2A20	A7M	89879100	2	2
21P1B09	24P1B28	Q15	89879100	2	2
21P1B10	22P2A12	OVFL*	89879100	1	1
21P1B12	26P2B27	OVFW*	89879100	1	1
21P1B13	22P1B12	ODD*	89879100	1	1
21P1B13	23P2B19	ODD*	89879100	2	2
21P1B15	23P1A19	SS1	89879100	2	2
21P1B16	20P1A30	INT.SW*	89879100	1	1
21P1B17	20P1A23	SWEEP*	89879100	1	1
21P1B18	20P1A24	ENTER*	89879100	1	1
21P1B18	22P2B11	ENTER*	89879100	2	2
21P1B20	26P1B21	GLM	89879100	1	1
21P1B21	27P2B23	GPEC*	89879100	2	2
21P1B22	27P2B28	RGPWR	89879100	2	2
21P1B23	22P2A08	INDIND*	89879100	1	1
21P1B24	22P1A05	ENI20*	89879100	2	2
21P1B24	23P2A21	ENI20*	89879100	1	1
21P1B25	23P1B19	CRQ*	89879100	2	2
21P1B25	20P2B05	CRQ*	89879100	1	1
21P1B26	25P1B16	AL	89879100	2	2
21P1B27	25P1B08	Q30	89879100	1	1
21P1B28	22P2B14	KRNI1	89879100	2	2
21P1B29	26P1B26	LCNM	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
21P1B30	26P2A07	MCNM	89879100	2	2
21P1B31	25P2B03	GML	89879100	1	1
21P2A01	25P1A23	PLL	89879100	1	1
21P2A02	26P2A01	PMM	89879100	2	2
21P2A04	20P1B28	GOCSW*	89879100	1	1
21P2A05	24P2B25	GOCS	89879100	1	1
21P2A05	20P2B02	GOCS	89879100	2	2
21P2A06	23P2B25	KRNI	89879100	2	2
21P2A07	25P2B29	WEZL*	89879100	1	1
21P2A08	20P1A09	AUTRSW*	89879100	1	1
21P2A09	24P1A27	PEF*	89879100	2	2
21P2A10	23P2B17	FEO*	89879100	2	2
21P2A10	22P1A18	FEO*	89879100	1	1
21P2A11	27P2B11	NORMAL	89879100	2	2
21P2A12	27P1A27	MPRY	89879100	2	2
21P2A13	20P2B01	SG1*	89879100	2	2
21P2A13	23P2B22	SG1*	89879100	1	1
21P2A14	20P1B09	PRTSW	89879100	1	1
21P2A14	27P2B01	PRTSW	89879100	2	2
21P2A15	25P1B02	TAOL	89879100	2	2
21P2A16	25P1A25	ITA2L*	89879100	1	1
21P2A17	26P1A04	TA1M	89879100	1	1
21P2A18	25P1A24	ITA3L	89879100	2	2
21P2A19	27P1A26	MX17	89879100	2	2
21P2A20	25P2B10	ITA4L*	89879100	1	1
21P2A21	26P1B04	TA2M	89879100	2	2
21P2A22	20P1A26	PCL*	89879100	1	1
21P2A23	23P2A27	INR	89879100	1	1
21P2A24	20P1A08	TMSW*	89879100	1	1
21P2A25	23P2A13	JENI	89879100	1	1
21P2A26	24P1A15	DEL2	89879100	1	1
21P2A27	20P2B08	MC*	89879100	2	2
21P2A27	13P2B11	MC*	89879100	3	3
21P2A28	15P2B28	PRTAO*	89879100	1	1
21P2A29	26P1B20	CLRXM	89879100	1	1
21P2A30	20P1B26	BEAC	89879100	1	1
21P2A31	20P1B01	VCC	89879104		
21P2B01	25P2A01	PML	89879100	2	2
21P2B02	25P1B21	GLL	89879100	2	2
21P2B03	26P2B03	GMM	89879100	2	2
21P2B04	27P1A28	CVI01*	89879100	2	2
21P2B05	22P2B20	PH3	89879100	2	2
21P2B06	22P1B19	R3	89879100	2	2
21P2B06	23P2A28	R3	89879100	1	1
21P2B07	25P1A10	INTOL	89879100	1	1
21P2B08	23P1B01	DFEO	89879100	1	1
21P2B08	27P2B19	DFEO	89879100	2	2
21P2B09	22P1A19	OPST	89879100	2	2
21P2B10	23P1A23	CLRIR	89879100	1	1
21P2B11	23P2B11	ODD2*	89879100	1	1
21P2B12	23P2A15	CLREQ	89879100	2	2

	FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV	
	21P2B13	20P1B22	PRF(PFIND)	89879100	1	1	
	21P2B14	22P1A10	ENI4*	89879100	1	1	
	21P2B15	23P1A06	VIO*	89879100	1	1	
	21P2B16	26P1B02	TAOM	89879100	2	2	
	21P2B17	25P1A04	TA1L	89879100	1	1	
	21P2B18	22P2A19	JKCK	89879100	2	2	
	21P2B19	22P1A22	1E	89879100	2	2	
	21P2B20	25P1B04	TA2L	89879100	2	2	
	21P2B22	22P2B15	MPC	89879100	1	1	
	21P2B23	23P1B17	IO	89879100	1	1	
	21P2B24	27P1B30	PRTM*	89879100	2	2	
	21P2B25	24P1B06	PRY	89879100	1	1	
	21P2B26	27P2B30	32M	89879100	1	1	
	21P2B27	20P1B08	MCCS*	89879100	1	1	
	21P2B28	15P1A09	T.P.	89879100	1	1	
	21P2B29	22P2A23	MC	89879100	2	2	
	21P2B30	15P1A20	WEZ*	89879100	2	2	LENGTH 11"
SEE BELOW >	21P2B30	12P2A25	WEZ*	89879100	3	3	LENGTH 7"
	21P2B31	20P1A02	BEA	89879100	1	1	
	22P1A01	21P1A05	I7*	89879100	1	1	
	22P1A01	24P2A23	I7*	89879100	2	2	
	22P1A02	24P2A15	ITR	89879100	2	2	
	22P1A03	23P2B30	MDS	89879100	1	1	
	22P1A04	25P1B23	CO	89879100	2	2	
	22P1A05	21P1B24	ENI20*	89879100	2	2	
	22P1A05	24P1A07	ENI20*	89879100	1	1	
	22P1A06	23P2B24	OP20*	89879100	1	1	
	22P1A07	23P1B03	MMRQ	89879100	2	2	
	22P1A08	23P2B16	ENI3*	89879100	2	2	
	22P1A10	21P2B14	ENI4*	89879100	1	1	
	22P1A11	23P1B21	GOCS	89879100	2	2	
	22P1A12	27P1B26	CRI*	89879100	1	1	
	22P1A14	24P2A09	T3	89879100	1	1	
	22P1A15	24P1A14	DEL*	89879100	2	2	
	22P1A17	23P2A09	CNTE2*	89879100	1	1	
	22P1A18	21P2A10	FEO*	89879100	1	1	
	22P1A19	20P1A22	OPST	89879100	1	1	
	22P1A19	21P2B09	OPST	89879100	2	2	
	22P1A20	24P2B29	F1E23	89879100	1	1	
	22P1A21	25P2A30	AQC*	89879100	2	2	
	22P1A22	21P2B19	1E	89879100	2	2	
	22P1A23	24P1A28	R2	89879100	2	2	
	22P1A24	24P1B27	R1	89879100	2	2	
	22P1A25	28P1A12	SPBM*	89879100	2	2	
	22P1A26	23P2B14	EAD*	89879100	2	2	
	22P1A27	21P1A09	F1E1	89879100	2	2	
	22P1A28	23P1B22	ODD2	89879100	2	2	
	22P1A30	23P1A25	IN41	89879100	1	1	
	22P1A31	20P1B31	CSX*	89879100	1	1	
	22P1A31	24P2A21	CSX*	89879100	2	2	
	22P1B01	25P1A01	C2	89879100	2	2	
	> 21P2B30	19P1A02	WEZ*		1	1	LENGTH 14"

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
22P1B02	24P2A22	I65	89879100	2	2
22P1B03	24P1B31	02*	89879100	1	1
22P1B04	25P2B31	C3	89879100	1	1
22P1B05	23P2B07	N41	89879100	1	1
22P1B06	24P2B11	SHI	89879100	1	1
22P1B07	25P1A13	CLRQ*	89879100	1	1
22P1B08	23P1B27	EXT	89879100	1	1
22P1B09	25P2A10	C1	89879100	1	1
22P1B10	24P2A01	OD*	89879100	2	2
22P1B12	24P1B09	ODD*	89879100	2	2
22P1B12	21P1B13	ODD*	89879100	1	1
22P1B13	24P1A13	MDS1	89879100	2	2
22P1B14	23P1A27	OP	89879100	1	1
22P1B15	24P1B18	ENI2E*	89879100	1	1
22P1B16	24P2B06	T4	89879100	2	2
22P1B17	28P1B13	CPBM*	89879100	2	2
22P1B18	23P2B20	FIEF	89879100	2	2
22P1B19	21P2B06	R3	89879100	2	2
22P1B19	24P1A24	R3	89879100	1	1
22P1B20	21P1A17	RNI	89879100	2	2
22P1B22	21P1A30	R4	89879100	2	2
22P1B22	24P1B23	R4	89879100	1	1
22P1B23	23P2A27	INR	89879100	2	2
22P1B24	20P1B24	SLS	89879100	1	1
22P1B25	24P1B12	WE*	89879100	1	1
22P1B26	23P2B26	RNI21*	89879100	2	2
22P1B27	23P1A21	INO	89879100	1	1
22P1B28	24P1A12	WXL1*	89879100	2	2
22P1B29	23P2A07	IN32	89879100	2	2
22P2A02	21P1A12	32KW	89879100	3	3
22P2A02	23P2B08	32KW	89879100	2	2
22P2A04	26P1A22	SE	89879100	2	2
22P2A05	25P1A18	XFZ	89879100	2	2
22P2A06	23P2B28	RNI12*	89879100	2	2
22P2A07	23P1B15	WXM	89879100	1	1
22P2A08	21P1B23	INDIND*	89879100	1	1
22P2A08	20P2A18	INDIND*	89879100	2	2
22P2A09	26P1A17	SIM	89879100	1	1
22P2A10	21P1A11	WRQ	89879100	2	2
22P2A11	23P2B01	MD1*	89879100	1	1
22P2A12	21P1B10	OVFL*	89879100	1	1
22P2A12	20P2A01	OVFL*	89879100	2	2
22P2A13	23P2B09	JITR*	89879100	2	2
22P2A15	23P1B10	WXL	89879100	2	2
22P2A16	23P2B13	SHADR	89879100	1	1
22P2A17	20P1A21	RIND	89879100	1	1
22P2A18	23P2A05	JCP2	89879100	2	2
22P2A19	21P2B18	JKCK	89879100	2	2
22P2A19	23P2B05	JKCK	89879100	1	1
22P2A20	21P1B08	A7M	89879100	2	2
22P2A20	26P2B23	A7M	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
22P2A21	20P1B25	P4M	89879100	1	1
22P2A21	27P2A15	P4M	89879100	2	2
22P2A22	24P1A08	RP	89879100	2	2
22P2A23	21P2B29	MC	89879100	2	2
22P2A23	25P2B30	MC	89879100	1	1
22P2A24	20P2B13	REJECT*	89879100	1	1
22P2A25	24P1B17	IRJ*	89879100	2	2
22P2A26	23P1B16	GOAQ*	89879100	1	1
22P2A27	24P1B25	BB	89879100	1	1
22P2A28	26P2B08	AUG7M	89879100	2	2
22P2A29	25P2A04	ALU7AM	89879104		
22P2A30	21P1B04	SKT	89879100	1	1
22P2B01	20P2B06	WRITE*	89879100	2	2
22P2B02	20P2A04	READ*	89879100	2	2
22P2B03	24P2A07	M	89879100	1	1
22P2B04	24P1B08	RNI11*	89879100	1	1
22P2B04	23P2B27	RNI11*	89879100	2	2
22P2B05	25P1B22	SFL	89879100	1	1
22P2B07	21P1B07	03*	89879100	1	1
22P2B07	24P2B01	03*	89879100	2	2
22P2B08	23P2B02	F23	89879100	1	1
22P2B10	23P2A24	JRNI*	89879100	1	1
22P2B11	21P1B18	ENTER*	89879100	2	2
22P2B12	23P2B04	JOP	89879100	1	1
22P2B13	23P2A23	KITR	89879100	1	1
22P2B14	21P1B28	KRNI1	89879100	2	2
22P2B15	23P1A26	MPC	89879100	2	2
22P2B15	21P2B22	MPC	89879100	1	1
22P2B16	24P1B30	01*	89879100	2	2
22P2B17	23P1B26	X15	89879100	2	2
22P2B18	20P2B03	EINT	89879100	2	2
22P2B18	21P1A19	EINT	89879100	1	1
22P2B19	21P1A10	KOVF	89879100	1	1
22P2B20	21P2B05	PH3	89879100	2	2
22P2B20	23P1A22	PH3	89879100	1	1
22P2B22	23P1A31	ADR*	89879100	1	1
22P2B23	26P2A09	ZITSH	89879100	1	1
22P2B24	24P1A19	PTADD	89879100	2	2
22P2B25	20P2B12	REPLY*	89879100	1	1
22P2B26	24P2A12	SO	89879100	2	2
22P2B27	24P2A28	BX15	89879100	2	2
22P2B28	26P2A14	ADD7M	89879100	1	1
22P2B29	23P1B08	PH2	89879100	1	1
22P2B30	24P2B10	DELTAUG*	89879100	2	2
23P1A01	27P2A30	VCC2	89879100	1	1
23P1A02	26P2A19	XSEL7M	89879100	2	2
23P1A03	24P1B26	CRQ	89879104		
23P1A04	20P1B10	CSPR	89879100	1	1
23P1A05	33P2B11	GCM2	89879104		
23P1A06	21P2B15	VIO*	89879100	1	1
23P1A07	27P2A23	OSC*	89879104		

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
23P1A08	27P2B09	GOM1	89879104		
23P1A09	24P1A21	IRCK	89879100	1	1
23P1A09	21P1A20	IRCK	89879100	2	2
23P1A10	25P1A15	XLCK	89879100	2	2
23P1A11	25P1A14	QCK	89879100	1	1
23P1A12	25P1A20	YCK	89879100	2	2
23P1A13	24P1B04	WP	89879100	1	1
23P1A14	24P2A26	WA	89879100	2	2
23P1A15	21P1A14	PH1	89879100	2	2
23P1A16	24P1B24	AD1	89879100	1	1
23P1A17	24P1B10	I2	89879100	2	2
23P1A19	21P1B15	SS1	89879100	2	2
23P1A20	21P1A28	KENI1*	89879100	1	1
23P1A21	22P1B27	INO	89879100	1	1
23P1A22	22P2B20	PH3	89879100	1	1
23P1A23	24P1A31	CLRIR	89879100	2	2
23P1A23	21P2B10	CLRIR	89879100	1	1
23P1A24	24P2B07	ADY*	89879100	1	1
23P1A25	22P1A30	IN41	89879100	1	1
23P1A26	22P2B15	MPC	89879100	2	2
23P1A27	22P1B14	OP	89879100	1	1
23P1A28	24P2B04	MDS2	89879100	2	2
23P1A30	25P1B17	YTAUG	89879100	2	2
23P1A31	24P1B07	ACR*	89879100	2	2
23P1A31	22P2B22	ACR*	89879100	1	1
23P1B01	21P2B08	DFEO	89879100	1	1
23P1B03	22P1A07	MMRQ	89879100	2	2
23P1B05	24P1A10	I3	89879100	1	1
23P1B08	22P2B29	PH2	89879100	1	1
23P1B09	26P1A15	XMCK	89879100	1	1
23P1B10	22P2A15	WXL	89879100	2	2
23P1B11	27P2B21	GND	89879104		
23P1B12	24P1B29	WQ	89879100	1	1
23P1B13	25P1B13	PCK	89879100	2	2
23P1B14	25P1B19	ALCK	89879100	1	1
23P1B15	22P2AC7	WXM	89879100	1	1
23P1B16	22P2A26	GOAQ*	89879100	1	1
23P1B17	21P2B23	IO	89879100	1	1
23P1B17	24P1B13	IO	89879100	2	2
23P1B18	24P1B05	I1	89879100	1	1
23P1B19	25P1B03	CRQ*	89879100	1	1
23P1B19	21P1B25	CRQ*	89879100	2	2
23P1B20	24P1A26	AD2	89879100	2	2
23P1B21	22P1A11	GOCS	89879100	2	2
23P1B21	20P2B02	GOCS	89879100	1	1
23P1B22	24P1A02	ODD2	89879100	1	1
23P1B22	22P1A28	ODD2	89879100	2	2
23P1B23	20P1B23	OPIND	89879100	1	1
23P1B24	21P1B01	I4	89879100	1	1
23P1B24	24P2B26	I4	89879100	2	2
23P1B26	22P2B17	X15	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
23P1B26	24P1B22	X15	89879100	1	1
23P1B27	22P1B08	EXT	89879100	1	1
23P1B28	24P2A14	NO	89879100	2	2
23P1B29	20P1B29	CSY*	89879100	1	1
23P1B30	24P1A22	BBCK	89879100	2	2
23P1B31	24P2B12	MD21*	89879100	2	2
23P2A01	24P2B13	WSA*	89879100	2	2
23P2A02	24P1A13	MDS1	89879100	1	1
23P2A04	24P2B28	OPE*	89879100	1	1
23P2A05	22P2A18	JOP2	89879100	2	2
23P2A07	22P1B29	IN32	89879100	2	2
23P2A08	24P2B27	MDSO	89879100	1	1
23P2A09	24P2A30	CNTE2*	89879100	2	2
23P2A09	22P1A17	CNTE2*	89879100	1	1
23P2A10	21P1A01	I5	89879100	2	2
23P2A10	24P2B24	I5	89879100	1	1
23P2A11	26P1B19	AMCK	89879100	2	2
23P2A12	24P1B27	R1	89879100	1	1
23P2A13	21P2A25	JENI	89879100	1	1
23P2A14	25P1A22	SGL	89879100	1	1
23P2A15	21P2B12	CLREQ	89879100	2	2
23P2A16	24P2B16	OI6*	89879100	1	1
23P2A17	24P2B18	EI5*	89879100	2	2
23P2A19	24P2B15	RE1F	89879100	1	1
23P2A20	24P1B18	ENI2E*	89879100	2	2
23P2A21	21P1B24	ENI20*	89879100	1	1
23P2A22	25P2A13	MCK	89879100	2	2
23P2A23	22P2B13	KITR	89879100	1	1
23P2A24	22P2B10	JRNI*	89879100	1	1
23P2A24	24P1A04	JRNI*	89879100	2	2
23P2A25	24P1A05	RNI22*	89879100	1	1
23P2A26	24P2A27	RE18*	89879100	2	2
23P2A27	22P1B23	INR	89879100	2	2
23P2A27	21P2A23	INR	89879100	1	1
23P2A28	21P2B06	R3	89879100	1	1
23P2A29	20P2B04	RNI	89879100	2	2
23P2A30	24P2B01	03*	89879100	1	1
23P2B01	22P2A11	MD1*	89879100	1	1
23P2B01	24P2A11	MD1*	89879100	2	2
23P2B02	22P2B08	F23	89879100	1	1
23P2B03	24P1B01	MDSE	89879100	1	1
23P2B04	22P2B12	JOP	89879100	1	1
23P2B05	22P2A19	JKCK	89879100	1	1
23P2B06	24P1A06	OPO*	89879100	2	2
23P2B07	24P2B14	N41	89879100	2	2
23P2B07	22P1B05	N41	89879100	1	1
23P2B08	26P2A29	32KW	89879100	1	1
23P2B08	22P2A02	32KW	89879100	2	2
23P2B09	22P2A13	JITR*	89879100	2	2
23P2B10	21P1B05	I6	89879100	2	2
23P2B10	24P2B23	I6	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
23P2B11	21P2B11	ODD2*	89879100	1	1
23P2B12	24P1A28	R2	89879100	1	1
23P2B13	22P2A16	SHADR	89879100	1	1
23P2B14	22P1A26	EAD*	89879100	2	2
23P2B15	21P1A15	ENI	89879100	1	1
23P2B16	22P1A08	ENI3*	89879100	2	2
23P2B17	21P2A10	FEO*	89879100	2	2
23P2B18	21P1A30	R4	89879100	1	1
23P2B19	21P1B13	ODD*	89879100	2	2
23P2B20	22P1B18	FIEF	89879100	2	2
23P2B22	21P2A13	SG1*	89879100	1	1
23P2B23	24P2B03	WM	89879100	1	1
23P2B24	22P1A06	OP20*	89879100	1	1
23P2B25	21P2A06	KRNI	89879100	2	2
23P2B26	22P1B26	RNI21*	89879100	2	2
23P2B26	24P2A29	RNI21*	89879100	1	1
23P2B27	22P2B04	RNI11*	89879100	2	2
23P2B28	22P2A06	RNI12*	89879100	2	2
23P2B28	24P2B30	RNI12*	89879100	1	1
23P2B29	24P2A15	ITR	89879100	1	1
23P2B30	22P1A03	MDS	89879100	1	1
23P2B31	20P2B25	CHI*	89879100	1	1
24P1A02	23P1B22	ODD2	89879100	1	1
24P1A03	21P1A27	FS*	89879100	1	1
24P1A04	23P2A24	JRNI*	89879100	2	2
24P1A05	23P2A25	RNI22*	89879100	1	1
24P1A06	23P2B06	OPO*	89879100	2	2
24P1A07	22P1A05	ENI20*	89879100	1	1
24P1A08	22P2A22	RP	89879100	2	2
24P1A09	25P1A09	XTADD	89879100	1	1
24P1A10	23P1B05	I3	89879100	1	1
24P1A11	21P1A11	WRQ	89879100	1	1
24P1A12	22P1B28	WXL1*	89879100	2	2
24P1A13	22P1B13	MDS1	89879100	2	2
24P1A13	23P2A02	MDS1	89879100	1	1
24P1A14	22P1A15	DEL*	89879100	2	2
24P1A15	21P2A26	DEL2	89879100	1	1
24P1A16	25P1A19	MX1L	89879100	1	1
24P1A17	25P1B14	MTADD	89879100	2	2
24P1A18	25P1B15	MX2L	89879100	1	1
24P1A19	25P1A12	PTADD	89879100	1	1
24P1A19	22P2B24	PTADD	89879100	2	2
24P1A20	25P1A16	MX3L	89879100	1	1
24P1A21	23P1A09	IRCK	89879100	1	1
24P1A22	23P1B30	BBCK	89879100	2	2
24P1A23	26P1A19	MX1M	89879100	1	1
24P1A24	22P1B19	R3	89879100	1	1
24P1A25	26P1B18	MXOM	89879100	1	1
24P1A26	23P1B20	AD2	89879100	2	2
24P1A27	21P2A09	PEF*	89879100	2	2
24P1A28	22P1A23	R2	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
24P1A28	23P2B12	R2	89879100	1	1
24P1A31	23P1A23	CLRIR	89879100	2	2
24P1B01	23P2B03	MDSE	89879100	1	1
24P1B02	21P1A15	ENI	89879100	2	2
24P1B03	20P1A25	CSP*	89879100	1	1
24P1B04	23P1A13	WP	89879100	1	1
24P1B05	23P1B18	I1	89879100	1	1
24P1B06	21P2B25	PRY	89879100	1	1
24P1B07	23P1A31	ADR*	89879100	2	2
24P1B08	22P2B04	RNI11*	89879100	1	1
24P1B09	22P1B17	ODD*	89879100	2	2
24P1B10	23P1A17	I2	89879100	2	2
24P1B12	27P1A30	WE*	89879100	2	2
24P1B12	22P1B25	WE*	89879100	1	1
24P1B13	23P1B17	IO	89879100	2	2
24P1B14	26P1B15	MX2M	89879100	1	1
24P1B15	26P1A16	MX3M	89879100	1	1
24P1B16	25P1B18	MXOL	89879100	1	1
24P1B17	22P2A25	IRJ*	89879100	2	2
24P1B18	23P2A20	ENI2E*	89879100	2	2
24P1B18	22P1B15	ENI2E*	89879100	1	1
24P1B19	25P1A17	SIL	89879100	2	2
24P1B20	27P2B20	MDEL	89879100	2	2
24P1B21	21P1A06	DBB	89879100	1	1
24P1B22	23P1B26	X15	89879100	1	1
24P1B22	21P1A08	X15	89879100	2	2
24P1B23	22P1B22	R4	89879100	1	1
24P1B24	23P1A16	AD1	89879100	1	1
24P1B25	22P2A27	BB	89879100	1	1
24P1B26	23P1A03	CRQ	89879104		
24P1B26	27P2A09	CRQ	89879104		
24P1B27	23P2A12	R1	89879100	1	1
24P1B27	22P1A24	R1	89879100	2	2
24P1B28	21P1B09	Q15	89879100	2	2
24P1B28	26P2A28	Q15	89879100	1	1
24P1B29	23P1B12	WQ	89879100	1	1
24P1B30	22P2B16	O1*	89879100	2	2
24P1B31	22P1B03	O2*	89879100	1	1
24P2A01	22P1B10	OD*	89879100	2	2
24P2A02	25P2A27	AO*	89879100	2	2
24P2A04	20P1B12	CSM*	89879100	1	1
24P2A05	26P2B19	MX7M	89879100	1	1
24P2A07	22P2B03	M	89879100	1	1
24P2A07	25P2B07	M	89879100	2	2
24P2A08	26P2B20	MX5M	89879100	1	1
24P2A09	22P1A14	T3	89879100	1	1
24P2A10	20P1A27	CSQ*	89879100	1	1
24P2A11	23P2B01	MD1*	89879100	2	2
24P2A12	22P2B26	SQ	89879100	2	2
24P2A12	25P2A08	SO	89879100	1	1
24P2A13	25P1B25	S3	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
24P2A14	23P1B28	NO	89879100	2	2
24P2A15	22P1A07	ITR	89879100	2	2
24P2A15	23P2B29	ITR	89879100	1	1
24P2A16	25P2B19	MX7L	89879100	1	1
24P2A17	25P1A26	S2	89879100	1	1
24P2A18	25P2B09	S1	89879100	1	1
24P2A19	25P2A18	MX6L	89879100	1	1
24P2A20	26P2A25	XTAUGM	89879100	2	2
24P2A21	22P1A31	CSX*	89879100	2	2
24P2A22	22P1B02	I65	89879100	2	2
24P2A23	22P1A01	I7*	89879100	2	2
24P2A24	25P2A21	ATAUG	89879100	1	1
24P2A26	23P1A14	WA	89879100	2	2
24P2A27	23P2A26	RE18*	89879100	2	2
24P2A28	22P2B27	BX15	89879100	2	2
24P2A29	23P2B26	RNI21*	89879100	1	1
24P2A30	23P2A09	CNTE2*	89879100	2	2
24P2B01	22P2B07	03*	89879100	2	2
24P2B01	23P2A30	03*	89879100	1	1
24P2B02	21P1B03	QSX	89879100	1	1
24P2B02	25P2A06	QSX	89879100	2	2
24P2B03	23P2B23	WM	89879100	1	1
24P2B04	23P1A28	MDS2	89879100	2	2
24P2B05	26P2A20	MX4M	89879100	1	1
24P2B06	22P1B16	T4	89879100	2	2
24P2B07	23P1A24	ADY*	89879100	1	1
24P2B08	26P2A18	MX6M	89879100	1	1
24P2B10	25P2B16	DELTAUG*	89879100	1	1
24P2B10	22P2B30	DELTAUG*	89879100	2	2
24P2B11	22P1B06	SHI	89879100	1	1
24P2B12	23P1B31	MD21*	89879100	2	2
24P2B13	23P2A01	W9A*	89879100	2	2
24P2B14	23P2B07	N41	89879100	2	2
24P2B15	23P2A19	RE1F	89879100	1	1
24P2B16	23P2A16	OI6*	89879100	1	1
24P2B17	25P2B20	MX5L	89879100	1	1
24P2B18	23P2A17	EI5*	89879100	2	2
24P2B19	25P2A20	MX4L	89879100	1	1
24P2B20	20P1B27	CSA*	89879100	1	1
24P2B22	25P2A26	QTADD	89879100	1	1
24P2B23	23P2B10	I6	89879100	1	1
24P2B24	23P2A10	I5	89879100	1	1
24P2B25	21P2A05	GOCS	89879100	1	1
24P2B26	23P1B24	I4	89879100	2	2
24P2B27	23P2A08	MDSO	89879100	1	1
24P2B28	23P2A04	OPE*	89879100	1	1
24P2B29	22P1A20	F1E23	89879100	1	1
24P2B30	23P2B28	RNI12*	89879100	1	1
24P2B31	25P2A25	XTAUGL	89879100	1	1
25P1A01	26P1A01	C2	89879100	1	1
25P1A01	22P1B01	C2	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
25P1A02	21P1A22	GSL*	89879100	2	2
25P1A04	21P2B17	TA1L	89879100	1	1
25P1A08	19P2B01	Q2	89879100	2	2
25P1A09	26P1A09	XTADD	89879100	2	2
25P1A09	24P1A09	XTADD	89879100	1	1
25P1A10	21P2B07	INTOL	89879100	1	1
25P1A11	19P2B02	Q1	89879100	1	1
25P1A12	24P1A19	PTADD	89879100	1	1
25P1A12	26P1A12	PTADD	89879100	2	2
25P1A13	26P1A13	CLRQ*	89879100	2	2
25P1A13	22P1B07	CLRQ*	89879100	1	1
25P1A14	26P1A14	QCK	89879100	2	2
25P1A14	23P1A11	QCK	89879100	1	1
25P1A15	23P1A10	XLCK	89879100	2	2
25P1A16	27P1A06	MX3L	89879100	2	2
25P1A16	24P1A20	MX3L	89879100	1	1
25P1A17	24P1B19	SIL	89879100	2	2
25P1A18	22P2A05	XEZ	89879100	2	2
25P1A18	26P1A18	XEZ	89879100	1	1
25P1A19	24P1A16	MX1L	89879100	1	1
25P1A19	27P1B03	MX1L	89879100	2	2
25P1A20	23P1A12	YCK	89879100	2	2
25P1A20	26P1A20	YCK	89879100	1	1
25P1A21	28P1A10	ALU3L	89879100	2	2
25P1A22	23P2A14	SGL	89879100	1	1
25P1A23	21P2A01	PLL	89879100	1	1
25P1A24	21P2A18	ITA3L	89879100	2	2
25P1A25	21P2A16	ITA2L*	89879100	1	1
25P1A26	24P2A17	S2	89879100	1	1
25P1A26	26P1A26	S2	89879100	2	2
25P1A28	26P1A28	CLREG*	89879100	2	2
25P1A28	20P1B07	CLREG*	89879100	1	1
25P1A30	20P2B19	OA2*	89879100	1	1
25P1A31	20P1B19	CNS1L*	89879100	1	1
25P1B01	26P1A03	CI	89879100	2	2
25P1B02	21P2A15	TAOL	89879100	2	2
25P1B03	26P1B03	CRQ*	89879100	2	2
25P1B03	23P1B19	CRQ*	89879100	1	1
25P1B04	21P2B20	TA2L	89879100	2	2
25P1B08	26P1B08	Q3O	89879100	2	2
25P1B08	21P1B27	Q3O	89879100	1	1
25P1B09	15P1B13	Q3	89879100	1	1
25P1B10	20P2A12	INT1L*	89879100	1	1
25P1B12	20P2A05	QO	89879100	2	2
25P1B13	23P1B13	PCK	89879100	2	2
25P1B13	26P1B13	PCK	89879100	1	1
25P1B14	26P1B14	MTADD	89879100	1	1
25P1B14	24P1A17	MTADD	89879100	2	2
25P1B15	27P1A04	MX2L	89879100	2	2
25P1B15	24P1A18	MX2L	89879100	1	1
25P1B16	21P1B26	AL	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
25P1B17	23P1A30	YTAUG	89879100	2	2
25P1B17	26P1B17	YTAUG	89879100	1	1
25P1B18	24P1B16	MXOL	89879100	1	1
25P1B18	27P1B02	MXOL	89879100	2	2
25P1B19	23P1B14	ALCK	89879100	1	1
25P1B20	20P2B08	MC*	89879100	1	1
25P1B20	15P1B23	MC*	89879100	3	3
25P1B21	21P2B02	GLL	89879100	2	2
25P1B22	22P2B05	SFL	89879100	1	1
25P1B23	26P1B23	CO	89879100	1	1
25P1B23	22P1A04	CO	89879100	2	2
25P1B24	28P1B12	ALUOL	89879100	2	2
25P1B25	26P1B25	S3	89879100	2	2
25P1B25	24P2A13	S3	89879100	1	1
25P1B26	21P1A23	LCNL	89879100	2	2
25P1B27	28P1B10	ALU2L	89879100	2	2
25P1B28	20P1A20	CNS3L*	89879100	1	1
25P1B29	20P1A18	CNS2L*	89879100	1	1
25P1B30	28P1A11	ALU1L	89879100	2	2
25P1B31	20P1B17	CNSOL*	89879100	1	1
25P2A01	21P2B01	PML	89879100	2	2
25P2A02	20P2B20	OA1*	89879100	1	1
25P2A04	26P2B02	ALU7AM	89879100	1	1
25P2A04	22P2A29	ALU7AM	89879104		
25P2A05	20P2A20	OA0*	89879100	1	1
25P2A06	26P2A06	QSX	89879100	1	1
25P2A06	24P2B02	QSX	89879100	2	2
25P2A07	21P1A31	MCNL	89879100	1	1
25P2A08	24P2A12	SO	89879100	1	1
25P2A08	26P2A08	SO	89879100	2	2
25P2A09	25P2B11	ALUOAM	89879100	2	2
25P2A09	26P1A27	ALUOAM	89879100	1	1
25P2A10	26P2A10	C1	89879100	2	2
25P2A10	22P1B09	C1	89879100	1	1
25P2A11	20P1A06	CNS5L*	89879100	1	1
25P2A12	21P1A24	GSM*	89879100	2	2
25P2A13	23P2A22	MCK	89879100	2	2
25P2A13	26P2A13	MCK	89879100	1	1
25P2A15	28P2A12	ALU6L	89879100	2	2
25P2A16	28P2A15	ALU5L	89879100	2	2
25P2A17	21P1A03	XGQL	89879100	1	1
25P2A18	24P2A19	MX6L	89879100	1	1
25P2A18	27P1A11	MX6L	89879100	2	2
25P2A20	27P1B08	MX4L	89879100	2	2
25P2A20	24P2B19	MX4L	89879100	1	1
25P2A21	24P2A24	ATAUG	89879100	1	1
25P2A21	26P2A21	ATAUG	89879100	2	2
25P2A22	20P2B18	OA6*	89879100	1	1
25P2A23	20P2A21	OA4*	89879100	1	1
25P2A24	20P2B07	Q4	89879100	2	2
25P2A25	24P2B31	XTAUGL	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
25P2A26	24P2B22	QTADD	89879100	1	1
25P2A26	26P2A26	QTADD	89879100	2	2
25P2A27	24P2A02	AD*	89879100	2	2
25P2A28	20P2A06	Q7	89879100	2	2
25P2A30	22P1A21	ACC*	89879100	2	2
25P2A30	26P2A30	ACC*	89879100	1	1
25P2B02	26P2A04	ALU7AL	89879100	1	1
25P2B03	21P1B31	GML	89879100	1	1
25P2B04	20P2A17	DA3*	89879100	1	1
25P2B05	26P2B26	SHAM	89879100	2	2
25P2B06	26P2B16	HIGH	89879100	1	1
25P2B07	24P2A07	M	89879100	2	2
25P2B07	26P2B07	M	89879100	1	1
25P2B09	24P2A18	S1	89879100	1	1
25P2B09	26P2B09	S1	89879100	2	2
25P2B10	21P2A20	ITA4L*	89879100	1	1
25P2B11	25P2A09	ALUCAM	89879100	2	2
25P2B12	20P1A07	CNS4L*	89879100	1	1
25P2B13	20P1B13	CNS6L*	89879100	1	1
25P2B14	20P1A13	CNS7L*	89879100	1	1
25P2B15	28P2A09	ALU7L	89879100	2	2
25P2B16	24P2B10	DELTAUG*	89879100	1	1
25P2B17	28P2A17	ALU4L	89879100	2	2
25P2B19	27P1B13	MX7L	89879100	2	2
25P2B19	24P2A16	MX7L	89879100	1	1
25P2B20	24P2B17	MX5L	89879100	1	1
25P2B20	27P1A09	MX5L	89879100	2	2
25P2B22	20P2A19	DA7*	89879100	1	1
25P2B24	20P2B22	DA5*	89879100	1	1
25P2B25	20P2A14	Q6	89879100	2	2
25P2B26	26P2B11	SHAL	89879100	1	1
25P2B28	20P2B15	Q5	89879100	2	2
25P2B29	21P2A07	WEZL*	89879100	1	1
25P2B30	26P2B30	MC	89879100	2	2
25P2B30	22P2A23	MC	89879100	1	1
25P2B31	26P2B31	C3	89879100	2	2
25P2B31	22P1B04	C3	89879100	1	1
26P1A01	25P1A01	C2	89879100	1	1
26P1A02	21P1A24	GSM*	89879100	1	1
26P1A03	25P1B01	CI	89879100	2	2
26P1A04	21P2A17	TA1M	89879100	1	1
26P1A08	20P2B16	Q10	89879100	2	2
26P1A09	25P1A09	XTADD	89879100	2	2
26P1A11	20P2A16	Q9	89879100	2	2
26P1A12	25P1A12	PTADD	89879100	2	2
26P1A13	25P1A13	CLRC*	89879100	2	2
26P1A14	25P1A14	QCK	89879100	2	2
26P1A15	23P1B09	XMCK	89879100	1	1
26P1A16	24P1B15	MX3M	89879100	1	1
26P1A16	27P1B19	MX3M	89879100	2	2
26P1A17	22P2A09	SIM	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
26P1A18	25P1A18	XFZ	89879100	1	1
26P1A19	24P1A23	MX1M	89879100	1	1
26P1A19	27P1A15	MX1M	89879100	2	2
26P1A20	25P1A20	YCK	89879100	1	1
26P1A21	28P1B28	ALU3M	89879100	2	2
26P1A22	22P2A04	SE	89879100	2	2
26P1A22	26P1B22	SE	89879100	1	1
26P1A23	21P1A21	PLM	89879100	1	1
26P1A24	26P1A25	HIGH	89879100	1	1
26P1A25	26P1A24	HIGH	89879100	1	1
26P1A25	26P2A12	HIGH	89879100	2	2
26P1A26	25P1A26	S2	89879100	2	2
26P1A27	25P2A09	ALUCAM	89879100	1	1
26P1A28	25P1A28	CLREG*	89879100	2	2
26P1A30	20P2B26	OA1C*	89879100	1	1
26P1A31	20P1B15	CNS1M*	89879100	1	1
26P1B02	21P2B16	TAOM	89879100	2	2
26P1B03	25P1B03	CRQ*	89879100	2	2
26P1B04	21P2A21	TA2M	89879100	2	2
26P1B08	25P1B08	Q30	89879100	2	2
26P1B09	15P1B17	Q11	89879100	1	1
26P1B12	20P2B14	Q8	89879100	2	2
26P1B13	25P1B13	PCK	89879100	1	1
26P1B14	25P1B14	MTADD	89879100	1	1
26P1B15	24P1B14	MX2M	89879100	1	1
26P1B15	27P1B17	MX2M	89879100	2	2
26P1B16	21P1A26	AM	89879100	1	1
26P1B17	25P1B17	YTAUG	89879100	1	1
26P1B18	24P1A25	MXOM	89879100	1	1
26P1B18	27P1A14	MXOM	89879100	2	2
26P1B19	23P2A11	AMCK	89879100	2	2
26P1B20	21P2A29	CLRXM	89879100	1	1
26P1B21	21P1B20	GLM	89879100	1	1
26P1B22	26P1A22	SE	89879100	1	1
26P1B23	25P1B23	CO	89879100	1	1
26P1B24	28P1A28	ALUCM	89879100	2	2
26P1B25	25P1B25	S3	89879100	2	2
26P1B26	21P1B29	LCNM	89879100	2	2
26P1B27	28P1A27	ALU2M	89879100	2	2
26P1B28	20P1A15	CNS3M*	89879100	1	1
26P1B29	20P1B14	CNS2M*	89879100	1	1
26P1B30	28P1A22	ALU1M	89879100	2	2
26P1B31	20P1A14	CNSCM*	89879100	1	1
26P2A01	21P2A02	PMM	89879100	2	2
26P2A02	20P2B24	OA9*	89879100	1	1
26P2A04	25P2B02	ALU7AL	89879100	1	1
26P2A04	26P2B05	ALU7AL	89879100	2	2
26P2A05	20P2B23	OA8*	89879100	1	1
26P2A06	25P2A06	QSX	89879100	1	1
26P2A07	21P1B30	MCNM	89879100	2	2
26P2A08	25P2AC8	SO	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
26P2A09	22P2B23	Z1TSH	89879100	1	1
26P2A10	25P2A10	C1	89879100	2	2
26P2A11	20P1A03	CNS5M*	89879100	1	1
26P2A12	26P1A25	HIGH	89879100	2	2
26P2A12	26P2B10	HIGH	89879100	1	1
26P2A13	25P2A13	MCK	89879100	1	1
26P2A14	22P2B28	ADD7M	89879100	1	1
26P2A15	28P2B16	ALU6M	89879100	2	2
26P2A16	28P2B09	ALU5M	89879100	2	2
26P2A17	21P1A07	XGQM	89879100	1	1
26P2A18	24P2B08	MX6M	89879100	1	1
26P2A18	27P1A22	MX6M	89879100	2	2
26P2A19	23P1A07	XSEL7M	89879100	2	2
26P2A20	27P1B21	MX4M	89879100	2	2
26P2A20	24P2B05	MX4M	89879100	1	1
26P2A21	25P2A21	ATAUG	89879100	2	2
26P2A22	17P2B16	OA14*	89879100	2	2
26P2A23	17P2A19	OA12*	89879100	2	2
26P2A24	15P1A18	Q12	89879100	1	1
26P2A25	24P2A20	XTAUGM	89879100	2	2
26P2A26	25P2A26	QTADD	89879100	2	2
26P2A28	24P1B28	Q15	89879100	1	1
26P2A29	23P2B08	32KW	89879100	1	1
26P2A29	27P2A06	32KW	89879100	2	2
26P2A30	25P2A30	AQC*	89879100	1	1
26P2B01	15P1B19	Q15	89879100	1	1
26P2B02	25P2A04	ALU7AM	89879100	1	1
26P2B03	21P2B03	GMM	89879100	2	2
26P2B04	20P2B28	OA11*	89879100	1	1
26P2B05	26P2A04	ALU7AL	89879100	2	2
26P2B07	25P2B07	M	89879100	1	1
26P2B08	22P2A28	AUG7M	89879100	2	2
26P2B09	25P2B09	S1	89879100	2	2
26P2B10	26P2B16	HIGH	89879100	2	2
26P2B10	26P2A12	HIGH	89879100	1	1
26P2B11	25P2B26	SHAL	89879100	1	1
26P2B12	20P1B03	CNS4M*	89879100	1	1
26P2B13	20P1A04	CNS6M*	89879100	1	1
26P2B14	20P1B05	CNS7M*	89879100	1	1
26P2B15	28P2B13	ALU7M	89879100	2	2
26P2B16	26P2B10	HIGH	89879100	2	2
26P2B16	25P2B06	HIGH	89879100	1	1
26P2B17	28P2A16	ALU4M	89879100	2	2
26P2B18	21P1B07	XSQM	89879100	2	2
26P2B19	27P1B20	MX7M	89879100	2	2
26P2B19	24P2A05	MX7M	89879100	1	1
26P2B20	24P2A08	MX5M	89879100	1	1
26P2B20	27P1A23	MX5M	89879100	2	2
26P2B22	17P2B18	OA15*	89879100	2	2
26P2B23	22P2A20	A7M	89879100	1	1
26P2B24	20P2A11	OA13*	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
26P2B25	15P1A19	Q14	89879100	1	1
26P2B26	25P2B05	SHAM	89879100	2	2
26P2B27	21P1B12	OVFW*	89879100	1	1
26P2B28	15P1B18	Q13	89879100	1	1
26P2B29	21P1A13	WEZM*	89879100	1	1
26P2B29	20P2A15	WEZM*	89879100	2	2
26P2B30	25P2B30	MC	89879100	2	2
26P2B31	25P2B31	C3	89879100	2	2
27P1A01	28P1B03	SD0	89879100	2	2
27P1A01	13P1A12	SD0	89879100	1	1
27P1A02	29P1A04	DOUT1	89879100	2	2
27P1A03	13P1A10	SD1	89879100	1	1
27P1A03	28P1A01	SD1	89879100	2	2
27P1A04	25P1B15	MX2L	89879100	2	2
27P1A04	31P1B04	MX2L	89879100	1	1
27P1A05	28P1B04	SD2	89879100	2	2
27P1A05	13P1B10	SD2	89879100	1	1
27P1A06	25P1A16	MX3L	89879100	2	2
27P1A06	31P1B06	MX3L	89879100	1	1
27P1A07	13P1B15	SD4	89879100	1	1
27P1A07	28P1B08	SD4	89879100	2	2
27P1A08	28P1B07	SD5	89879100	2	2
27P1A08	13P1B13	SD5	89879100	1	1
27P1A09	25P2B20	MX5L	89879100	2	2
27P1A09	31P1B09	MX5L	89879100	1	1
27P1A10	13P1A16	SD6	89879100	1	1
27P1A10	28P1B06	SD6	89879100	2	2
27P1A11	25P2A18	MX6L	89879100	2	2
27P1A11	31P1B12	MX6L	89879100	1	1
27P1A12	28P1B05	SD7	89879100	2	2
27P1A12	13P1A15	SD7	89879100	1	1
27P1A13	29P1A20	DOUT8	89879100	2	2
27P1A14	26P1B18	MXOM	89879100	2	2
27P1A14	31P1B13	MXOM	89879100	1	1
27P1A15	31P1B14	MX1M	89879100	1	1
27P1A15	26P1A19	MX1M	89879100	2	2
27P1A16	29P1B24	DOUT10	89879100	2	2
27P1A17	29P1A30	DOUT11	89879100	2	2
27P1A18	14P1A12	SD11	89879100	1	1
27P1A18	28P1A15	SD11	89879100	2	2
27P1A19	28P1A24	SD15	89879100	2	2
27P1A19	14P1A14	SD15	89879100	1	1
27P1A20	14P1B15	SD12	89879100	1	1
27P1A20	28P1A23	SD12	89879100	2	2
27P1A21	29P1A31	DOUT12	89879100	2	2
27P1A22	26P2A18	MX6M	89879100	2	2
27P1A22	31P1B21	MX6M	89879100	1	1
27P1A23	31P1A22	MX5M	89879100	1	1
27P1A23	26P2B20	MX5M	89879100	2	2
27P1A24	29P1B29	DOUT13	89879100	2	2
27P1A25	28P1B19	CAA15	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
27P1A26	31P2B03	MX17	89879100	1	1
27P1A26	21P2A19	MX17	89879100	2	2
27P1A27	21P2A12	MPRY	89879100	2	2
27P1A27	31P2B04	MPRY	89879100	1	1
27P1A28	31P2B05	CVIO1*	89879100	1	1
27P1A28	21P2B04	CVIO1*	89879100	2	2
27P1A30	24P1B12	WE*	89879100	2	2
27P1A30	31P2B06	WE*	89879100	1	1
27P1A31	31P2B09	CPEC*	89879100	1	1
27P1B01	29P1A07	DOUT0	89879100	2	2
27P1B02	25P1B18	MXOL	89879100	2	2
27P1B02	31P1B01	MXOL	89879100	1	1
27P1B03	31P1B02	MX1L	89879100	1	1
27P1B03	25P1A19	MX1L	89879100	2	2
27P1B04	29P1A06	DOUT2	89879100	2	2
27P1B05	29P1A08	DOUT3	89879100	2	2
27P1B06	28P1A05	SD3	89879100	2	2
27P1B06	13P1B17	SD3	89879100	1	1
27P1B07	29P1A09	DOUT4	89879100	2	2
27P1B08	25P2A20	MX4L	89879100	2	2
27P1B08	31P1B08	MX4L	89879100	1	1
27P1B09	29P1A14	DOUT5	89879100	2	2
27P1B10	29P1A17	DOUT6	89879100	2	2
27P1B12	29P1A19	DOUT7	89879100	2	2
27P1B13	25P2B19	MX7L	89879100	2	2
27P1B13	31P1A13	MX7L	89879100	1	1
27P1B14	14P1B17	SD8	89879100	1	1
27P1B14	28P1B14	SD8	89879100	2	2
27P1B15	29P1A25	DOUT9	89879100	2	2
27P1B16	28P1B18	SD9	89879100	2	2
27P1B16	14P1B10	SD9	89879100	1	1
27P1B17	26P1B15	MX2M	89879100	2	2
27P1B17	31P1B15	MX2M	89879100	1	1
27P1B18	14P1A10	SD10	89879100	1	1
27P1B18	28P1B20	SD10	89879100	2	2
27P1B19	26P1A16	MX3M	89879100	2	2
27P1B19	31P1A16	MX3M	89879100	1	1
27P1B20	31P1B17	MX7M	89879100	1	1
27P1B20	26P2B19	MX7M	89879100	2	2
27P1B21	26P2A20	MX4M	89879100	2	2
27P1B21	31P1B18	MX4M	89879100	1	1
27P1B22	28P1A19	SD14	89879100	2	2
27P1B22	14P1A15	SD14	89879100	1	1
27P1B23	14P1B26	SD13	89879100	1	1
27P1B23	28P1A20	SD13	89879100	2	2
27P1B24	29P1B30	DOUT14	89879100	2	2
27P1B25	29P1B31	DOUT15	89879100	2	2
27P1B26	28P1B22	CRI*	89879100	2	2
27P1B26	22P1A12	CRI*	89879100	1	1
27P1B27	28P2A13	D17	89879100	2	2
27P1B28	28P2A11	PAR	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
27P1B29	16P1A03	SPI*	89879100	2	2
27P1B29	31P2A10	SPI*	89879100	1	1
27P1B30	21P2B24	PRTM*	89879100	2	2
27P1B30	31P2A09	PRTM*	89879100	1	1
27P1B31	31P2B10	S WRITE*	89879100	1	1
27P1B31	16P1B05	S WRITE*	89879100	2	2
27P2A01	18P1A01	SA15	89879100	2	2
27P2A01	33P2A12	SA15	89879100	1	1
27P2A02	27P2B13	ICA*ICO*	89879100	2	2
27P2A04	27P2B15	ISAISO	89879100	1	1
27P2A05	33P2A11	EDX*	89879100	1	1
27P2A06	33P2A13	32KW	89879100	1	1
27P2A06	26P2A29	32KW	89879100	2	2
27P2A07	29P2A20	REF*	89879100	2	2
27P2A08	27P2B03	ICA-ICO	89879100	2	2
27P2A09	31P2A11	CRQ	89879104		
27P2A09	24P1B26	CRQ	89879104		
27P2A10	31P2B11	CCPE*	89879100	1	1
27P2A10	30P1B23	CCPE*	89879100	2	2
27P2A11	28P2B28	SXP*	89879100	2	2
27P2A12	29P2A07	STROBE*	89879100	2	2
27P2A14	33P2B14	MSXA*	89879100	1	1
27P2A15	22P2A21	P4M	89879100	2	2
27P2A16	29P2A01	DOUT16	89879100	2	2
27P2A17	28P2A14	P16	89879100	1	1
27P2A18	33P2B15	SD17	89879100	1	1
27P2A18	05P1A20	SD17	89879100	2	2
27P2A19	33P2B17	SS*	89879100	1	1
27P2A19	16P1B03	SS*	89879100	2	2
27P2A20	29P2B27	R/W	89879100	2	2
27P2A21	05P1A18	SD16	89879100	2	2
27P2A21	33P2A18	SD16	89879100	1	1
27P2A22	28P1A13	PBC	89879100	2	2
27P2A23	23P1A07	OSC*	89879104		
27P2A24	28P2A19	HOLDW	89879100	1	1
27P2A25	28P2B27	RXA	89879100	2	2
27P2A26	28P2A29	LOADRA*	89879100	1	1
27P2A28	33P2B20	SRQ*	89879100	1	1
27P2A28	16P1A01	SRQ*	89879100	2	2
27P2A30	23P1A01	VCC2	89879100	1	1
27P2B01	33P2B12	PRTSW	89879100	1	1
27P2B01	21P2A14	PRTSW	89879100	2	2
27P2B02	28P2A05	CMDR*	89879100	2	2
27P2B03	27P2A08	ICA-ICO	89879100	2	2
27P2B05	28P2B10	DOUT17	89879100	1	1
27P2B06	28P2A22	D16	89879100	1	1
27P2B08	28P2A20	SXA*	89879100	2	2
27P2B09	23P1A08	GCM1	89879104		
27P2B10	29P2A21	DISABLE	89879100	2	2
27P2B11	21P2A11	NORMAL	89879100	2	2
27P2B11	33P2B13	NORMAL	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
27P2B12	28P2B08	B	89879100	1	1
27P2B13	27P2A02	ICA*ICO*	89879100	2	2
27P2B14	28P2A25	HOLD	89879100	2	2
27P2B15	27P2A04	ISAISO	89879100	1	1
27P2B16	28P2B26	CXP*	89879100	1	1
27P2B17	28P2B18	DE*	89879100	1	1
27P2B18	16P1A10	SRSM*	89879100	2	2
27P2B18	33P2B16	SRSM*	89879100	1	1
27P2B19	21P2B08	DFEO	89879100	2	2
27P2B19	31P2B18	DFEO	89879100	1	1
27P2B20	31P2A19	MDEL	89879100	1	1
27P2B20	24P1B20	MDEL	89879100	2	2
27P2B21	23P1B11	GND	89879104		
27P2B22	28P2B29	BRWRA*	89879100	1	1
27P2B23	31P2B20	GPEC*	89879100	1	1
27P2B23	21P1B21	GPEC*	89879100	2	2
27P2B24	19P1A09	SVIO*	89879100	2	2
27P2B24	33P2B18	SVIO*	89879100	1	1
27P2B25	28P2B14	ADVANCE*	89879100	2	2
27P2B26	31P2A22	PEL*	89879100	1	1
27P2B26	20P2A07	PEL*	89879100	2	2
27P2B27	29P2A26	CE*	89879100	2	2
27P2B28	21P1B22	RGPWR	89879100	2	2
27P2B28	33P2A22	RGPWR	89879100	1	1
27P2B30	21P2B26	32M	89879100	1	1
27P2B31	28P2B31	MPWR*	89879100	1	1
28P1A01	27P1A03	SD1	89879100	2	2
28P1A01	33P1B01	SD1	89879100	1	1
28P1A02	29P1B03	DIN0	89879100	2	2
28P1A03	29P1B07	DIN3	89879100	2	2
28P1A04	29P1A05	DIN2	89879100	2	2
28P1A05	33P1B08	SD3	89879100	1	1
28P1A05	27P1B06	SD3	89879100	2	2
28P1A06	18P1A08	SA3	89879100	2	2
28P1A06	33P1A10	SA3	89879100	1	1
28P1A07	29P1B16	DIN5	89879100	2	2
28P1A08	29P1A07	DIN4	89879100	2	2
28P1A09	33P1B12	SA5	89879100	1	1
28P1A09	18P1B09	SA5	89879100	2	2
28P1A10	25P1A21	ALU3L	89879100	2	2
28P1A10	31P1A10	ALU3L	89879100	1	1
28P1A11	31P1A11	ALU1L	89879100	1	1
28P1A11	25P1B30	ALU1L	89879100	2	2
28P1A12	22P1A25	SPBM*	89879100	2	2
28P1A12	33P1B13	SPBM*	89879100	1	1
28P1A13	27P2A22	PBC	89879100	2	2
28P1A14	29P1B19	DIN8	89879100	2	2
28P1A15	27P1A18	SD11	89879100	2	2
28P1A15	33P1A16	SD11	89879100	1	1
28P1A16	29P1A15	DIN6	89879100	2	2
28P1A17	29P1A28	DIN10	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
28P1A18	29P1B20	DIN9	89879100	2	2
28P1A19	33P1B18	SD14	89879100	1	1
28P1A19	27P1B22	SD14	89879100	2	2
28P1A20	27P1B23	SD13	89879100	2	2
28P1A20	33P1B21	SD13	89879100	1	1
28P1A21	33P1B22	SA6	89879100	1	1
28P1A21	18P1B06	SA6	89879100	2	2
28P1A22	26P1B30	ALU1M	89879100	2	2
28P1A22	31P1B22	ALU1M	89879100	1	1
28P1A23	27P1A20	SD12	89879100	2	2
28P1A23	33P2B02	SD12	89879100	1	1
28P1A24	33P2B04	SD15	89879100	1	1
28P1A24	27P1A19	SD15	89879100	2	2
28P1A25	29P1B28	DIN14	89879100	2	2
28P1A26	18P1B02	SA10	89879100	2	2
28P1A26	33P2B05	SA10	89879100	1	1
28P1A27	26P1B27	ALU2M	89879100	2	2
28P1A27	31P1A23	ALU2M	89879100	1	1
28P1A28	31P1B23	ALU0M	89879100	1	1
28P1A28	26P1B24	ALUCM	89879100	2	2
28P1A30	33P2B09	SA14	89879100	1	1
28P1A30	18P1B04	SA14	89879100	2	2
28P1A31	18P1A04	SA13	89879100	2	2
28P1A31	33P2B10	SA13	89879100	1	1
28P1B01	33P1B02	SA2	89879100	1	1
28P1B01	18P1B08	SA2	89879100	2	2
28P1B02	29P1A03	DIN1	89879100	2	2
28P1B03	27P1A01	SD0	89879100	2	2
28P1B03	33P1B04	SD0	89879100	1	1
28P1B04	33P1B06	SD2	89879100	1	1
28P1B04	27P1A05	SD2	89879100	2	2
28P1B05	27P1A12	SD7	89879100	2	2
28P1B05	33P1B09	SD7	89879100	1	1
28P1B06	33P1B10	SD6	89879100	1	1
28P1B06	27P1A10	SD6	89879100	2	2
28P1B07	27P1A08	SD5	89879100	2	2
28P1B07	33P1A11	SD5	89879100	1	1
28P1B08	33P1A12	SD4	89879100	1	1
28P1B08	27P1A07	SD4	89879100	2	2
28P1B09	18P1A09	SA4	89879100	2	2
28P1B09	33P1A13	SA4	89879100	1	1
28P1B10	25P1B27	ALU2L	89879100	2	2
28P1B10	31P1B10	ALU2L	89879100	1	1
28P1B12	31P1A12	ALU0L	89879100	1	1
28P1B12	25P1B24	ALU0L	89879100	2	2
28P1B13	22P1B17	CPBM*	89879100	2	2
28P1B13	33P1B14	CPBM*	89879100	1	1
28P1B14	33P1B15	SD8	89879100	1	1
28P1B14	27P1B14	SD8	89879100	2	2
28P1B16	29P1A27	DIN11	89879100	2	2
28P1B17	29P1A18	DIN7	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
28P1B18	27P1B16	SD9	89879100	2	2
28P1B18	33P1B17	SD9	89879100	1	1
28P1B19	27P1A25	CAA15	89879100	1	1
28P1B20	33P1A22	SD10	89879100	1	1
28P1B20	27P1B18	SD10	89879100	2	2
28P1B21	18P1A03	SA11	89879100	2	2
28P1B21	33P1A23	SA11	89879100	1	1
28P1B22	27P1B26	CRI*	89879100	2	2
28P1B22	33P1B23	CRI*	89879100	1	1
28P1B23	33P2B03	SA7	89879100	1	1
28P1B23	18P1A06	SA7	89879100	2	2
28P1B24	29P1B25	DIN12	89879100	2	2
28P1B25	29P1B26	DIN15	89879100	2	2
28P1B26	29P1B27	DIN13	89879100	2	2
28P1B27	18P1B01	SA12	89879100	2	2
28P1B27	33P2B06	SA12	89879100	1	1
28P1B28	26P1A21	ALU3M	89879100	2	2
28P1B28	31P2B02	ALU3M	89879100	1	1
28P1B29	33P2A09	SA9	89879100	1	1
28P1B29	18P1B07	SA9	89879100	2	2
28P1B30	18P1A07	SA8	89879100	2	2
28P1B30	33P2A10	SA8	89879100	1	1
28P1B31	32P2B01	DX3*	89879100	1	1
28P2A01	30P2B01	DX1*	89879100	1	1
28P2A02	30P2A06	MDX1*	89879100	1	1
28P2A04	31P2A06	MDX2*	89879100	1	1
28P2A05	36P2B01	DX7*	89879100	1	1
28P2A06	27P2B02	CMDR*	89879100	2	2
28P2A07	35P2A06	MDX6*	89879100	1	1
28P2A08	36P2A06	MDX7*	89879100	1	1
28P2A09	31P2B12	ALU7L	89879100	1	1
28P2A09	25P2B15	ALU7L	89879100	2	2
28P2A10	29P2A05	DIN17	89879100	2	2
28P2A11	27P1B28	PAR	89879100	2	2
28P2A12	25P2A15	ALU6L	89879100	2	2
28P2A12	31P2B13	ALU6L	89879100	1	1
28P2A13	27P1B27	D17	89879100	2	2
28P2A14	27P2A17	P16	89879100	1	1
28P2A15	31P2B15	ALU5L	89879100	1	1
28P2A15	25P2A16	ALU5L	89879100	2	2
28P2A16	26P2B17	ALU4M	89879100	2	2
28P2A16	31P2B16	ALU4M	89879100	1	1
28P2A17	31P2A18	ALU4L	89879100	1	1
28P2A17	25P2B17	ALU4L	89879100	2	2
28P2A18	29P2B22	ACA8	89879100	2	2
28P2A19	27P2A24	HCLDW	89879100	1	1
28P2A20	27P2B08	SXA*	89879100	2	2
28P2A21	29P2B25	ARA3	89879100	2	2
28P2A22	27P2B06	D16	89879100	1	1
28P2A23	29P2A28	ARA2	89879100	2	2
28P2A24	33P2A19	SA0	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
28P2A24	18P1A02	SA0	89879100	2	2
28P2A25	27P2B14	HOLD	89879100	2	2
28P2A26	29P2B24	1K2*	89879100	2	2
28P2A27	29P2A24	1K3*	89879100	2	2
28P2A28	29P2A30	1K0*	89879100	2	2
28P2A29	27P2A26	LOADRA*	89879100	1	1
28P2B01	31P2B01	DX2*	89879100	1	1
28P2B02	32P2A06	MDX3*	89879100	1	1
28P2B03	29P2A06	MDX0*	89879100	1	1
28P2B04	33P2A06	MDX4*	89879100	1	1
28P2B05	35P2B01	DX6*	89879100	1	1
28P2B06	34P2B01	DX5*	89879100	1	1
28P2B07	34P2A06	MDX5*	89879100	1	1
28P2B08	27P2B12	B	89879100	1	1
28P2B09	31P2A13	ALU5M	89879100	1	1
28P2B09	26P2A16	ALU5M	89879100	2	2
28P2B10	29P2A02	DOUT17	89879100	2	2
28P2B10	27P2B05	DOUT17	89879100	1	1
28P2B11	33P2B01	DX4*	89879100	1	1
28P2B12	29P2A04	DIN16	89879100	2	2
28P2B13	26P2B15	ALU7M	89879100	2	2
28P2B13	31P2B14	ALU7M	89879100	1	1
28P2B14	27P2B25	ADVANCE*	89879100	2	2
28P2B15	29P2A25	ARA0	89879100	2	2
28P2B16	26P2A15	ALU6M	89879100	2	2
28P2B16	31P2B17	ALU6M	89879100	1	1
28P2B17	29P2B23	ACA6	89879100	2	2
28P2B18	27P2B17	DE*	89879100	1	1
28P2B19	29P2B26	ACA5	89879100	2	2
28P2B20	29P2A27	ACA9	89879100	2	2
28P2B22	29P2A29	ARA1	89879100	2	2
28P2B23	29P2B28	ARA4	89879100	2	2
28P2B24	29P2A23	ACA7	89879100	2	2
28P2B25	18P1B03	SA1	89879100	2	2
28P2B25	33P2B19	SA1	89879100	1	1
28P2B26	27P2B15	CXP*	89879100	1	1
28P2B27	27P2A25	RXA	89879100	2	2
28P2B28	27P2A11	SXP*	89879100	2	2
28P2B29	27P2B22	BRWRA*	89879100	1	1
28P2B30	29P2B29	1K1*	89879100	2	2
28P2B31	29P2B30	MPWR*	89879100	2	2
28P2B31	27P2B31	MPWR*	89879100	1	1
29P1A02	27P1B01	DOUT0	89879100	2	2
29P1A02	30P1A02	DOUT0	89879101	1	1
29P1A03	28P1B02	DIN1	89879100	2	2
29P1A03	30P1A03	DIN1	89879101	1	1
29P1A04	27P1A02	DOUT1	89879100	2	2
29P1A04	30P1A04	DOUT1	89879101	1	1
29P1A05	28P1A04	DIN2	89879100	2	2
29P1A05	30P1A05	DIN2	89879101	1	1
29P1A06	30P1A06	DOUT2	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
29P1A06	27P1B04	DOUT2	89879100	2	2
29P1A07	28P1A08	DIN4	89879100	2	2
29P1A07	30P1A07	DIN4	89879101	1	1
29P1A08	27P1B05	DOUT3	89879100	2	2
29P1A08	30P1A08	DOUT3	89879101	1	1
29P1A09	30P1A09	DOUT4	89879101	1	1
29P1A09	27P1B07	DOUT4	89879100	2	2
29P1A14	27P1B09	DOUT5	89879100	2	2
29P1A14	30P1A14	DOUT5	89879101	1	1
29P1A15	28P1A16	DIN6	89879100	2	2
29P1A15	30P1A15	DIN6	89879101	1	1
29P1A17	30P1A17	DOUT6	89879101	1	1
29P1A17	27P1B10	DOUT6	89879100	2	2
29P1A18	28P1B17	DIN7	89879100	2	2
29P1A18	30P1A18	DIN7	89879101	1	1
29P1A19	27P1B12	DOUT7	89879100	2	2
29P1A19	30P1A19	DOUT7	89879101	1	1
29P1A20	27P1A13	DOUT8	89879100	2	2
29P1A20	30P1A20	DOUT8	89879101	1	1
29P1A25	27P1B15	DOUT9	89879100	2	2
29P1A25	30P1A20	DOUT9	89879101	1	1
29P1A27	28P1B16	DIN11	89879100	2	2
29P1A27	30P1A27	DIN11	89879101	1	1
29P1A28	30P1A28	DIN10	89879101	1	1
29P1A28	28P1A17	DIN10	89879100	2	2
29P1A30	27P1A17	DOUT11	89879100	2	2
29P1A30	30P1A30	DOUT11	89879101	1	1
29P1A31	27P1A21	DOUT12	89879100	2	2
29P1A31	30P1A31	DOUT12	89879101	1	1
29P1B03	28P1A02	DIN0	89879100	2	2
29P1B03	30P1B03	DIN0	89879101	1	1
29P1B07	28P1A03	DIN3	89879100	2	2
29P1B07	30P1B07	DIN3	89879101	1	1
29P1B16	30P1B16	DIN5	89879101	1	1
29P1B16	28P1A07	DIN5	89879100	2	2
29P1B19	28P1A14	DIN8	89879100	2	2
29P1B19	30P1B19	DIN8	89879101	1	1
29P1B20	28P1A18	DIN9	89879100	2	2
29P1B20	30P1B20	DIN9	89879101	1	1
29P1B24	27P1A16	DOUT10	89879100	2	2
29P1B24	30P1B24	DOUT10	89879101	1	1
29P1B25	30P1B25	DIN12	89879101	1	1
29P1B25	28P1B24	DIN12	89879100	2	2
29P1B26	30P1B26	DIN15	89879101	1	1
29P1B26	28P1B25	DIN15	89879100	2	2
29P1B27	30P1B27	DIN13	89879101	1	1
29P1B27	28P1B26	DIN13	89879100	2	2
29P1B28	28P1A25	DIN14	89879100	2	2
29P1B28	30P1B28	DIN14	89879101	1	1
29P1B29	27P1A24	DOUT13	89879100	2	2
29P1B29	30P1B29	DOUT13	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
29P1B30	27P1B24	DOUT14	89879100	2	2
29P1B30	30P1B30	DOUT14	89879101	1	1
29P1B31	30P1B31	DOUT15	89879101	1	1
29P1B31	27P1B25	DOUT15	89879100	2	2
29P2A01	27P2A16	DOUT16	89879100	2	2
29P2A01	30P2A01	DOUT16	89879101	1	1
29P2A02	28P2B10	DOUT17	89879100	2	2
29P2A02	30P2A02	DOUT17	89879101	1	1
29P2A04	30P2A04	DIN16	89879101	1	1
29P2A04	28P2B12	DIN16	89879100	2	2
29P2A05	28P2A10	DIN17	89879100	2	2
29P2A05	30P2A05	DIN17	89879101	1	1
29P2A06	28P2B03	MDX0*	89879100	1	1
29P2A07	30P2A07	STROBE*	89879101	1	1
29P2A07	27P2A12	STROBE*	89879100	2	2
29P2A16	20P2B27	VSS	89879100	1	1
29P2A20	30P2A20	REF*	89879101	1	1
29P2A20	27P2A07	REF*	89879100	2	2
29P2A21	27P2B10	DISABLE	89879100	2	2
29P2A21	30P2A21	DISABLE	89879101	1	1
29P2A23	30P2A23	ACA7	89879101	1	1
29P2A23	28P2B24	ACA7	89879100	2	2
29P2A24	28P2A27	1K3*	89879100	2	2
29P2A24	30P2A24	1K3*	89879101	1	1
29P2A25	30P2A25	ARA0	89879101	1	1
29P2A25	28P2B15	ARA0	89879100	2	2
29P2A26	27P2B27	CE*	89879100	2	2
29P2A26	30P2A26	CE*	89879101	1	1
29P2A27	28P2B20	ACA9	89879100	2	2
29P2A27	30P2A27	ACA9	89879101	1	1
29P2A28	28P2A23	ARA2	89879100	2	2
29P2A28	30P2A28	ARA2	89879101	1	1
29P2A29	28P2B22	ARA1	89879100	2	2
29P2A29	30P2A29	ARA1	89879101	1	1
29P2A30	28P2A28	1K0*	89879100	2	2
29P2A30	30P2A30	1K0*	89879101	1	1
29P2B22	30P2B22	ACA8	89879101	1	1
29P2B22	28P2A18	ACA8	89879100	2	2
29P2B23	28P2B17	ACA6	89879100	2	2
29P2B23	30P2B23	ACA6	89879101	1	1
29P2B24	28P2A26	1K2*	89879100	2	2
29P2B24	30P2B24	1K2*	89879101	1	1
29P2B25	30P2B25	ARA3	89879101	1	1
29P2B25	28P2A21	ARA3	89879100	2	2
29P2B26	28P2B19	ACA5	89879100	2	2
29P2B26	30P2B26	ACA5	89879101	1	1
29P2B27	30P2B27	R/W	89879101	1	1
29P2B27	27P2A20	R/W	89879100	2	2
29P2B28	28P2B23	ARA4	89879100	2	2
29P2B28	30P2B28	ARA4	89879101	1	1
29P2B29	28P2B30	1K1*	89879100	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
29P2B29	30P2B29	1K1*	89879101	1	1
29P2B30	28P2B31	MPWR*	89879100	2	2
29P2B30	30P2B30	MPWR*	89879101	1	1
30P1A02	29P1A02	DOUT0	89879101	1	1
30P1A02	31P1A02	DOUT0	89879101	2	2
30P1A03	29P1A03	DIN1	89879101	1	1
30P1A03	31P1A03	DIN1	89879101	2	2
30P1A04	29P1A04	DOUT1	89879101	1	1
30P1A04	31P1A04	DOUT1	89879101	2	2
30P1A05	29P1A05	DIN2	89879101	1	1
30P1A05	31P1A05	DIN2	89879101	2	2
30P1A06	29P1A06	DOUT2	89879101	1	1
30P1A06	31P1A06	DOUT2	89879101	2	2
30P1A07	29P1A07	DIN4	89879101	1	1
30P1A07	31P1A07	DIN4	89879101	2	2
30P1A08	31P1A08	DOUT3	89879101	2	2
30P1A08	29P1A08	DOUT3	89879101	1	1
30P1A09	29P1A09	DOUT4	89879101	1	1
30P1A09	31P1A09	DOUT4	89879101	2	2
30P1A14	29P1A14	DOUT5	89879101	1	1
30P1A14	31P1A14	DOUT5	89879101	2	2
30P1A15	29P1A15	DIN6	89879101	1	1
30P1A15	31P1A15	DIN6	89879101	2	2
30P1A17	31P1A17	DOUT6	89879101	2	2
30P1A17	29P1A17	DOUT6	89879101	1	1
30P1A18	29P1A18	DIN7	89879101	1	1
30P1A18	31P1A18	DIN7	89879101	2	2
30P1A19	29P1A19	DOUT7	89879101	1	1
30P1A19	31P1A19	DOUT7	89879101	2	2
30P1A20	29P1A20	DOUT8	89879101	1	1
30P1A20	31P1A20	DOUT8	89879101	2	2
30P1A20	29P1A25	DOUT9	89879101	1	1
30P1A25	31P1A20	DOUT9	89879101	2	2
30P1A27	29P1A27	DIN11	89879101	1	1
30P1A27	31P1A27	DIN11	89879101	2	2
30P1A28	29P1A28	DIN10	89879101	1	1
30P1A28	31P1A28	DIN10	89879101	2	2
30P1A30	29P1A30	DOUT11	89879101	1	1
30P1A30	31P1A30	DOUT11	89879101	2	2
30P1A31	29P1A31	DOUT12	89879101	1	1
30P1A31	31P1A31	DOUT12	89879101	2	2
30P1B03	31P1B03	DIN0	89879101	2	2
30P1B03	29P1B03	DIN0	89879101	1	1
30P1B07	29P1B07	DIN3	89879101	1	1
30P1B07	31P1B07	DIN3	89879101	2	2
30P1B16	31P1B16	DIN5	89879101	2	2
30P1B16	29P1B16	DIN5	89879101	1	1
30P1B19	31P1B19	DIN8	89879101	2	2
30P1B19	29P1B19	DIN8	89879101	1	1
30P1B20	31P1B20	DIN9	89879101	2	2
30P1B20	29P1B20	DIN9	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
30P1B23	27P2A10	CCPE*	89879100	2	2
30P1B23	20P1A28	CCPE*	89879100	1	1
30P1B24	31P1B24	DOUT10	89879101	2	2
30P1B24	29P1B24	DOUT10	89879101	1	1
30P1B25	31P1B25	DIN12	89879101	2	2
30P1B25	29P1B25	DIN12	89879101	1	1
30P1B26	29P1B26	DIN15	89879101	1	1
30P1B26	31P1B26	DIN15	89879101	2	2
30P1B27	31P1B27	DIN13	89879101	2	2
30P1B27	29P1B27	DIN13	89879101	1	1
30P1B28	31P1B28	DIN14	89879101	2	2
30P1B28	29P1B28	DIN14	89879101	1	1
30P1B29	29P1B29	DOUT13	89879101	1	1
30P1B29	31P1B29	DOUT13	89879101	2	2
30P1B30	31P1B30	DOUT14	89879101	2	2
30P1B30	29P1B30	DOUT14	89879101	1	1
30P1B31	29P1B31	DOUT15	89879101	1	1
30P1B31	31P1B31	DOUT15	89879101	2	2
30P2A01	29P2A01	DOUT16	89879101	1	1
30P2A01	31P2A01	DOUT16	89879101	2	2
30P2A02	31P2A02	DOUT17	89879101	2	2
30P2A02	29P2A02	DOUT17	89879101	1	1
30P2A04	29P2A04	DIN16	89879101	1	1
30P2A04	31P2A04	DIN16	89879101	2	2
30P2A05	31P2A05	DIN17	89879101	2	2
30P2A05	29P2A05	DIN17	89879101	1	1
30P2A06	28P2A02	MDX1*	89879100	1	1
30P2A07	29P2A07	STROBE*	89879101	1	1
30P2A07	31P2A07	STROBE*	89879101	2	2
30P2A20	29P2A20	REF*	89879101	1	1
30P2A20	31P2A20	REF*	89879101	2	2
30P2A21	29P2A21	DISABLE	89879101	1	1
30P2A21	31P2A21	DISABLE	89879101	2	2
30P2A23	29P2A23	ACA7	89879101	1	1
30P2A23	31P2A23	ACA7	89879101	2	2
30P2A24	29P2A24	1K3*	89879101	1	1
30P2A24	31P2A24	1K3*	89879101	2	2
30P2A25	29P2A25	ARA0	89879101	1	1
30P2A25	31P2A25	ARA0	89879101	2	2
30P2A26	31P2A26	CE*	89879101	2	2
30P2A26	29P2A26	CE*	89879101	1	1
30P2A27	29P2A27	ACA9	89879101	1	1
30P2A27	31P2A27	ACA9	89879101	2	2
30P2A28	29P2A28	ARA2	89879101	1	1
30P2A28	31P2A28	ARA2	89879101	2	2
30P2A29	29P2A29	ARA1	89879101	1	1
30P2A29	31P2A29	ARA1	89879101	2	2
30P2A30	31P2A30	1K0*	89879101	2	2
30P2A30	29P2A30	1K0*	89879101	1	1
30P2B01	28P2A01	DX1*	89879100	1	1
30P2B22	29P2B22	ACA8	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
30P2B22	31P2B22	ACA8	89879101	2	2
30P2B23	29P2B23	ACA6	89879101	1	1
30P2B23	31P2B23	ACA6	89879101	2	2
30P2B24	29P2B24	1K2*	89879101	1	1
30P2B24	31P2B24	1K2*	89879101	2	2
30P2B25	29P2B25	ARA3	89879101	1	1
30P2B25	31P2B25	ARA3	89879101	2	2
30P2B26	29P2B26	ACA5	89879101	1	1
30P2B26	31P2B26	ACA5	89879101	2	2
30P2B27	31P2B27	R/W	89879101	2	2
30P2B27	29P2B27	R/W	89879101	1	1
30P2B28	31P2B28	ARA4	89879101	2	2
30P2B28	29P2B28	ARA4	89879101	1	1
30P2B29	29P2B29	1K1*	89879101	1	1
30P2B29	31P2B29	1K1*	89879101	2	2
30P2B30	31P2B30	MPWR*	89879101	2	2
30P2B30	29P2B30	MPWR*	89879101	1	1
31P1A02	32P1A02	DOUT0	89879101	1	1
31P1A02	30P1A02	DOUT0	89879101	2	2
31P1A03	32P1A03	DIN1	89879101	1	1
31P1A03	30P1A03	DIN1	89879101	2	2
31P1A04	30P1A04	DOUT1	89879101	2	2
31P1A04	32P1A04	DOUT1	89879101	1	1
31P1A05	32P1A05	DIN2	89879101	1	1
31P1A05	30P1A05	DIN2	89879101	2	2
31P1A06	32P1A06	DOUT2	89879101	1	1
31P1A06	30P1A06	DOUT2	89879101	2	2
31P1A07	30P1A07	DIN4	89879101	2	2
31P1A07	32P1A07	DIN4	89879101	1	1
31P1A08	32P1A08	DOUT3	89879101	1	1
31P1A08	30P1A08	DOUT3	89879101	2	2
31P1A09	30P1A09	DOUT4	89879101	2	2
31P1A09	32P1A09	DOUT4	89879101	1	1
31P1A10	28P1A10	ALU3L	89879100	1	1
31P1A11	28P1A11	ALU1L	89879100	1	1
31P1A12	28P1B12	ALU0L	89879100	1	1
31P1A13	27P1B13	MX7L	89879100	1	1
31P1A14	30P1A14	DOUT5	89879101	2	2
31P1A14	32P1A14	DOUT5	89879101	1	1
31P1A15	32P1A15	DIN6	89879101	1	1
31P1A15	30P1A15	DIN6	89879101	2	2
31P1A16	27P1B19	MX3M	89879100	1	1
31P1A17	32P1A17	DOUT6	89879101	1	1
31P1A17	30P1A17	DOUT6	89879101	2	2
31P1A18	30P1A18	DIN7	89879101	2	2
31P1A18	32P1A18	DIN7	89879101	1	1
31P1A19	32P1A19	DOUT7	89879101	1	1
31P1A19	30P1A19	DOUT7	89879101	2	2
31P1A20	30P1A25	DOUT9	89879101	2	2
31P1A20	32P1A20	DOUT8	89879101	1	1
31P1A20	30P1A20	DOUT8	89879101	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
31P1A22	27P1A23	MX5M	89879100	1	1
31P1A23	28P1A27	ALU2M	89879100	1	1
31P1A25	32P1A20	DOUT9	89879101	1	1
31P1A27	30P1A27	DIN11	89879101	2	2
31P1A27	32P1A27	DIN11	89879101	1	1
31P1A28	32P1A28	DIN10	89879101	1	1
31P1A28	30P1A28	DIN10	89879101	2	2
31P1A30	32P1A30	DOUT11	89879101	1	1
31P1A30	30P1A30	DOUT11	89879101	2	2
31P1A31	30P1A31	DOUT12	89879101	2	2
31P1A31	32P1A31	DOUT12	89879101	1	1
31P1B01	27P1B02	MX0L	89879100	1	1
31P1B02	27P1B03	MX1L	89879100	1	1
31P1B03	30P1B03	DIN0	89879101	2	2
31P1B03	32P1B03	DIN0	89879101	1	1
31P1B04	27P1A04	MX2L	89879100	1	1
31P1B06	27P1A06	MX3L	89879100	1	1
31P1B07	30P1B07	DIN3	89879101	2	2
31P1B07	32P1B07	DIN3	89879101	1	1
31P1B08	27P1B08	MX4L	89879100	1	1
31P1B09	27P1A09	MX5L	89879100	1	1
31P1B10	28P1B10	ALU2L	89879100	1	1
31P1B12	27P1A11	MX6L	89879100	1	1
31P1B13	27P1A14	MX0M	89879100	1	1
31P1B14	27P1A15	MX1M	89879100	1	1
31P1B15	27P1B17	MX2M	89879100	1	1
31P1B16	30P1B16	DIN5	89879101	2	2
31P1B16	32P1B16	DIN5	89879101	1	1
31P1B17	27P1B20	MX7M	89879100	1	1
31P1B18	27P1B21	MX4M	89879100	1	1
31P1B19	32P1B19	DIN8	89879101	1	1
31P1B19	30P1B19	DIN8	89879101	2	2
31P1B20	30P1B20	DIN9	89879101	2	2
31P1B20	32P1B20	DIN9	89879101	1	1
31P1B21	27P1A22	MX6M	89879100	1	1
31P1B22	28P1A22	ALU1M	89879100	1	1
31P1B23	28P1A28	ALU0M	89879100	1	1
31P1B24	32P1B24	DOUT10	89879101	1	1
31P1B24	30P1B24	DOUT10	89879101	2	2
31P1B25	30P1B25	DIN12	89879101	2	2
31P1B25	32P1B25	DIN12	89879101	1	1
31P1B26	32P1B26	DIN15	89879101	1	1
31P1B26	30P1B26	DIN15	89879101	2	2
31P1B27	30P1B27	DIN13	89879101	2	2
31P1B27	32P1B27	DIN13	89879101	1	1
31P1B28	30P1B28	DIN14	89879101	2	2
31P1B28	32P1B28	DIN14	89879101	1	1
31P1B29	32P1B29	DOUT13	89879101	1	1
31P1B29	30P1B29	DOUT13	89879101	2	2
31P1B30	30P1B30	DOUT14	89879101	2	2
31P1B30	32P1B30	DOUT14	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
31P1B31	32P1B31	DOUT15	89879101	1	1
31P1B31	30P1B31	DOUT15	89879101	2	2
31P2A01	30P2A01	DOUT16	89879101	2	2
31P2A01	32P2A01	DOUT16	89879101	1	1
31P2A02	32P2A02	DOUT17	89879101	1	1
31P2A02	30P2A02	DOUT17	89879101	2	2
31P2A04	30P2A04	DIN16	89879101	2	2
31P2A04	32P2A04	DIN16	89879101	1	1
31P2A05	32P2A05	DIN17	89879101	1	1
31P2A05	30P2A05	DIN17	89879101	2	2
31P2A06	28P2A04	MDX2*	89879100	1	1
31P2A07	30P2A07	STROBE*	89879101	2	2
31P2A07	32P2A07	STROBE*	89879101	1	1
31P2A09	27P1B30	PRTM*	89879100	1	1
31P2A10	27P1B29	SPI*	89879100	1	1
31P2A11	27P2A09	CRQ	89879104		
31P2A13	28P2B09	ALU5M	89879100	1	1
31P2A18	28P2A17	ALU4L	89879100	1	1
31P2A19	27P2B20	MDEL	89879100	1	1
31P2A20	32P2A20	REF*	89879101	1	1
31P2A20	30P2A20	REF*	89879101	2	2
31P2A21	30P2A21	DISABLE	89879101	2	2
31P2A21	32P2A21	DISABLE	89879101	1	1
31P2A22	27P2B26	PEL*	89879100	1	1
31P2A23	32P2A23	ACA7	89879101	1	1
31P2A23	30P2A23	ACA7	89879101	2	2
31P2A24	32P2A24	1K3*	89879101	1	1
31P2A24	30P2A24	1K3*	89879101	2	2
31P2A25	32P2A25	ARA0	89879101	1	1
31P2A25	30P2A25	ARA0	89879101	2	2
31P2A26	30P2A26	CE*	89879101	2	2
31P2A26	32P2A26	CE*	89879101	1	1
31P2A27	30P2A27	ACA9	89879101	2	2
31P2A27	32P2A27	ACA9	89879101	1	1
31P2A28	32P2A28	ARA2	89879101	1	1
31P2A28	30P2A28	ARA2	89879101	2	2
31P2A29	30P2A29	ARA1	89879101	2	2
31P2A29	32P2A29	ARA1	89879101	1	1
31P2A30	30P2A30	1K0*	89879101	2	2
31P2A30	32P2A30	1K0*	89879101	1	1
31P2B01	28P2B01	DX2*	89879100	1	1
31P2B02	28P1B28	ALU3M	89879100	1	1
31P2B03	27P1A26	MX17	89879100	1	1
31P2B04	27P1A27	MPRY	89879100	1	1
31P2B05	27P1A28	CVI01*	89879100	1	1
31P2B06	27P1A30	WE*	89879100	1	1
31P2B09	27P1A31	CPEC*	89879100	1	1
31P2B10	27P1B31	S WRITE*	89879100	1	1
31P2B11	27P2A10	CCPE*	89879100	1	1
31P2B12	28P2A09	ALU7L	89879100	1	1
31P2B13	28P2A12	ALU6L	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
31P2B14	28P2B13	ALU7M	89879100	1	1
31P2B15	28P2A15	ALU5L	89879100	1	1
31P2B16	28P2A16	ALU4M	89879100	1	1
31P2B17	28P2B16	ALU6M	89879100	1	1
31P2B18	27P2B19	DFE0	89879100	1	1
31P2B20	27P2B23	GPEC*	89879100	1	1
31P2B22	30P2B22	ACA8	89879101	2	2
31P2B22	32P2B22	ACA8	89879101	1	1
31P2B23	30P2B23	ACA6	89879101	2	2
31P2B23	32P2B23	ACA6	89879101	1	1
31P2B24	32P2B24	1K2*	89879101	1	1
31P2B24	30P2B24	1K2*	89879101	2	2
31P2B25	30P2B25	ARA3	89879101	2	2
31P2B25	32P2B25	ARA3	89879101	1	1
31P2B26	32P2B26	ACA5	89879101	1	1
31P2B26	30P2B26	ACA5	89879101	2	2
31P2B27	32P2B27	R/W	89879101	1	1
31P2B27	30P2B27	R/W	89879101	2	2
31P2B28	32P2B28	ARA4	89879101	1	1
31P2B28	30P2B28	ARA4	89879101	2	2
31P2B29	30P2B29	1K1*	89879101	2	2
31P2B29	32P2B29	1K1*	89879101	1	1
31P2B30	30P2B30	MPWR*	89879101	2	2
32P1A02	31P1A02	DOUT0	89879101	1	1
32P1A02	33P1A02	DOUT0	89879101	2	2
32P1A03	31P1A03	DIN1	89879101	1	1
32P1A03	33P1A03	DIN1	89879101	2	2
32P1A04	31P1A04	DOUT1	89879101	1	1
32P1A04	33P1A04	DOUT1	89879101	2	2
32P1A05	31P1A05	DIN2	89879101	1	1
32P1A05	33P1A05	DIN2	89879101	2	2
32P1A06	33P1A06	DOUT2	89879101	2	2
32P1A06	31P1A06	DOUT2	89879101	1	1
32P1A07	31P1A07	DIN4	89879101	1	1
32P1A07	33P1A07	DIN4	89879101	2	2
32P1A08	33P1A08	DOUT3	89879101	2	2
32P1A08	31P1A08	DOUT3	89879101	1	1
32P1A09	31P1A09	DOUT4	89879101	1	1
32P1A09	33P1A09	DOUT4	89879101	2	2
32P1A14	33P1A14	DOUT5	89879101	2	2
32P1A14	31P1A14	DOUT5	89879101	1	1
32P1A15	33P1A15	DIN6	89879101	2	2
32P1A15	31P1A15	DIN6	89879101	1	1
32P1A17	31P1A17	DOUT6	89879101	1	1
32P1A17	33P1A17	DOUT6	89879101	2	2
32P1A18	31P1A18	DIN7	89879101	1	1
32P1A18	33P1A18	DIN7	89879101	2	2
32P1A19	31P1A19	DOUT7	89879101	1	1
32P1A19	33P1A19	DOUT7	89879101	2	2
32P1A20	31P1A25	DOUT9	89879101	1	1
32P1A20	33P1A20	DOUT8	89879101	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
32P1A20	31P1A20	DOUT8	89879101	1	1
32P1A25	33P1A20	DOUT9	89879101	2	2
32P1A27	33P1A27	DIN11	89879101	2	2
32P1A27	31P1A27	DIN11	89879101	1	1
32P1A28	31P1A28	DIN10	89879101	1	1
32P1A28	33P1A28	DIN10	89879101	2	2
32P1A30	33P1A30	DOUT11	89879101	2	2
32P1A30	31P1A30	DOUT11	89879101	1	1
32P1A31	33P1A31	DOUT12	89879101	2	2
32P1A31	31P1A31	DOUT12	89879101	1	1
32P1B03	31P1B03	DIN0	89879101	1	1
32P1B03	33P1B03	DIN0	89879101	2	2
32P1B07	33P1B07	DIN3	89879101	2	2
32P1B07	31P1B07	DIN3	89879101	1	1
32P1B16	31P1B16	DIN5	89879101	1	1
32P1B16	33P1B16	DIN5	89879101	2	2
32P1B19	33P1B19	DIN8	89879101	2	2
32P1B19	31P1B19	DIN8	89879101	1	1
32P1B20	33P1B20	DIN9	89879101	2	2
32P1B20	31P1B20	DIN9	89879101	1	1
32P1B24	33P1B24	DOUT10	89879101	2	2
32P1B24	31P1B24	DOUT10	89879101	1	1
32P1B25	31P1B25	DIN12	89879101	1	1
32P1B25	33P1B25	DIN12	89879101	2	2
32P1B26	33P1B26	DIN15	89879101	2	2
32P1B26	31P1B26	DIN15	89879101	1	1
32P1B27	33P1B27	DIN13	89879101	2	2
32P1B27	31P1B27	DIN13	89879101	1	1
32P1B28	31P1B28	DIN14	89879101	1	1
32P1B28	33P1B28	DIN14	89879101	2	2
32P1B29	33P1B29	DOUT13	89879101	2	2
32P1B29	31P1B29	DOUT13	89879101	1	1
32P1B30	31P1B30	DOUT14	89879101	1	1
32P1B30	33P1B30	DOUT14	89879101	2	2
32P1B31	33P1B31	DOUT15	89879101	2	2
32P1B31	31P1B31	DOUT15	89879101	1	1
32P2A01	31P2A01	DOUT16	89879101	1	1
32P2A01	33P2A01	DOUT16	89879101	2	2
32P2A02	31P2A02	DOUT17	89879101	1	1
32P2A02	33P2A02	DOUT17	89879101	2	2
32P2A04	33P2A04	DIN16	89879101	2	2
32P2A04	31P2A04	DIN16	89879101	1	1
32P2A05	31P2A05	DIN17	89879101	1	1
32P2A05	33P2A05	DIN17	89879101	2	2
32P2A06	28P2B02	MDX3*	89879100	1	1
32P2A07	33P2A07	STROBE*	89879101	2	2
32P2A07	31P2A07	STROBE*	89879101	1	1
32P2A20	31P2A20	REF*	89879101	1	1
32P2A20	33P2A20	REF*	89879101	2	2
32P2A21	33P2A21	DISABLE	89879101	2	2
32P2A21	31P2A21	DISABLE	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
32P2A23	33P2A23	ACA7	89879101	2	2
32P2A23	31P2A23	ACA7	89879101	1	1
32P2A24	31P2A24	1K3*	89879101	1	1
32P2A24	33P2A24	1K3*	89879101	2	2
32P2A25	31P2A25	ARA0	89879101	1	1
32P2A25	33P2A25	ARA0	89879101	2	2
32P2A26	31P2A26	CE*	89879101	1	1
32P2A26	33P2A26	CE*	89879101	2	2
32P2A27	31P2A27	ACA9	89879101	1	1
32P2A27	33P2A27	ACA9	89879101	2	2
32P2A28	33P2A28	ARA2	89879101	2	2
32P2A28	31P2A28	ARA2	89879101	1	1
32P2A29	33P2A29	ARA1	89879101	2	2
32P2A29	31P2A29	ARA1	89879101	1	1
32P2A30	33P2A30	1K0*	89879101	2	2
32P2A30	31P2A30	1K0*	89879101	1	1
32P2B01	28P1B31	DX3*	89879100	1	1
32P2B22	31P2B22	ACA8	89879101	1	1
32P2B22	33P2B22	ACA8	89879101	2	2
32P2B23	33P2B23	ACA6	89879101	2	2
32P2B23	31P2B23	ACA6	89879101	1	1
32P2B24	33P2B24	1K2*	89879101	2	2
32P2B24	31P2B24	1K2*	89879101	1	1
32P2B25	31P2B25	ARA3	89879101	1	1
32P2B25	33P2B25	ARA3	89879101	2	2
32P2B26	31P2B26	ACA5	89879101	1	1
32P2B26	33P2B26	ACA5	89879101	2	2
32P2B27	33P2B27	R/W	89879101	2	2
32P2B27	31P2B27	R/W	89879101	1	1
32P2B28	31P2B28	ARA4	89879101	1	1
32P2B28	33P2B28	ARA4	89879101	2	2
32P2B29	31P2B29	1K1*	89879101	1	1
32P2B29	33P2B29	1K1*	89879101	2	2
32P2B30	33P2B30	MPWR*	89879101	2	2
33P1A02	32P1A02	DOUT0	89879101	2	2
33P1A02	34P1A02	DOUT0	89879101	1	1
33P1A03	32P1A03	DIN1	89879101	2	2
33P1A03	34P1A03	DIN1	89879101	1	1
33P1A04	34P1A04	DOUT1	89879101	1	1
33P1A04	32P1A04	DOUT1	89879101	2	2
33P1A05	34P1A05	DIN2	89879101	1	1
33P1A05	32P1A05	DIN2	89879101	2	2
33P1A06	32P1A06	DOUT2	89879101	2	2
33P1A06	34P1A06	DOUT2	89879101	1	1
33P1A07	34P1A07	DIN4	89879101	1	1
33P1A07	32P1A07	DIN4	89879101	2	2
33P1A08	34P1A08	DOUT3	89879101	1	1
33P1A08	32P1A08	DOUT3	89879101	2	2
33P1A09	34P1A09	DOUT4	89879101	1	1
33P1A09	32P1A09	DOUT4	89879101	2	2
33P1A10	28P1A06	SA3	89879100	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
33P1A11	28P1B07	SD5	89879100	1	1
33P1A12	28P1B08	SD4	89879100	1	1
33P1A13	28P1B09	SA4	89879100	1	1
33P1A14	32P1A14	DOUT5	89879101	2	2
33P1A14	34P1A14	DOUT5	89879101	1	1
33P1A15	34P1A15	DIN6	89879101	1	1
33P1A15	32P1A15	DIN6	89879101	2	2
33P1A16	28P1A15	SD11	89879100	1	1
33P1A17	34P1A17	DOUT6	89879101	1	1
33P1A17	32P1A17	DOUT6	89879101	2	2
33P1A18	32P1A18	DIN7	89879101	2	2
33P1A18	34P1A18	DIN7	89879101	1	1
33P1A19	32P1A19	DOUT7	89879101	2	2
33P1A19	34P1A19	DOUT7	89879101	1	1
33P1A20	32P1A25	DOUT9	89879101	2	2
33P1A20	32P1A20	DOUT8	89879101	2	2
33P1A20	34P1A20	DOUT8	89879101	1	1
33P1A22	28P1B20	SD10	89879100	1	1
33P1A23	28P1B21	SA11	89879100	1	1
33P1A25	34P1A20	DOUT9	89879101	1	1
33P1A27	34P1A27	DIN11	89879101	1	1
33P1A27	32P1A27	DIN11	89879101	2	2
33P1A28	34P1A28	DIN10	89879101	1	1
33P1A28	32P1A28	DIN10	89879101	2	2
33P1A30	34P1A30	DOUT11	89879101	1	1
33P1A30	32P1A30	DOUT11	89879101	2	2
33P1A31	34P1A31	DOUT12	89879101	1	1
33P1A31	32P1A31	DOUT12	89879101	2	2
33P1B01	28P1A01	SD1	89879100	1	1
33P1B02	28P1B01	SA2	89879100	1	1
33P1B03	32P1B03	DIN0	89879101	2	2
33P1B03	34P1B03	DIN0	89879101	1	1
33P1B04	28P1B03	SD0	89879100	1	1
33P1B06	28P1B04	SD2	89879100	1	1
33P1B07	34P1B07	DIN3	89879101	1	1
33P1B07	32P1B07	DIN3	89879101	2	2
33P1B08	28P1A05	SD3	89879100	1	1
33P1B09	28P1B05	SD7	89879100	1	1
33P1B10	28P1B06	SD6	89879100	1	1
33P1B12	28P1A09	SA5	89879100	1	1
33P1B13	28P1A12	SPBM*	89879100	1	1
33P1B14	28P1B13	CPBM*	89879100	1	1
33P1B15	28P1B14	SD8	89879100	1	1
33P1B16	34P1B16	DIN5	89879101	1	1
33P1B16	32P1B16	DIN5	89879101	2	2
33P1B17	28P1B18	SD9	89879100	1	1
33P1B18	28P1A19	SD14	89879100	1	1
33P1B19	34P1B19	DIN8	89879101	1	1
33P1B19	32P1B19	DIN8	89879101	2	2
33P1B20	32P1B20	DIN9	89879101	2	2
33P1B20	34P1B20	DIN9	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
33P1B21	28P1A20	SD13	89879100	1	1
33P1B22	28P1A21	SA6	89879100	1	1
33P1B23	28P1B27	CRI*	89879100	1	1
33P1B24	32P1B24	DOUT10	89879101	2	2
33P1B24	34P1B24	DOUT10	89879101	1	1
33P1B25	34P1B25	DIN12	89879101	1	1
33P1B25	32P1B25	DIN12	89879101	2	2
33P1B26	34P1B26	DIN15	89879101	1	1
33P1B26	32P1B26	DIN15	89879101	2	2
33P1B27	32P1B27	DIN13	89879101	2	2
33P1B27	34P1B27	DIN13	89879101	1	1
33P1B28	34P1B28	DIN14	89879101	1	1
33P1B28	32P1B28	DIN14	89879101	2	2
33P1B29	32P1B29	DOUT13	89879101	2	2
33P1B29	34P1B29	DOUT13	89879101	1	1
33P1B30	34P1B30	DOUT14	89879101	1	1
33P1B30	32P1B30	DOUT14	89879101	2	2
33P1B31	32P1B31	DOUT15	89879101	2	2
33P1B31	34P1B31	DOUT15	89879101	1	1
33P2A01	34P2A01	DOUT16	89879101	1	1
33P2A01	32P2A01	DOUT16	89879101	2	2
33P2A02	32P2A02	DOUT17	89879101	2	2
33P2A02	34P2A02	DOUT17	89879101	1	1
33P2A04	34P2A04	DIN16	89879101	1	1
33P2A04	32P2A04	DIN16	89879101	2	2
33P2A05	34P2A05	DIN17	89879101	1	1
33P2A05	32P2A05	DIN17	89879101	2	2
33P2A06	28P2B04	MDX4*	89879100	1	1
33P2A07	32P2A07	STROBE*	89879101	2	2
33P2A07	34P2A07	STROBE*	89879101	1	1
33P2A09	28P1B29	SA9	89879100	1	1
33P2A10	28P1B30	SA8	89879100	1	1
33P2A11	27P2A05	EDX*	89879100	1	1
33P2A12	27P2A01	SA15	89879100	1	1
33P2A13	27P2A06	32KW	89879100	1	1
33P2A18	27P2A21	SD16	89879100	1	1
33P2A19	28P2A24	SA0	89879100	1	1
33P2A20	34P2A20	REF*	89879101	1	1
33P2A20	32P2A20	REF*	89879101	2	2
33P2A21	34P2A21	DISABLE	89879101	1	1
33P2A21	32P2A21	DISABLE	89879101	2	2
33P2A22	27P2B28	RGPWR	89879100	1	1
33P2A23	34P2A23	ACA7	89879101	1	1
33P2A23	32P2A23	ACA7	89879101	2	2
33P2A24	34P2A24	1K3*	89879101	1	1
33P2A24	32P2A24	1K3*	89879101	2	2
33P2A25	34P2A25	ARA0	89879101	1	1
33P2A25	32P2A25	ARA0	89879101	2	2
33P2A26	32P2A26	CE*	89879101	2	2
33P2A26	34P2A26	CE*	89879101	1	1
33P2A27	34P2A27	ACA9	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
33P2A27	32P2A27	ACA9	89879101	2	2
33P2A28	34P2A28	ARA2	89879101	1	1
33P2A28	32P2A28	ARA2	89879101	2	2
33P2A29	34P2A29	ARA1	89879101	1	1
33P2A29	32P2A29	ARA1	89879101	2	2
33P2A30	34P2A30	1KO*	89879101	1	1
33P2A30	32P2A30	1KO*	89879101	2	2
33P2B01	28P2B11	DX4*	89879100	1	1
33P2B02	28P1A23	SD12	89879100	1	1
33P2B03	28P1B23	SA7	89879100	1	1
33P2B04	28P1A24	SD15	89879100	1	1
33P2B05	28P1A26	SA10	89879100	1	1
33P2B06	28P1B27	SA12	89879100	1	1
33P2B09	28P1A30	SA14	89879100	1	1
33P2B10	28P1A31	SA13	89879100	1	1
33P2B11	23P1A05	GOM2	89879104		
33P2B12	27P2B01	PRTSW	89879100	1	1
33P2B13	27P2B11	NORMAL	89879100	1	1
33P2B14	27P2A14	MSXA*	89879100	1	1
33P2B15	27P2A18	SD17	89879100	1	1
33P2B16	27P2B18	SRSM*	89879100	1	1
33P2B17	27P2A19	SS*	89879100	1	1
33P2B18	27P2B24	SVIO*	89879100	1	1
33P2B19	28P2B25	SA1	89879100	1	1
33P2B20	27P2A28	SRQ*	89879100	1	1
33P2B22	32P2B22	ACA8	89879101	2	2
33P2B22	34P2B22	ACA8	89879101	1	1
33P2B23	32P2B23	ACA6	89879101	2	2
33P2B23	34P2B23	ACA6	89879101	1	1
33P2B24	34P2B24	1K2*	89879101	1	1
33P2B24	32P2B24	1K2*	89879101	2	2
33P2B25	32P2B25	ARA3	89879101	2	2
33P2B25	34P2B25	ARA3	89879101	1	1
33P2B26	34P2B26	ACA5	89879101	1	1
33P2B26	32P2B26	ACA5	89879101	2	2
33P2B27	34P2B27	R/W	89879101	1	1
33P2B27	32P2B27	R/W	89879101	2	2
33P2B28	34P2B28	ARA4	89879101	1	1
33P2B28	32P2B28	ARA4	89879101	2	2
33P2B29	34P2B29	1K1*	89879101	1	1
33P2B29	32P2B29	1K1*	89879101	2	2
33P2B30	32P2B30	MPWR*	89879101	2	2
33P2B30	34P2B30	MPWR*	89879101	1	1
34P1A02	33P1A02	DOUT0	89879101	1	1
34P1A02	35P1A02	DOUT0	89879101	2	2
34P1A03	35P1A03	DIN1	89879101	2	2
34P1A03	33P1A03	DIN1	89879101	1	1
34P1A04	33P1A04	DOUT1	89879101	1	1
34P1A04	35P1A04	DOUT1	89879101	2	2
34P1A05	33P1A05	DIN2	89879101	1	1
34P1A05	35P1A05	DIN2	89879101	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
34P1A06	35P1A06	DOUT2	89879101	2	2
34P1A06	33P1A06	DOUT2	89879101	1	1
34P1A07	33P1A07	DIN4	89879101	1	1
34P1A07	35P1A07	DIN4	89879101	2	2
34P1A08	33P1A08	DOUT3	89879101	1	1
34P1A08	35P1A08	DOUT3	89879101	2	2
34P1A09	33P1A09	DOUT4	89879101	1	1
34P1A09	35P1A09	DOUT4	89879101	2	2
34P1A14	35P1A14	DOUT5	89879101	2	2
34P1A14	33P1A14	DOUT5	89879101	1	1
34P1A15	33P1A15	DIN6	89879101	1	1
34P1A15	35P1A15	DIN6	89879101	2	2
34P1A17	33P1A17	DOUT6	89879101	1	1
34P1A17	35P1A17	DOUT6	89879101	2	2
34P1A18	35P1A18	DIN7	89879101	2	2
34P1A18	33P1A18	DIN7	89879101	1	1
34P1A19	33P1A19	DOUT7	89879101	1	1
34P1A19	35P1A19	DOUT7	89879101	2	2
34P1A20	35P1A20	DOUT8	89879101	2	2
34P1A20	33P1A20	DOUT8	89879101	1	1
34P1A20	33P1A25	DOUT9	89879101	1	1
34P1A25	35P1A20	DOUT9	89879101	2	2
34P1A27	35P1A27	DIN11	89879101	2	2
34P1A27	33P1A27	DIN11	89879101	1	1
34P1A28	35P1A28	DIN10	89879101	2	2
34P1A28	33P1A28	DIN10	89879101	1	1
34P1A30	33P1A30	DOUT11	89879101	1	1
34P1A30	35P1A30	DOUT11	89879101	2	2
34P1A31	35P1A31	DOUT12	89879101	2	2
34P1A31	33P1A31	DOUT12	89879101	1	1
34P1B03	33P1B03	DIN0	89879101	1	1
34P1B03	35P1B03	DIN0	89879101	2	2
34P1B07	33P1B07	DIN3	89879101	1	1
34P1B07	35P1B07	DIN3	89879101	2	2
34P1B16	35P1B16	DIN5	89879101	2	2
34P1B16	33P1B16	DIN5	89879101	1	1
34P1B19	35P1B19	DIN8	89879101	2	2
34P1B19	33P1B19	DIN8	89879101	1	1
34P1B20	35P1B20	DIN9	89879101	2	2
34P1B20	33P1B20	DIN9	89879101	1	1
34P1B24	33P1B24	DOUT10	89879101	1	1
34P1B24	35P1B24	DOUT10	89879101	2	2
34P1B25	33P1B25	DIN12	89879101	1	1
34P1B25	35P1B25	DIN12	89879101	2	2
34P1B26	33P1B26	DIN15	89879101	1	1
34P1B26	35P1B26	DIN15	89879101	2	2
34P1B27	35P1B27	DIN13	89879101	2	2
34P1B27	33P1B27	DIN13	89879101	1	1
34P1B28	35P1B28	DIN14	89879101	2	2
34P1B28	33P1B28	DIN14	89879101	1	1
34P1B29	33P1B29	DOUT13	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
34P1B29	35P1B29	DOUT13	89879101	2	2
34P1B30	35P1B30	DOUT14	89879101	2	2
34P1B30	33P1B30	DOUT14	89879101	1	1
34P1B31	33P1B31	DOUT15	89879101	1	1
34P1B31	35P1B31	DOUT15	89879101	2	2
34P2A01	33P2A01	DOUT16	89879101	1	1
34P2A01	35P2A01	DOUT16	89879101	2	2
34P2A02	35P2A02	DOUT17	89879101	2	2
34P2A02	33P2A02	DOUT17	89879101	1	1
34P2A04	35P2A04	DIN16	89879101	2	2
34P2A04	33P2A04	DIN16	89879101	1	1
34P2A05	35P2A05	DIN17	89879101	2	2
34P2A05	33P2A05	DIN17	89879101	1	1
34P2A06	28P2B07	MDX5*	89879100	1	1
34P2A07	35P2A07	STROBE*	89879101	2	2
34P2A07	33P2A07	STROBE*	89879101	1	1
34P2A20	33P2A20	REF*	89879101	1	1
34P2A20	35P2A20	REF*	89879101	2	2
34P2A21	35P2A21	DISABLE	89879101	2	2
34P2A21	33P2A21	DISABLE	89879101	1	1
34P2A23	33P2A23	ACA7	89879101	1	1
34P2A23	35P2A23	ACA7	89879101	2	2
34P2A24	33P2A24	1K3*	89879101	1	1
34P2A24	35P2A24	1K3*	89879101	2	2
34P2A25	33P2A25	ARA0	89879101	1	1
34P2A25	35P2A25	ARA0	89879101	2	2
34P2A26	35P2A26	CE*	89879101	2	2
34P2A26	33P2A26	CE*	89879101	1	1
34P2A27	33P2A27	ACA9	89879101	1	1
34P2A27	35P2A27	ACA9	89879101	2	2
34P2A28	33P2A28	ARA2	89879101	1	1
34P2A28	35P2A28	ARA2	89879101	2	2
34P2A29	33P2A29	ARA1	89879101	1	1
34P2A29	35P2A29	ARA1	89879101	2	2
34P2A30	33P2A30	1K0*	89879101	1	1
34P2A30	35P2A30	1K0*	89879101	2	2
34P2B01	28P2B06	DX5*	89879100	1	1
34P2B22	35P2B22	ACA8	89879101	2	2
34P2B22	33P2B22	ACA8	89879101	1	1
34P2B23	33P2B23	ACA6	89879101	1	1
34P2B23	35P2B23	ACA6	89879101	2	2
34P2B24	33P2B24	1K2*	89879101	1	1
34P2B24	35P2B24	1K2*	89879101	2	2
34P2B25	35P2B25	ARA3	89879101	2	2
34P2B25	33P2B25	ARA3	89879101	1	1
34P2B26	33P2B26	ACA5	89879101	1	1
34P2B26	35P2B26	ACA5	89879101	2	2
34P2B27	33P2B27	R/W	89879101	1	1
34P2B27	35P2B27	R/W	89879101	2	2
34P2B28	33P2B28	ARA4	89879101	1	1
34P2B28	35P2B28	ARA4	89879101	2	2

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
34P2B29	33P2B29	1K1*	89879101	1	1
34P2B29	35P2B29	1K1*	89879101	2	2
34P2B30	33P2B30	MPWR*	89879101	1	1
34P2B30	35P2B30	MPWR*	89879101	2	2
35P1A02	34P1A02	DOUT0	89879101	2	2
35P1A02	36P1A02	DOUT0	89879101	1	1
35P1A03	36P1A03	DIN1	89879101	1	1
35P1A03	34P1A03	DIN1	89879101	2	2
35P1A04	36P1A04	DOUT1	89879101	1	1
35P1A04	34P1A04	DOUT1	89879101	2	2
35P1A05	36P1A05	DIN2	89879101	1	1
35P1A05	34P1A05	DIN2	89879101	2	2
35P1A06	36P1A06	DOUT2	89879101	1	1
35P1A06	34P1A06	DOUT2	89879101	2	2
35P1A07	36P1A07	DIN4	89879101	1	1
35P1A07	34P1A07	DIN4	89879101	2	2
35P1A08	36P1A08	DOUT3	89879101	1	1
35P1A08	34P1A08	DOUT3	89879101	2	2
35P1A09	34P1A09	DOUT4	89879101	2	2
35P1A09	36P1A09	DOUT4	89879101	1	1
35P1A14	34P1A14	DOUT5	89879101	2	2
35P1A14	36P1A14	DOUT5	89879101	1	1
35P1A15	34P1A15	DIN6	89879101	2	2
35P1A15	36P1A15	DIN6	89879101	1	1
35P1A17	36P1A17	DOUT6	89879101	1	1
35P1A17	34P1A17	DOUT6	89879101	2	2
35P1A18	36P1A18	DIN7	89879101	1	1
35P1A18	34P1A18	DIN7	89879101	2	2
35P1A19	34P1A19	DOUT7	89879101	2	2
35P1A19	36P1A19	DOUT7	89879101	1	1
35P1A20	34P1A20	DOUT8	89879101	2	2
35P1A20	36P1A20	DOUT8	89879101	1	1
35P1A20	34P1A25	DOUT9	89879101	2	2
35P1A25	36P1A20	DOUT9	89879101	1	1
35P1A27	36P1A27	DIN11	89879101	1	1
35P1A27	34P1A27	DIN11	89879101	2	2
35P1A28	36P1A28	DIN10	89879101	1	1
35P1A28	34P1A28	DIN10	89879101	2	2
35P1A30	34P1A30	DOUT11	89879101	2	2
35P1A30	36P1A30	DOUT11	89879101	1	1
35P1A31	36P1A31	DOUT12	89879101	1	1
35P1A31	34P1A31	DOUT12	89879101	2	2
35P1B03	36P1B03	DIN0	89879101	1	1
35P1B03	34P1B03	DIN0	89879101	2	2
35P1B07	36P1B07	DIN3	89879101	1	1
35P1B07	34P1B07	DIN3	89879101	2	2
35P1B16	34P1B16	DIN5	89879101	2	2
35P1B16	36P1B16	DIN5	89879101	1	1
35P1B19	36P1B19	DIN8	89879101	1	1
35P1B19	34P1B19	DIN8	89879101	2	2
35P1B20	36P1B20	DIN9	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
35P1B20	34P1B20	DIN9	89879101	2	2
35P1B24	34P1B24	DOUT10	89879101	2	2
35P1B24	36P1B24	DOUT10	89879101	1	1
35P1B25	36P1B25	DIN12	89879101	1	1
35P1B25	34P1B25	DIN12	89879101	2	2
35P1B26	34P1B26	DIN15	89879101	2	2
35P1B26	36P1B26	DIN15	89879101	1	1
35P1B27	36P1B27	DIN13	89879101	1	1
35P1B27	34P1B27	DIN13	89879101	2	2
35P1B28	36P1B28	DIN14	89879101	1	1
35P1B28	34P1B28	DIN14	89879101	2	2
35P1B29	34P1B29	DOUT13	89879101	2	2
35P1B29	36P1B29	DOUT13	89879101	1	1
35P1B30	36P1B30	DOUT14	89879101	1	1
35P1B30	34P1B30	DOUT14	89879101	2	2
35P1B31	34P1B31	DOUT15	89879101	2	2
35P1B31	36P1B31	DOUT15	89879101	1	1
35P2A01	36P2A01	DOUT16	89879101	1	1
35P2A01	34P2A01	DOUT16	89879101	2	2
35P2A02	34P2A02	DOUT17	89879101	2	2
35P2A02	36P2A02	DOUT17	89879101	1	1
35P2A04	34P2A04	DIN16	89879101	2	2
35P2A04	36P2A04	DIN16	89879101	1	1
35P2A05	34P2A05	DIN17	89879101	2	2
35P2A05	36P2A05	DIN17	89879101	1	1
35P2A06	28P2A07	MDX6*	89879100	1	1
35P2A07	36P2A07	STROBE*	89879101	1	1
35P2A07	34P2A07	STROBE*	89879101	2	2
35P2A20	34P2A20	REF*	89879101	2	2
35P2A20	36P2A20	REF*	89879101	1	1
35P2A21	36P2A21	DISABLE	89879101	1	1
35P2A21	34P2A21	DISABLE	89879101	2	2
35P2A23	36P2A23	ACA7	89879101	1	1
35P2A23	34P2A23	ACA7	89879101	2	2
35P2A24	36P2A24	1K3*	89879101	1	1
35P2A24	34P2A24	1K3*	89879101	2	2
35P2A25	36P2A25	ARA0	89879101	1	1
35P2A25	34P2A25	ARA0	89879101	2	2
35P2A26	36P2A26	CE*	89879101	1	1
35P2A26	34P2A26	CE*	89879101	2	2
35P2A27	36P2A27	ACA9	89879101	1	1
35P2A27	34P2A27	ACA9	89879101	2	2
35P2A28	34P2A28	ARA2	89879101	2	2
35P2A28	36P2A28	ARA2	89879101	1	1
35P2A29	34P2A29	ARA1	89879101	2	2
35P2A29	36P2A29	ARA1	89879101	1	1
35P2A30	36P2A30	1K0*	89879101	1	1
35P2A30	34P2A30	1K0*	89879101	2	2
35P2B01	28P2B05	DX6*	89879100	1	1
35P2B22	34P2B22	ACA8	89879101	2	2
35P2B22	36P2B22	ACA8	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
35P2B23	36P2B23	ACA6	89879101	1	1
35P2B23	34P2B23	ACA6	89879101	2	2
35P2B24	36P2B24	1K2*	89879101	1	1
35P2B24	34P2B24	1K2*	89879101	2	2
35P2B25	34P2B25	ARA3	89879101	2	2
35P2B25	36P2B25	ARA3	89879101	1	1
35P2B26	36P2B26	ACA5	89879101	1	1
35P2B26	34P2B26	ACA5	89879101	2	2
35P2B27	36P2B27	R/W	89879101	1	1
35P2B27	34P2B27	R/W	89879101	2	2
35P2B28	36P2B28	ARA4	89879101	1	1
35P2B28	34P2B28	ARA4	89879101	2	2
35P2B29	36P2B29	1K1*	89879101	1	1
35P2B29	34P2B29	1K1*	89879101	2	2
35P2B30	34P2B30	MPWR*	89879101	2	2
35P2B30	36P2B30	MPWR*	89879101	1	1
36P1A02	35P1A02	DOUT0	89879101	1	1
36P1A03	35P1A03	DIN1	89879101	1	1
36P1A04	35P1A04	DOUT1	89879101	1	1
36P1A05	35P1A05	DIN2	89879101	1	1
36P1A06	35P1A06	DOUT2	89879101	1	1
36P1A07	35P1A07	DIN4	89879101	1	1
36P1A08	35P1A08	DOUT3	89879101	1	1
36P1A09	35P1A09	DOUT4	89879101	1	1
36P1A14	35P1A14	DOUT5	89879101	1	1
36P1A15	35P1A15	DIN6	89879101	1	1
36P1A17	35P1A17	DOUT6	89879101	1	1
36P1A18	35P1A18	DIN7	89879101	1	1
36P1A19	35P1A19	DOUT7	89879101	1	1
36P1A20	35P1A20	DOUT8	89879101	1	1
36P1A20	35P1A25	DOUT9	89879101	1	1
36P1A27	35P1A27	DIN11	89879101	1	1
36P1A28	35P1A28	DIN10	89879101	1	1
36P1A30	35P1A30	DOUT11	89879101	1	1
36P1A31	35P1A31	DOUT12	89879101	1	1
36P1B03	35P1B03	DIN0	89879101	1	1
36P1B07	35P1B07	DIN3	89879101	1	1
36P1B16	35P1B16	DIN5	89879101	1	1
36P1B19	35P1B19	DIN8	89879101	1	1
36P1B20	35P1B20	DIN9	89879101	1	1
36P1B24	35P1B24	DOUT10	89879101	1	1
36P1B25	35P1B25	DIN12	89879101	1	1
36P1B26	35P1B26	DIN15	89879101	1	1
36P1B27	35P1B27	DIN13	89879101	1	1
36P1B28	35P1B28	DIN14	89879101	1	1
36P1B29	35P1B29	DOUT13	89879101	1	1
36P1B30	35P1B30	DOUT14	89879101	1	1
36P1B31	35P1B31	DOUT15	89879101	1	1
36P2A01	35P2A01	DOUT16	89879101	1	1
36P2A02	35P2A02	DOUT17	89879101	1	1
36P2A04	35P2A04	DIN16	89879101	1	1

FROM	TO	SIGNAL-NAME	W.L.	FR.LEV	TO.LEV
36P2A05	35P2A05	DIN17	89879101	1	1
36P2A06	28P2A08	MDX7*	89879100	1	1
36P2A07	35P2A07	STROBE*	89879101	1	1
36P2A20	35P2A20	REF*	89879101	1	1
36P2A21	35P2A21	DISABLE	89879101	1	1
36P2A23	35P2A23	ACA7	89879101	1	1
36P2A24	35P2A24	1K3*	89879101	1	1
36P2A25	35P2A25	ARA0	89879101	1	1
36P2A26	35P2A26	CE*	89879101	1	1
36P2A27	35P2A27	ACA9	89879101	1	1
36P2A28	35P2A28	ARA2	89879101	1	1
36P2A29	35P2A29	ARA1	89879101	1	1
36P2A30	35P2A30	1K0*	89879101	1	1
36P2B01	28P2A05	DX7*	89879100	1	1
36P2B22	35P2B22	ACA8	89879101	1	1
36P2B23	35P2B23	ACA6	89879101	1	1
36P2B24	35P2B24	1K2*	89879101	1	1
36P2B25	35P2B25	ARA3	89879101	1	1
36P2B26	35P2B26	ACA5	89879101	1	1
36P2B27	35P2B27	R/W	89879101	1	1
36P2B28	35P2B28	ARA4	89879101	1	1
36P2B29	35P2B29	1K1*	89879101	1	1
36P2B30	35P2B30	MPWR*	89879101	1	1

TABLE 9-5 WIRE LIST BT148 EXPANSION ENCLOSURE BACKPLANE
(signal name order)

02P1A21,06P1A21 32KW
06P1A21,14P1A21 32KW
14P1A21,22P1A21 32KW
14P1B18,22P1B18 AUTOLOAD
02P1B18,06P1B18 AUTOLOAD
06P1B18,14P1B18 AUTOLOAD
12P1B07,13P1B07 CHI*
11P1B07,12P1B07 CHI*
03P1B07,04P1B07 CHI*
05P1B07,11P1B07 CHI*
04P1B07,05P1B07 CHI*
01P1B07,03P1B07 CHI*
19P1B07,20P1B07 CHI*
13P1B07,19P1B07 CHI*
20P1B07,21P1B07 CHI*
13P1B23,19P1B23 MC*
19P1B23,20P1B23 MC*
20P1B23,21P1B23 MC*
14P1A09,22P1A09 MC*
06P1A09,14P1A09 MC*
11P1B23,12P1B23 MC*
04P1B23,05P1B23 MC*
03P1B23,04P1B23 MC*
01P1B23,03P1B23 MC*
02P1A09,06P1A09 MC*
12P1B23,13P1B23 MC*
05P1B23,11P1B23 MC*
01P1A03,03P1A03 OA0*
05P1A03,11P1A03 OA0*
11P1A03,12P1A03 OA0*
12P1A03,13P1A03 OA0*
03P1A03,04P1A03 OA0*
04P1A03,05P1A03 OA0*
13P1A03,19P1A03 OA0*
19P1A03,20P1A03 OA0*
20P1A03,21P1A03 OA0*
20P1B01,21P1B01 OA1*
19P1B01,20P1B01 OA1*
03P1B01,04P1B01 OA1*
04P1B01,05P1B01 OA1*
11P1B01,12P1B01 OA1*
13P1B01,19P1B01 OA1*
05P1B01,11P1B01 OA1*
01P1B01,03P1B01 OA1*
12P1B01,13P1B01 OA1*
12P1B02,13P1B02 OA2*
11P1B02,12P1B02 OA2*
05P1B02,11P1B02 OA2*
04P1B02,05P1B02 OA2*
13P1B02,19P1B02 OA2*
03P1B02,04P1B02 OA2*
01P1B02,03P1B02 OA2*
20P1B02,21P1B02 OA2*
19P1B02,20P1B02 OA2*
19P1A06,20P1A06 OA3*
20P1A06,21P1A06 OA3*
11P1A06,12P1A06 OA3*
12P1A06,13P1A06 OA3*
05P1A06,11P1A06 OA3*

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04P1A06•05P1A06 0A3*
01P1A06•03P1A06 0A3*
03P1A06•04P1A06 0A3*
13P1A06•19P1A06 0A3*
13P1A07•19P1A07 0A4*
03P1A07•04P1A07 0A4*
12P1A07•13P1A07 0A4*
01P1A07•03P1A07 0A4*
05P1A07•11P1A07 0A4*
11P1A07•12P1A07 0A4*
04P1A07•05P1A07 0A4*
20P1A07•21P1A07 0A4*
19P1A07•20P1A07 0A4*
20P1A01•21P1A01 0A5*
19P1A01•20P1A01 0A5*
12P1A01•13P1A01 0A5*
04P1A01•05P1A01 0A5*
11P1A01•12P1A01 0A5*
03P1A01•04P1A01 0A5*
05P1A01•11P1A01 0A5*
13P1A01•19P1A01 0A5*
01P1A01•03P1A01 0A5*
01P1A02•03P1A02 0A6*
13P1A02•19P1A02 0A6*
05P1A02•11P1A02 0A6*
03P1A02•04P1A02 0A6*
11P1A02•12P1A02 0A6*
04P1A02•05P1A02 0A6*
12P1A02•13P1A02 0A6*
20P1A02•21P1A02 0A6*
19P1A02•20P1A02 0A6*
19P1B03•20P1B03 0A7*
20P1B03•21P1B03 0A7*
13P1B03•19P1B03 0A7*
11P1B03•12P1B03 0A7*
03P1B03•04P1B03 0A7*
05P1B03•11P1B03 0A7*
01P1B03•03P1B03 0A7*
04P1B03•05P1B03 0A7*
12P1B03•13P1B03 0A7*
12P1B04•13P1B04 0A8*
04P1B04•05P1B04 0A8*
01P1B04•03P1B04 0A8*
11P1B04•12P1B04 0A8*
05P1B04•11P1B04 0A8*
13P1B04•19P1B04 0A8*
03P1B04•04P1B04 0A8*
19P1B04•20P1B04 0A8*
20P1B04•21P1B04 0A8*
20P1B05•21P1B05 CA9*
19P1B05•20P1B05 0A9*
04P1B05•05P1B05 0A9*
13P1B05•19P1B05 0A9*
05P1B05•11P1B05 0A9*
11P1B05•12P1B05 0A9*
01P1B05•03P1B05 CA9*
03P1B05•04P1B05 0A9*
12P1B05•13P1B05 0A9*
05P1B06•11P1B06 0A10*
12P1B06•13P1B06 0A10*
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04P1B06,05P1B06 0A10*
01P1B06,03P1B06 0A10*
11P1B06,12P1B06 0A10*
03P1B06,04P1B06 0A10*
13P1B06,19P1B06 0A10*
19P1B06,20P1B06 0A10*
20P1B06,21P1B06 0A10*
20P1A05,21P1A05 0A11*
01P1A05,03P1A05 0A11*
11P1A05,12P1A05 0A11*
12P1A05,13P1A05 0A11*
03P1A05,04P1A05 0A11*
19P1A05,20P1A05 0A11*
05P1A05,11P1A05 0A11*
04P1A05,05P1A05 0A11*
13P1A05,19P1A05 0A11*
01P1A04,03P1A04 0A12*
11P1A04,12P1A04 0A12*
04P1A04,05P1A04 0A12*
03P1A04,04P1A04 0A12*
19P1A04,20P1A04 0A12*
12P1A04,13P1A04 0A12*
05P1A04,11P1A04 0A12*
13P1A04,19P1A04 0A12*
20P1A04,21P1A04 0A12*
20P1B09,21P1B09 0A13*
19P1B09,20P1B09 0A13*
11P1B09,12P1B09 0A13*
03P1B09,04P1B09 0A13*
05P1B09,11P1B09 0A13*
01P1B09,03P1B09 0A13*
13P1B09,19P1B09 0A13*
04P1B09,05P1B09 0A13*
12P1B09,13P1B09 0A13*
12P1B10,13P1B10 0A14*
13P1B10,19P1B10 0A14*
05P1B10,11P1B10 0A14*
03P1B10,04P1B10 0A14*
01P1B10,03P1B10 0A14*
11P1B10,12P1B10 0A14*
19P1B10,20P1B10 0A14*
04P1B10,05P1B10 0A14*
20P1B10,21P1B10 0A14*
05P1A11,11P1A11 0A15*
04P1A11,05P1A11 0A15*
11P1A11,12P1A11 0A15*
12P1A11,13P1A11 0A15*
13P1A11,19P1A11 0A15*
20P1A11,21P1A11 0A15*
19P1A11,20P1A11 0A15*
03P1A11,04P1A11 0A15*
01P1A11,03P1A11 0A15*
02P1A17,06P1A17 PEL*
06P1A17,14P1A17 PEL*
14P1A17,22P1A17 PEL*
03P1A23,04P1A23 PRTM*
05P1A23,11P1A23 PRTM*
11P1A23,12P1A23 PRTM*
19P1A23,20P1A23 PRTM*
01P1A23,03P1A23 PRTM*
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20P1A23•21P1A23 PRTM*
13P1A23•19P1A23 PRTM*
12P1A23•13P1A23 PRTM*
04P1A23•05P1A23 PRTM*
05P1A12•11P1A12 Q0
12P1A12•13P1A12 Q0
03P1A12•04P1A12 Q0
11P1A12•12P1A12 Q0
04P1A12•05P1A12 Q0
01P1A12•03P1A12 Q0
13P1A12•19P1A12 Q0
20P1A12•21P1A12 Q0
19P1A12•20P1A12 Q0
05P1B12•11P1B12 Q1
13P1B12•19P1B12 Q1
04P1B12•05P1B12 Q1
20P1B12•21P1B12 Q1
01P1B12•03P1B12 Q1
03P1B12•04P1B12 Q1
12P1B12•13P1B12 Q1
19P1B12•20P1B12 Q1
11P1B12•12P1B12 Q1
04P1A13•05P1A13 Q2
01P1A13•03P1A13 Q2
11P1A13•12P1A13 Q2
12P1A13•13P1A13 Q2
20P1A13•21P1A13 Q2
13P1A13•19P1A13 Q2
05P1A13•11P1A13 Q2
03P1A13•04P1A13 Q2
19P1A13•20P1A13 Q2
13P1B13•19P1B13 Q3
04P1B13•05P1B13 Q3
19P1B13•20P1B13 Q3
20P1B13•21P1B13 Q3
01P1B13•03P1B13 Q3
12P1B13•13P1B13 Q3
05P1B13•11P1B13 Q3
03P1B13•04P1B13 Q3
11P1B13•12P1B13 Q3
12P1A14•13P1A14 Q4
11P1A14•12P1A14 Q4
04P1A14•05P1A14 Q4
13P1A14•19P1A14 Q4
20P1A14•21P1A14 Q4
01P1A14•03P1A14 Q4
05P1A14•11P1A14 Q4
03P1A14•04P1A14 Q4
19P1A14•20P1A14 Q4
19P1B14•20P1B14 Q5
04P1B14•05P1B14 Q5
20P1B14•21P1B14 Q5
03P1B14•04P1B14 Q5
05P1B14•11P1B14 Q5
13P1B14•19P1B14 Q5
01P1B14•03P1B14 Q5
12P1B14•13P1B14 Q5
11P1B14•12P1B14 Q5
12P1A15•13P1A15 Q6
04P1A15•05P1A15 Q6
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11P1A15•12P1A15 Q6
19P1A15•20P1A15 Q6
13P1A15•19P1A15 Q6
20P1A15•21P1A15 Q6
01P1A15•03P1A15 Q6
05P1A15•11P1A15 Q6
03P1A15•04P1A15 Q6
20P1B15•21P1B15 Q7
04P1B15•05P1B15 Q7
03P1B15•04P1B15 Q7
19P1B15•20P1B15 Q7
05P1B15•11P1B15 Q7
12P1B15•13P1B15 Q7
13P1B15•19P1B15 Q7
01P1B15•03P1B15 Q7
11P1B15•12P1B15 Q7
05P1A16•11P1A16 Q8
11P1A16•12P1A16 Q8
12P1A16•13P1A16 Q8
13P1A16•19P1A16 Q8
19P1A16•20P1A16 Q8
01P1A16•03P1A16 Q8
20P1A16•21P1A16 Q8
04P1A16•05P1A16 Q8
03P1A16•04P1A16 Q8
01P1B16•03P1B16 Q9
03P1B16•04P1B16 Q9
20P1B16•21P1B16 Q9
19P1B16•20P1B16 Q9
05P1B16•11P1B16 Q9
13P1B16•19P1B16 Q9
12P1B16•13P1B16 Q9
04P1B16•05P1B16 Q9
11P1B16•12P1B16 Q9
03P1A17•04P1A17 Q10
05P1A17•11P1A17 Q10
12P1A17•13P1A17 Q10
01P1A17•03P1A17 Q10
11P1A17•12P1A17 Q10
19P1A17•20P1A17 Q10
13P1A17•19P1A17 Q10
20P1A17•21P1A17 Q10
04P1A17•05P1A17 Q10
19P1B17•20P1B17 Q11
20P1B17•21P1B17 Q11
03P1B17•04P1B17 Q11
01P1B17•03P1B17 Q11
13P1B17•19P1B17 Q11
12P1B17•13P1B17 Q11
05P1B17•11P1B17 Q11
04P1B17•05P1B17 Q11
11P1B17•12P1B17 Q11
19P1A18•20P1A18 Q12
05P1A18•11P1A18 Q12
03P1A18•04P1A18 Q12
11P1A18•12P1A18 Q12
12P1A18•13P1A18 Q12
20P1A18•21P1A18 Q12
01P1A18•03P1A18 Q12
04P1A18•05P1A18 Q12

13P1A18,19P1A18 Q12
05P1B18,11P1B18 Q13
20P1B18,21P1B18 Q13
01P1B18,03P1B18 Q13
13P1B18,19P1B18 Q13
12P1B18,13P1B18 Q13
19P1B18,20P1B18 Q13
11P1B18,12P1B18 Q13
04P1B18,05P1B18 Q13
03P1B18,04P1B18 Q13
04P1A19,05P1A19 Q14
05P1A19,11P1A19 Q14
11P1A19,12P1A19 Q14
12P1A19,13P1A19 Q14
01P1A19,03P1A19 Q14
20P1A19,21P1A19 Q14
13P1A19,19P1A19 Q14
19P1A19,20P1A19 Q14
03P1A19,04P1A19 Q14
05P1B19,11P1B19 Q15
13P1B19,19P1B19 Q15
12P1B19,13P1B19 Q15
20P1B19,21P1B19 Q15
19P1B19,20P1B19 Q15
11P1B19,12P1B19 Q15
04P1B19,05P1B19 Q15
01P1B19,03P1B19 Q15
03P1B19,04P1B19 Q15
04P1A21,05P1A21 READ*
05P1A21,11P1A21 READ*
12P1A21,13P1A21 READ*
11P1A21,12P1A21 READ*
01P1A21,03P1A21 READ*
13P1A21,19P1A21 READ*
03P1A21,04P1A21 READ*
19P1A21,20P1A21 READ*
20P1A21,21P1A21 READ*
05P1B22,11P1B22 REJECT*
01P1B22,03P1B22 REJECT*
19P1B22,20P1B22 REJECT*
12P1B22,13P1B22 REJECT*
20P1B22,21P1B22 REJECT*
03P1B22,04P1B22 REJECT*
13P1B22,19P1B22 REJECT*
04P1B22,05P1B22 REJECT*
11P1B22,12P1B22 REJECT*
04P1A22,05P1A22 REPLY*
12P1A22,13P1A22 REPLY*
13P1A22,19P1A22 REPLY*
01P1A22,03P1A22 REPLY*
20P1A22,21P1A22 REPLY*
03P1A22,04P1A22 REPLY*
11P1A22,12P1A22 REPLY*
05P1A22,11P1A22 REPLY*
19P1A22,20P1A22 REPLY*
06P1B12,14P1B12 SS*
02P1B12,06P1B12 SS*
14P1B12,22P1B12 SS*
06P1B23,14P1B23 SA0
14P1B23,22P1B23 SA0

02P1B23,06P1B23 SA0
06P1A03,14P1A03 SD0
14P1A03,22P1A03 SD0
02P1A03,06P1A03 SD0
06P1B24,14P1B24 SA1
14P1B24,22P1B24 SA1
02P1B24,06P1B24 SA1
14P1B01,22P1B01 SD1
02P1B01,06P1B01 SD1
06P1B01,14P1B01 SD1
06P1B25,14P1B25 SA2
14P1B25,22P1B25 SA2
02P1B25,06P1B25 SA2
14P1B02,22P1B02 SD2
02P1B02,06P1B02 SD2
06P1B02,14P1B02 SD2
06P1B26,14P1B26 SA3
14P1B26,22P1B26 SA3
02P1B26,06P1B26 SA3
14P1A06,22P1A06 SD3
06P1A06,14P1A06 SD3
02P1A06,06P1A06 SD3
14P1B27,22P1B27 SA4
06P1B27,14P1B27 SA4
02P1B27,06P1B27 SA4
14P1A07,22P1A07 SD4
02P1A07,06P1A07 SD4
06P1A07,14P1A07 SD4
14P1B28,22P1B28 SA5
06P1B28,14P1B28 SA5
02P1B28,06P1B28 SA5
06P1A01,14P1A01 SD5
06P1B30,14P1B30 SA6
14P1B30,22P1B30 SA6
02P1B30,06P1B30 SA6
14P1A02,22P1A02 SD6
06P1A02,14P1A02 SD6
02P1A02,06P1A02 SD6
02P1B31,06P1B31 SA7
14P1B31,22P1B31 SA7
06P1B31,14P1B31 SA7
06P1B03,14P1B03 SD7
14P1B03,22P1B03 SD7
02P1B03,06P1B03 SD7
06P1A23,14P1A23 SA8
02P1A23,06P1A23 SA8
14P1A23,22P1A23 SA8
14P1B04,22P1B04 SD8
02P1B04,06P1B04 SD8
06P1B04,14P1B04 SD8
06P1A24,14P1A24 SA9
14P1A24,22P1A24 SA9
02P1A24,06P1A24 SA9
02P1B05,06P1B05 SD9
14P1B05,22P1B05 SD9
06P1B05,14P1B05 SD9
06P1B14,14P1B14 SPI*
02P1B14,06P1B14 SPI*
14P1B14,22P1B14 SPI*
06P1A15,14P1A15 SRQ*

02P1A15,06P1A15 SRQ*
14P1A15,22P1A15 SRQ*
06P1A25,14P1A25 SA10
14P1A25,22P1A25 SA10
02P1A25,06P1A25 SA10
14P1B06,22P1B06 SD10
02P1B06,06P1B06 SD10
06P1B06,14P1B06 SD10
14P1A26,22P1A26 SA11
06P1A26,14P1A26 SA11
02P1A26,06P1A26 SA11
06P1A05,14P1A05 SD11
02P1A05,06P1A05 SD11
14P1A05,22P1A05 SD11
02P1A27,06P1A27 SA12
14P1A27,22P1A27 SA12
06P1A27,14P1A27 SA12
06P1A04,14P1A04 SD12
14P1A04,22P1A04 SD12
02P1A04,06P1A04 SD12
06P1A28,14P1A28 SA13
02P1A28,06P1A28 SA13
14P1A28,22P1A28 SA13
02P1B09,06P1B09 SD13
06P1B09,14P1B09 SD13
14P1B09,22P1B09 SD13
06P1A30,14P1A30 SA14
02P1A30,06P1A30 SA14
14P1A30,22P1A30 SA14
02P1B10,06P1B10 SD14
06P1B10,14P1B10 SD14
14P1B10,22P1B10 SD14
02P1A31,06P1A31 SA15
06P1A31,14P1A31 SA15
14P1A31,22P1A31 SA15
02P1A11,06P1A11 SD15
14P1A11,22P1A11 SD15
06P1A11,14P1A11 SD15
02P1A18,06P1A18 SD16
06P1A18,14P1A18 SD16
14P1A18,22P1A18 SD16
06P1A20,14P1A20 SD17
02P1A20,06P1A20 SD17
14P1A20,22P1A20 SD17
06P1B21,14P1B21 SWRITE*
14P1B21,22P1B21 SWRITE*
02P1B21,06P1B21 SWRITE*
14P1A13,22P1A13 SRSM*
02P1A13,06P1A13 SRSM*
06P1A13,14P1A13 SRSM*
02P1B17,06P1B17 SVIO*
06P1B17,14P1B17 SVIO*
14P1B17,22P1B17 SVIO*
03P1A09,04P1A09 T.P.
01P1A09,03P1A09 T.P.
13P1A09,19P1A09 T.P.
19P1A09,20P1A09 T.P.
11P1A09,12P1A09 T.P.
04P1A09,05P1A09 T.P.
20P1A09,21P1A09 T.P.

WIRE LIST BT148

12P1A09,13P1A09 T.P.
05P1A09,11P1A09 T.P.
05P1A20,11P1A20 WEZ*
04P1A20,05P1A20 WEZ*
11P1A20,12P1A20 WEZ*
12P1A20,13P1A20 WEZ*
20P1A20,21P1A20 WEZ*
13P1A20,19P1A20 WEZ*
03P1A20,04P1A20 WEZ*
01P1A20,03P1A20 WEZ*
19P1A20,20P1A20 WEZ*
19P1B21,20P1B21 WRITE*
01P1B21,03P1B21 WRITE*
13P1B21,19P1B21 WRITE*
05P1B21,11P1B21 WRITE*
12P1B21,13P1B21 WRITE*
20P1B21,21P1B21 WRITE*
03P1B21,04P1B21 WRITE*
04P1B21,05P1B21 WRITE*
11P1B21,12P1B21 WRITE*

TABLE 9-6. CDT EXTERNAL CABLE ASSEMBLY WIRE LIST (P/N 89668300)

CDT CONNECTOR/PIN	WIRE GAUGE	WIRE COLOR	CPU CONNECTOR/ PIN	SIGNAL NAME
P1-2	AWG22	BLK	P14-51	CRT-TRANS
-3		RED	P14-57	CRT-REC
-7		GRN	P14-58	COMMON (GND)
P1-4	AWG22	WHT/BLU	P1-5*	CLEAR TO SEND jumpered to REQUEST TO SEND

* P1-5 (CLEAR TO SEND) is jumpered to P1-4 (REQUEST TO SEND) at assembly connector for CDT.

COMMENT SHEET

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